Reduction of Computational Burden on Observed Optimal Vector-Based FSMPC for SCIM Control fed 3L-NPC

Arya Kusumawardana, *Member, IAENG,* Muhammad Afnan Habibi, *Member, IAENG,* Langlang Gumilar, Hendi Purnata, Arfittariah

***Abstract*— This paper proposes a new mechanism to reduce the computational load on the FSMPC for SCIM control. The mechanism used is to reduce the number of candidate vectors that are calculated during the optimization process. Candidate vectors are reduced based on the results of conventional FSMPC observations. The candidate vector selection is based on the calculated sector based on the stator flux. Each sector's lowest vector occurrence percentage is eliminated and reconstructed to produce a new candidate vector. Based on the reconstruction results, the number of candidate vectors is less than in the conventional algorithm. Based on the test results, the proposed FSMPC stator current THD is more minor than conventional FSMPC. In addition, the robustness analysis of the proposed system shows better performance. This condition also proves that the proposed FSMPC can reduce the computational load significantly from conventional FSMPC, which is more than 43%.**

***Index Terms*—FSMPC, SCIM, Computational Burden, Electrical Drive, Motor Control**

I. Introduction

THE rapid development of computer technology, especially for embedded system applications, is in line with the development of Electrical Drive (ED) technology. The use of ED is quite diverse. It can be applied in industry for conveyor devices, servo motors, and also Heating Ventilation and Air Conditioning (HVAC) [1]. Moreover, ED has also been widely used as the prime mover of electric vehicles. The latest technologies, such as the Microcontroller (MCU) integration with the Digital Signal Processor (DSP), make realizing complex algorithms easier in discrete form. As a result, increasing efficiency is no longer centered on the power inverter technology but on the algorithm used.

Apart from the many types of motors that are currently being used and developed, the Squirrel Cage Induction Motor (SCIM) is excellent in terms of initial cost and maintenance compared to other types of motors [1]–[4]. Until now, many SCIM control algorithms have been developed. The most accessible algorithm to implement and still widely used in the industry is scalar control, namely V/f and I/f. Inasmuch as it is easy to implement, vector control is preferred to be used and developed to increasing efficiency. In general, the algorithm is divided into three types, including Direct Torque Control (DTC) [5], [6], Field Oriented Control (FOC) [7], [8], and Finite Set Model Predictive Control (FSMPC) [9], [10]. Compared to other types, FSMPC dominates because it is flexible in algorithm design and can generate PWM pulses without the additional modulation [11], [12]. FSMPC is still a topic that makes the attention of the researcher.

Turning to power conversion devices, especially power inverters, Neutral Point Clamped (NPC) inverters are one of the most popular types of Multi-Level Inverters (MLI) for compact systems. In addition, the inverter is also designed to be used in Medium Voltage (MV) applications [13]–[15]. In its development, FSMPC, with its flexibility, is also widely used to control NPC [16], [17].

FSMPC's flexibility is not the solitary advantage. The average PWM frequency generated will also be significant if the algorithm uses a relatively fast sampling time. The consequence is stress conditions on the inverter device. The study [18] utilizes deadbeat control to reduce the switching frequency generated by the FSMPC. However, the solution for decreasing the switching frequency is counter to the ripple torque generated.

On the other hand, research [19] raised the delay effect when using FSMPC. Delays in the system due to sampling time or computational problems can reduce performance. The problem is solved by making predictions sequentially. However, the more steps taken for predicting the state, the longer the computation will take.

The hallmark of FSMPC is its flexibility when designing the cost functions. Generally, when the controller objective of a system is designed to be more complex, it is also complicated to determine each optimized factor's weight. Interestingly, research [20] utilized two-stage optimization to solve this problem. The algorithm is also able to solve computational problems in FSMPC. Unlike conventional FSMPC, where control objectives are calculated and optimized simultaneously, research [21] performs calculations sequentially to reduce computational load. Utilizing Reference Stator Flux Vector Calculation (RSFVC), research [22] reduced computational complexity in FSMPC based on factor weights. In this case research [23] reduced the computational load without using factor weights. However, manipulation of factor weights can make FSMPC

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produce sub-optimal control signals.

To solve the computational problem of FSMPC, research [24] utilized Discrete Space Vector Modulation (DSVM) with MPC to reduce the enumeration of conventional FSMPC. The proposed algorithm was still able to avoid suboptimally. A simpler alternative, lookup tables, can also reduce computational problems [25].

Based on Selected Prediction Vector, research [26] reduced the computational load by 38% from conventional FSMPC. The proposed algorithm to obtain the optimal signal was not based on the whole vector calculation but used vector prediction. A similar process to lowering vector combinations also dropped the computational load [27]. Recently, research [28] succeeded in reducing NPC vectors candidate from 27 to 17 vectors. The computational load reduction was made through two-stage optimizations. The attraction of the vector candidate selection mechanism was the accuracy of the selection. If the candidate vector selected for calculation was unsuitable, then FSMPC would produce a sub-optimal and reduced system performance.

Indeed, the previous works could solve the computational burden, but the methods were not direct in obtaining the optimal voltage vector candidate. Approaching candidate vectors during optimization has become the main point in reducing the computation burden. For this reason, this work is focused on solving computational burden problems with an optimal selection procedure.

Conventional FSMPC utilizes the optimized signal to control the inverter device directly. The concept has a clear pattern. In other words, the FSMPC-optimized signal is not a non-random pattern. This condition can be observed to obtain the pattern of the FSMPC output signal. This study selected and utilized that pattern and operated it as an optimal vector candidate. To make the pattern observation and the choosing of it easier, this study divides the pattern of the optimization results into six sectors. Where the sector is generated from the stator flux signal as in DTC. The contributions of this study are as follows:

1. The proposed algorithm can reduce the computational load significantly compared to conventional FSMPC.
2. The proposed algorithm can also maintain the positive performance generated by FSMPC.

The system model needs to be obtained first to design the proposed algorithm. The SCIM modeling with three-level NPC (3L-NPC) is explained in more details in the following sub-section.

II. System Model

A model-based approach is often used to obtain adequate control system performance. As with other model approaches, FSMPC requires accurate system model information. In this case, two sub-systems are being modeled: SCIM and 3L-NPC inverter.

A. SCIM Model

SCIM is a complex type of motor. This complexity is shown in asynchronous conditions between mechanical and electrical speeds. This is because that type of motor does not have a permanent magnet on the rotor. Instead, SCIM uses a squirrel cage which causes that type of motor price to be relatively low compared to other AC motors.

Unlike studies [26], and [28], where SCIM was modeled in an equation involving an imaginary, this study represents a motor in vector form in a stationary frame. As shown by (1) and (2), SCIM is a 5th-order system with coupling parameters and nonlinear. Equation (1) represents the electrical characteristics, and (2) represents the mechanical characteristics of SCIM [29], [30].

$$\begin{aligned}
\frac{di_{s\alpha}^t}{dt} &= -\frac{1}{\tau_\sigma} i_{s\alpha}^t + \frac{k_r}{\sigma L_s \tau_r} \psi_{r\alpha}^t + \frac{k_r \omega_e^t}{\sigma L_s} \psi_{r\beta}^t \\
&\quad + \frac{1}{\sigma L_s} v_{s\alpha}^t \\
\frac{di_{s\beta}^t}{dt} &= -\frac{1}{\tau_\sigma} i_{s\beta}^t - \frac{k_r}{\sigma L_s \tau_r} \psi_{r\beta}^t + \frac{k_r \omega_e^t}{\sigma L_s} \psi_{r\alpha}^t \\
&\quad + \frac{1}{\sigma L_s} v_{s\beta}^t \\
\frac{d\psi_{r\alpha}^t}{dt} &= \frac{L_m}{\tau_r} i_{s\alpha}^t - \frac{1}{\tau_\sigma} \psi_{r\alpha}^t - \omega_e^t \psi_{r\beta}^t \\
\frac{d\psi_{r\beta}^t}{dt} &= \frac{L_m}{\tau_r} i_{s\beta}^t - \frac{1}{\tau_\sigma} \psi_{r\beta}^t - \omega_e^t \psi_{r\alpha}^t
\end{aligned} \tag{1}$$

$$\frac{d\omega_m^t}{dt} = \frac{T_e^t}{J_m} - \frac{f_d \omega_m^t}{J_m} - \frac{T_L^t}{J_m} \tag{2}$$

where the state variables $i_{s\alpha}$ and $i_{s\beta}$ are stator current in $\alpha\beta$-frame, $\psi_{r\alpha}$ and $\psi_{r\beta}$ are rotor fluxes in $\alpha\beta$-frame, while ω_m is the SCIM mechanical rotational speed. Given that (1) uses ω_e instead, then ω_m in (2) can be converted to get $\omega_e = Z_p \omega_m$, where Z_p is SCIM's pole pair. To represent the model more concisely, the superscript t sign in each state represents a function of time. There are several SCIM parameters defined as L_m, L_s, R_s, R_r, J_m, and f_d which are magnetizing inductance, stator inductance, stator resistance, rotor resistance, moment of inertia, and friction coefficient, while T_L is the load torque. In addition, each constant in (1) is defined as follows:

- Stator coupling coefficient, $k_s = \frac{L_m}{L_s}$
- Rotor coupling coefficient, $k_r = \frac{L_m}{L_r}$
- Leakage total coefficient, $\sigma = 1 - k_s k_r = 1 - \frac{L_m^2}{L_s L_r}$
- Equivalent resistance, $r_\sigma = R_s + k_r^2 R_r\ (\Omega)$
- Stator transient time constant, $\tau_\sigma = \frac{\sigma L_s}{r_\sigma}\ (s)$
- Stator time constant, $\tau_s = \frac{L_s}{R_s}(s)$
- Rotor time constant, $\tau_r = \frac{L_r}{R_r}(s)$
- Total leakage inductance, $\sigma L_s = \frac{L_s L_r - L_m^2}{L_r}$.

Based on the mechanical equation in (2), it can be seen that the T_e is not explicitly comprised in the model. However, T_e can be known or in other words can be estimated using (3).

$$T_e^t = 1.5 Z_p \left(\psi_{s\alpha}^t i_{s\beta}^t - \psi_{s\beta}^t i_{s\alpha}^t \right) \tag{3}$$

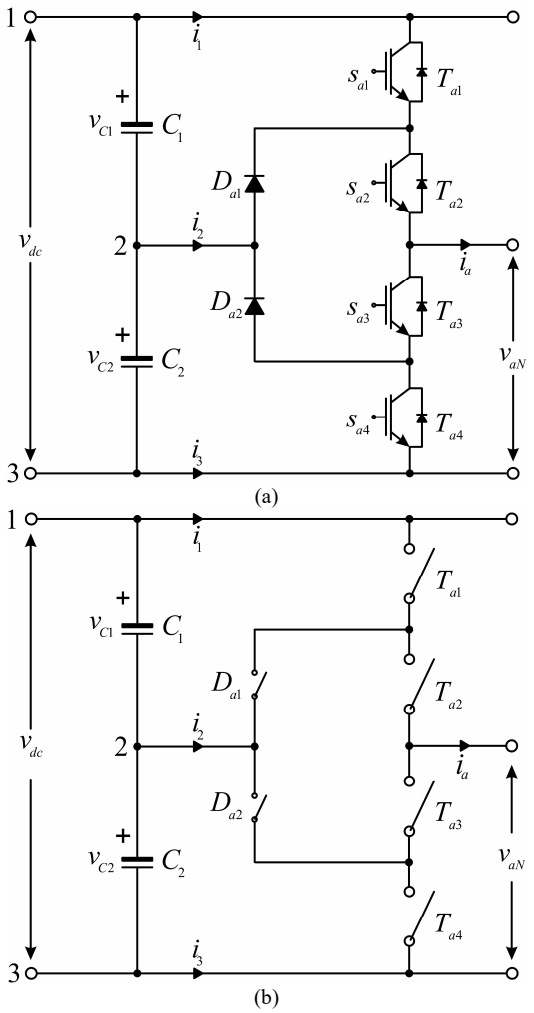


Fig. 1. One leg NPC Circuit; (a) Circuit in IGBT form; (b) Circuit in Switch form

Referring to (3), it can be seen that the stator fluxes $\psi_{\alpha s}$ and $\psi_{\beta s}$ need to be estimated. The two variables can be identified using (4).

$$\psi_{s\alpha}^{t} = \sigma L_s i_{s\alpha}^{t} + k_r \psi_{r\alpha}^{t}$$
$$\psi_{s\beta}^{t} = \sigma L_s i_{s\beta}^{t} + k_r \psi_{r\beta}^{t} \quad (4)$$

Thus, the two variables can be determined using the stator current and rotor flux.

B. 3L-NPC Model

SCIM control cannot be separated from the power inverter device. The development of power inverters is not limited to two-level inverters but has come to Multi-Level Inverters (MLI) to improve system performance by reducing torque ripple [31], [32]. One type of MLI that is popular and can be designed for compact systems is NPC. Specifically, in this study, the NPC used is a three-level type. A three-level voltage vector can be generated to reduce the torque ripple by utilizing a clamped diode on each leg. One leg of the 3L-NPC circuit is shown in Fig. 1.

It can be seen that T_{a1}, T_{a2} T_{a3}, dan T_{a4} are semiconductor switches such as IGBT with signals s_{a1}, s_{a2}, s_{a3}, and s_{a4}. The semiconductor switch is used to connect terminals 1, 2, and 3 to the output terminal a. The currents i_1, i_2, and i_3 are related to the switching signal from the NPC and the three-phase load current.

Based on the literature [30], there are three operating modes of the 3L-NPC, as shown in Fig.2. The three operating modes can be written as follows:

Mode 1: when T_{a1} and T_{a2} are active because the signals s_{a1} and s_{a2} are logic 1, then the two switches connect a to P. This causes $v_{aN} = v_{C1} + v_{C2}$. In other words, the current $i_1 = i_a$.

Mode 2: terminal a connected to N when T_{a2} and T_{a3} are active. So we can write $v_{aN} = v_{C2}$ and $i_2 = i_a$.

Mode 3: when in mode 3, terminal a is connected to N so that $v_{aN} = 0$.

In simple terms, the output voltage v_{xN} on a three-phase inverter is as (5)

$$v_{xN} = \begin{cases} v_{C1} + v_{C2} & \text{if } T_{x1}, T_{x2} = 1 \\ v_{C2} & \text{if } T_{x2}, T_{x3} = 1 \\ 0 & \text{if } T_{x3}, T_{x4} = 1 \end{cases} \forall x \in \{a, b, c\} \quad (5)$$

The relationship between the output terminal current and the current in each branch is as follows:

$$i_x = \begin{cases} i_P & \text{if } T_{x1}, T_{x2} = 1 \\ i_Z & \text{if } T_{x2}, T_{x3} = 1 \\ i_N & \text{if } T_{x3}, T_{x4} = 1 \end{cases} \forall x \in \{a, b, c\} \quad (6)$$

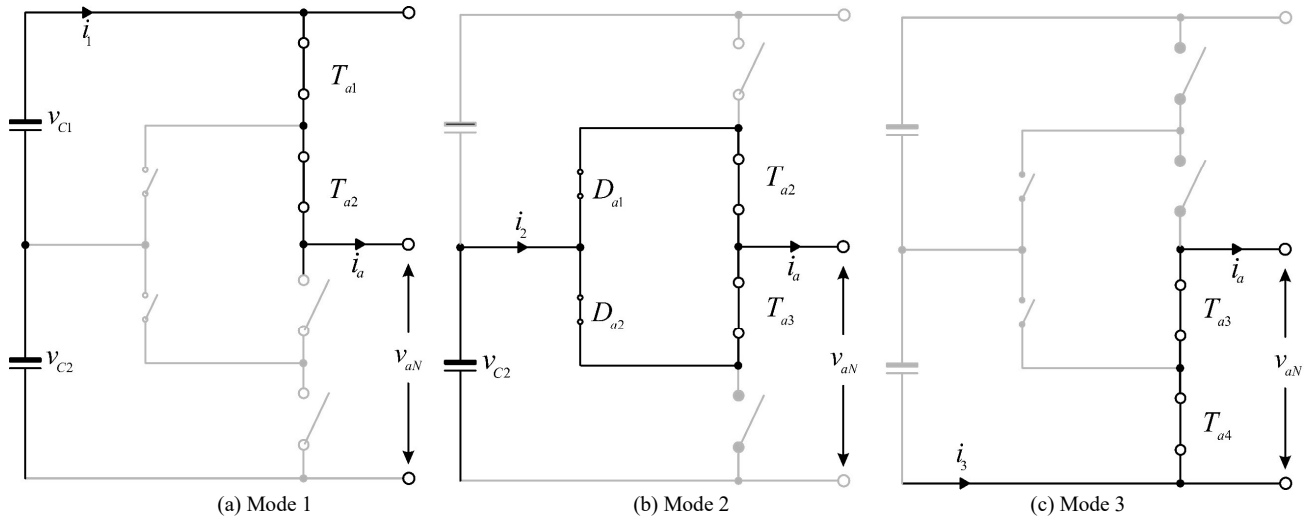


Fig. 2. Operation Mode of 3L-NPC

The switching vector is as follows:

$$S_x = \begin{cases} [2] \text{ if } T_{x1}, T_{x2} = 1 \\ [1] \text{ if } T_{x2}, T_{x3} = 1 \\ [0] \text{ if } T_{x3}, T_{x4} = 1 \end{cases} \forall x \in \{a, b, c\} \quad (7)$$

Based on the three conditions described, the relationship between the switching vector, the current, and the output voltage is shown in Table 1 [30]. In the abc-frame, the 3L-NPC output voltage is affected by the signals s_{a1}, s_{a2}, s_{b1}, s_{b2}, s_{c1}, and s_{c2}. The relationship between the six signals and the voltage across the capacitors v_{C1} and v_{C2} can be represented in (8)

TABLE I
RELATIONSHIP BETWEEN SWITCHING VECTOR AND OUTPUT VOLTAGE ON 3L-NPC

Switching Vector	Switching Signal				Output Voltage	Input Current		
S_x	s_{x1}	s_{x2}	s_{x3}	s_{x4}	v_{xN}	i_P	i_Z	i_N
2	1	1	0	0	$v_{C1} + v_{C2}$	i_x	0	0
1	0	1	1	0	v_{C2}	0	i_x	0
0	0	0	1	1	0	0	0	i_x

$$\begin{bmatrix} v_{aN} \\ v_{bN} \\ v_{cN} \end{bmatrix} = v_{C1} \begin{bmatrix} s_{a1} \\ s_{b1} \\ s_{c1} \end{bmatrix} + v_{C2} \begin{bmatrix} s_{a2} \\ s_{b2} \\ s_{c2} \end{bmatrix} \quad (8)$$

The relationship of the current of each branch to the three-phase output current is as follows:

$$\begin{bmatrix} i_1 \\ i_2 \\ i_3 \end{bmatrix} = \begin{bmatrix} \mathrm{S_a}[2] & \mathrm{S_a}[2] & \mathrm{S_a}[2] \\ \mathrm{S_b}[1] & \mathrm{S_b}[1] & \mathrm{S_b}[1] \\ \mathrm{S_c}[0] & \mathrm{S_c}[0] & \mathrm{S_c}[0] \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \quad (9)$$

Equation (9) can be rewritten based on the switching signal as (10).

$$\begin{bmatrix} i_1 \\ i_2 \\ i_3 \end{bmatrix} = \begin{bmatrix} s_{a1}s_{a2} & s_{b1}s_{b2} & s_{c1}s_{c2} \\ s_{a2}s_{a3} & s_{b2}s_{b3} & s_{c2}s_{c3} \\ s_{a3}s_{a4} & s_{b3}s_{b4} & s_{c3}s_{c4} \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \quad (10)$$

Refer to Kirchhoff's Current Law, the DC link capacitor can be written as follow:

$$\frac{d}{dt} v_{C1} = \frac{1}{C_1} i_{C1}, \quad \frac{d}{dt} v_{C2} = \frac{1}{C_2} i_{C2} \quad (11)$$

where i_{C1} and i_{C2} can be obtained using (12)

$$\begin{aligned} i_{C1} &= i_{dc} - i_1 \\ i_{C2} &= i_{dc} - i_{C1} - i_2 \end{aligned} \quad (12)$$

The DC i_{dc} can be obtained as follows:

$$i_{dc} = \frac{1}{2R_C} (v_{DC} - v_{C1} - v_{C2}) \quad (13)$$

where R_C is the internal resistance of the capacitor or ESR. Assumed that $C_1 = C_2$, so that $R_{C1} \approx R_{C2} = R_C$.

As shown by equations (8) to (13), it can be seen that the higher the NPC level, the more system output voltage can approach the sine signal. However, the higher the power inverter, the more complex the space vector is generated, for example, 3L has 27 space vectors, as in Fig. 3. There are three numbers of vectors with "Zero" values, twelve numbers for "Low" vectors, six numbers for "Medium" vectors, and six numbers for "High" vectors. The four types of vectors are represented in the alphabet O, L, M, and H. The complexity of the modulation upsurges with the increase of the level of NPC used. The level of complexity is also caused by redundancy in the O and L vectors which can cause the capacitance-voltage unbalanced. The wrong selection of candidate vectors can cause the power inverter not to work correctly.

III. CONVENTIONAL FSMPC

FSMPC is a development algorithm from conventional MPC. In contrast to its predecessors, which utilize optimization processes to obtain control signals, such as quadratic optimization or linear programming, FSMPC uses sequential computation of control signal sets to receive optimal control signals. Therefore, the algorithm is specifically for the control of power electronics devices. Another advantage is that the algorithm does not require linearization if the controlled plant has nonlinear characteristics. Even in the case of power electronics, the system can be modeled as a switching model without converting it into an average model. Of course, this is a breakthrough for control systems, especially in the field of power electronics. Like conventional MPC, FSMPC requires a system model to obtain optimal control signals. Instead, the system's parameters should be identified accurately to avoid mismatches during optimization. Because the algorithm works on discrete time, information regarding the discrete model of the system being controlled is needed.

In this case, the SCIM and 3L-NPC models should be converted into discrete forms. Based on the system model described in section 2, model conversion from continuous to discrete is only required in SCIM models (1), (2), and DC link capacitor voltage models (11). The discrete SCIM model can be represented as state space as in (14). This representation is obtained by using Forward Euler's.

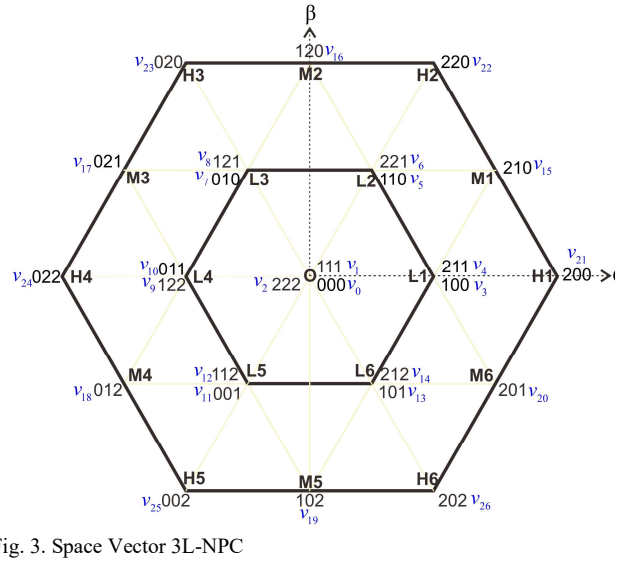


Fig. 3. Space Vector 3L-NPC

$$\hat{x}^{k+1} = \Phi^k x^k + \Gamma_b u^k \tag{14}$$

where x is the estimated state variables with $x = [i_{s\alpha} \quad i_{s\beta} \quad \psi_{s\alpha} \quad \psi_{s\beta}]^T$ and control signal u is defined as vector $u = [v_{s\alpha} \quad v_{s\beta}]^T$. The superscript sign k is the time step with $k = 1,2,3,\ldots$ which corresponds to the sampling time t_s. While the matrixes Φ^k and Γ_b are defined as follows:

$$\Phi^k = \begin{bmatrix} 1-\frac{t_s}{\tau_\sigma} & 0 & \frac{k_r t_s}{\sigma L_s \tau_r} & \frac{k_r \omega_e^k t_s}{\sigma L_s} \\ 0 & 1-\frac{t_s}{\tau_\sigma} & -\frac{k_r \omega_e^k t_s}{\sigma L_s} & \frac{k_r t_s}{\sigma L_s \tau_r} \\ \frac{L_m t_s}{\tau_r} & 0 & 1-\frac{t_s}{\tau_\sigma} & -\omega_e^k t_s \\ 0 & \frac{L_m t_s}{\tau_r} & \omega_e^k t_s & 1-\frac{t_s}{\tau_\sigma} \end{bmatrix} \text{ and}$$

$$\Gamma_b = \begin{bmatrix} \frac{t_s}{\sigma L_s} & 0 \\ 0 & \frac{t_s}{\sigma L_s} \\ 0 & 0 \\ 0 & 0 \end{bmatrix}$$

The DC link capacitor discrete model can be represented in (15).

$$\hat{v}_{C1}^{k+1} = v_{C1}^k + \frac{t_s}{C_1} i_{C1}, \quad \hat{v}_{C2}^{k+1} = v_{C2}^k + \frac{t_s}{C_2} i_{C2} \tag{15}$$

Equation (14) does not include the SCIM mechanical model. It is unnecessary because the control objective, in this case, does not require SCIM mechanical velocity prediction information. The control objective for FSMPC can be represented as a cost function. The control objective is to ensure that the electrical torque and stator flux are close to the reference values. So, we can write a cost function to guarantee this condition in (16).

$$g^k = \lambda_T \left[T_{er}^{k+1} - \hat{T}_e^{k+1}\right]^2 + \lambda_\psi \left[\psi_{sr}^{k+1} - \hat{\psi}_s^{k+1}\right]^2 + \lambda_{dc} [\hat{v}_{C1}^{k+1} - \hat{v}_{C2}^{k+1}]^2 \tag{16}$$

where T_{er}, ψ_{sr} are the electrical torque and stator flux reference, respectively. Meanwhile λ_T, λ_ψ, and λ_{dc} are cost function coefficients. The value of each of these parameters will affect the system's performance. Equation (16) includes the stator flux in the computation. To obtain the importance of these variables can be distinguished by (17). While the estimation of the electrical torque at $k+1$ is determined from equation (18).

$$\hat{\psi}_s^{k+1} = \sqrt{\left[\hat{\psi}_{s\alpha}^{k+1}\right]^2 + \left[\hat{\psi}_{s\beta}^{k+1}\right]^2} \tag{17}$$

$$\hat{T}_e^{k+1} = 1.5 Z_p \left(\hat{\psi}_{s\alpha}^{k+1} \hat{\imath}_{s\beta}^{k+1} - \hat{\psi}_{s\beta}^{k+1} \hat{\imath}_{s\alpha}^{k+1}\right) \tag{18}$$

The stator flux $\alpha\beta$-frame at $k+1$ can be identified by using (19).

$$\begin{aligned} \psi_{s\alpha}^{k+1} &= \sigma L_s i_{s\alpha}^{k+1} + k_r \psi_{r\alpha}^{k+1} \\ \psi_{s\beta}^{k+1} &= \sigma L_s i_{s\beta}^{k+1} + k_r \psi_{r\beta}^{k+1} \end{aligned} \tag{19}$$

Equations (14) to (19) that have been modeled are insufficient to represent the discrete SCIM model. Let's say, we consider (14) as the SCIM model and (8) as the system input voltage. Consequently, there is a mismatch in the input parameters. Equation (8) represents the three-phase voltage in the abc-frame. To be able to use this equation, it is necessary to convert it to $\alpha\beta$-frame, commonly known as the Clarke Transformation as in (20).

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} v_{aN} \\ v_{bN} \\ v_{cN} \end{bmatrix} \tag{20}$$

Defined $\mathbf{S}_{opt}$ as the optimal control signal of the optimization result, the control signal is used directly to activate and deactivate the electrical switch or IGBT on the 3L-NPC. The signal can be generated from **Algorithm 1**.

Algorithm 1: Conventional FSMPC

Measure x^k, ω_m^k v_{C1}^k, and v_{C2}^k;
Obtain reference signals T_{er}^{k+1} and ψ_{sr}^{k+1};
Define **S** as vector voltage candidate matrix using Figure 4;
  for n=1 to 27
    Calculate v_α and v_β using (20);
    Predict the state variables using (14);
    Predict $\alpha\beta$ stator flux using (19);
    Predict the capacitor voltage using (15);
    Predict the torque using (18);
    Predict the amplitude of stator flux using (17);
    Calculate g^k(n);
  end
$g_{opt} = \arg\min(g)$; $\mathbf{S}_{opt} = \mathbf{S}(:, g_{opt})$;

It can be seen that the total computation required to get $\mathbf{S}_{opt}$ is 27 times. These values are all candidate vectors, as shown in Fig. 3. This study reduces the number of candidate voltage vectors to reduce the computational load on the FSMPC. The procedure is described in more details in the next section.

IV. Proposed FSMPC

If we pay attention to **Algorithm 1**, it is known that the computational load on conventional FSMPC lies in the $\mathbf{S}_{opt}$ searching process, where the calculation is carried out 27 times. To reduce the computational load, one way that can be done is to reduce the candidate vector.

In this study, the reduction in the number of candidate vectors was selected based on the g_{opt} value generated by conventional FSMPC. The selection process was divided into three stages, those area) Sector classification in the 3L-NPC vector space, b) reconstruction of candidate vectors, and lastly, c) redesign of FSMPC. The details of each stage are explained in the following sub-section.

A. Sector classification in the 3L-NPC vector space

First, we need to know that the signal $\mathbf{S}_{opt}$ consists of six signals corresponding to (8). Instead, the g_{opt} signal is used

to make observations easier. g_{opt} is not a random signal but a signal with an observable pattern because $g_{opt} \in [0,27]$. To simplify the observation, the space vector in Fig. 3 can be divided into six sectors, as in Table 2.

TABLE II
CLASSIFICATION OF SECTOR AREA

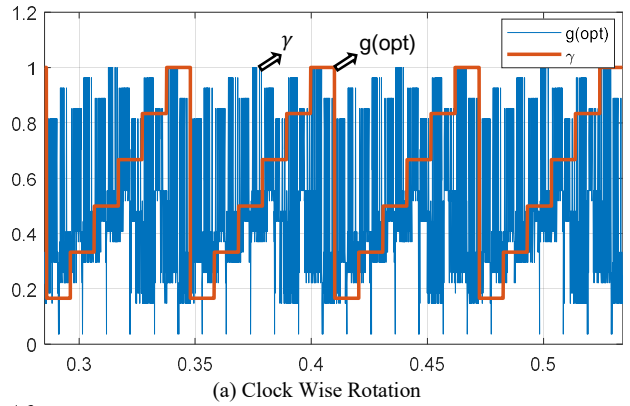
Sector Number	Area of Sector
1	$-\frac{\pi}{6} \le \gamma < \frac{\pi}{6}$
2	$\frac{\pi}{6} \le \gamma < \frac{\pi}{2}$
3	$\frac{\pi}{2} \le \gamma < \frac{5\pi}{6}$
4	$\frac{5\pi}{6} \le \gamma < -\frac{5\pi}{6}$
5	$-\frac{5\pi}{6} \le \gamma < -\frac{\pi}{2}$
6	$-\frac{\pi}{2} \le \gamma < -\frac{\pi}{6}$

where γ can be obtained using (21).

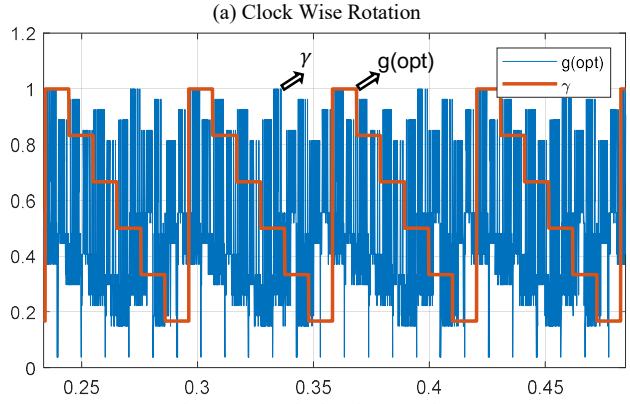
$$\gamma = \tan^{-1}\frac{\psi_{s\beta}}{\psi_{s\alpha}} \tag{21}$$

Based on the six known sectors, the patterned relationship with each of these sectors is shown in Fig. 4. The g_{opt} signal has been converted into per unit form, as well as γ.

The signal generated in Fig. 4 is a simulation result that captures the signal when the system is in a steady state. Under these conditions, the SCIM rotated at speeds of 50rad/s (Fig. 4 a) and -50rad/s (Fig. 4 b). We know that in both CW (Clock Wise) and CCW (Counter Clock Wise) conditions, the γ has a regular pattern in its four cycles. Likewise with g_{opt}, if we look more closely, it can be seen that the parameter also has the same pattern in the four cycles. This shows that the FSMPC optimization result is not a random signal but a patterned signal. The simulation has a duration of 1s, with $t_s = 0.1ms$. So it can be said that the total g_{opt} data obtained is 10001 data.



(a) Clock Wise Rotation



(b) Counter Clock Wise Rotation

Fig. 4. Pattern g_{opt} with γ

Furthermore, g_{opt} is divided into six sectors, and the same data can be eliminated. An example of the g_{opt} distribution in sector 1 is shown in Fig. 5. We can see that when SCIM rotates in CW or CW conditions, not all vectors appear. The data was taken with a simulation time of 1s. with the number of sampling times previously mentioned, the total number of vectors occurring in sector 1 is 1676 times. When the motor rotates CW, the FSMPC output produces 14 vectors, as well as when the CCW condition. This shows that in one sector, not all vectors are needed. Therefore, the unneeded vector can be eliminated from the computational list.

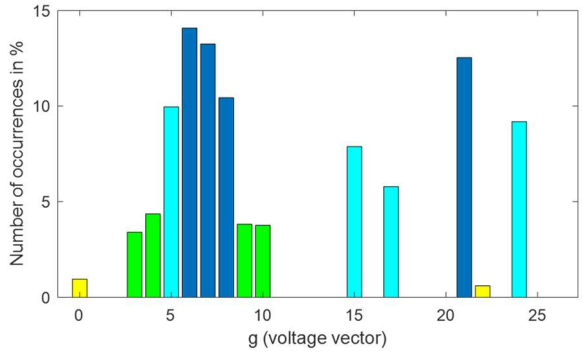
Overall, the occurrence of candidate vectors in each sector is shown in Table 3. The following sub-section describes how to eliminate and select appropriate vectors candidate in each sector.

B. Vector Candidate Reconstruction

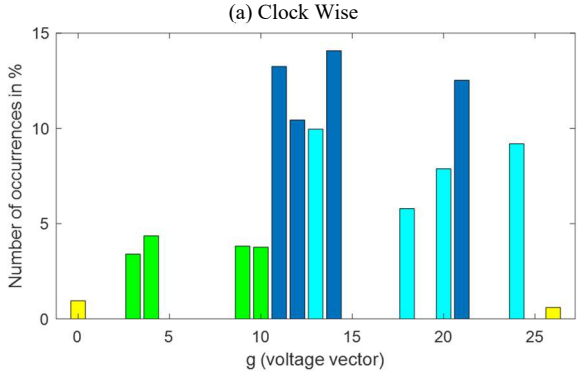
Based on Fig. 5, there is a vector with a tiny percentage of occurrences, less than 1% while some vectors do not appear at all. The vectors reconstruction can be done by reducing small percentage the vectors or by eliminating the vectors which do not appear. Given the number of vectors in each sector is not the same, then to reconstruct the vector can be done as follows:

1. Determine the percentage of each vector that appears in each sector.
2. Eliminate all vectors that do not appear in each sector, starting from the sector with the most vectors and those with vectors with the highest percentage of less than 1%.
3. Equalize the vector length for all sectors by adding a new vector (with zero vectors) or eliminating the vector with the lowest percentage occurrence.

In each sector, there is a reduction in the number of



(a) Clock Wise



(b) Counter Clock Wise (CCW)

Fig. 5. Occurrences Vector Number at Sector 1

vectors. However, this process also adds vectors, especially for sectors 1, 2, and 6. The addition is caused to equalize the length of the vector, which is 15. The results of the reconstruction of the candidate vectors are shown in Table 4.

TABLE III
ORIGINAL VECTOR NUMBER EACH SECTOR

Sector Number	Vectors Candidate
	Clock Wise Condition
1	$v_0, v_3, v_4, v_5, v_6, v_7, v_8, v_9, v_{10}, v_{15}, v_{17}, v_{21}, v_{22}, v_{24}$
2	$v_0, v_5, v_6, v_7, v_8, v_9, v_{10}, v_{11}, v_{12}, v_{16}, v_{18}, v_{22}, v_{23}, v_{25}$
3	$v_0, v_7, v_8, v_9, v_{10}, v_{11}, v_{12}, v_{13}, v_{14}, v_{17}, v_{19}, v_{23}, v_{24}, v_{25}, v_{26}$
4	$v_0, v_3, v_4, v_9, v_{10}, v_{11}, v_{12}, v_{13}, v_{14}, v_{18}, v_{20}, v_{21}, v_{23}, v_{24}, v_{25}, v_{26}$
5	$v_0, v_3, v_4, v_5, v_6, v_{11}, v_{12}, v_{13}, v_{14}, v_{15}, v_{18}, v_{19}, v_{20}, v_{22}, v_{23}, v_{25}, v_{26}$
6	$v_0, v_3, v_4, v_5, v_6, v_7, v_8, v_{13}, v_{14}, v_{16}, v_{20}, v_{23}, v_{26}$
	Counter Clock Wise Condition
1	$v_0, v_3, v_4, v_9, v_{10}, v_{11}, v_{12}, v_{13}, v_{14}, v_{18}, v_{20}, v_{21}, v_{24}, v_{26}$
2	$v_0, v_3, v_4, v_5, v_6, v_{11}, v_{12}, v_{13}, v_{14}, v_{15}, v_{19}, v_{22}, v_{25}$
3	$v_0, v_3, v_4, v_5, v_6, v_7, v_8, v_{13}, v_{14}, v_{15}, v_{16}, v_{17}, v_{20}, v_{22}, v_{23}, v_{25}, v_{26}$
4	$v_0, v_3, v_4, v_5, v_6, v_7, v_8, v_9, v_{10}, v_{15}, v_{17}, v_{21}, v_{22}, v_{23}, v_{24}, v_{25}$
5	$v_0, v_5, v_6, v_7, v_8, v_9, v_{10}, v_{11}, v_{12}, v_{16}, v_{18}, v_{22}, v_{23}, v_{24}, v_{25}$
6	$v_0, v_7, v_8, v_9, v_{10}, v_{11}, v_{12}, v_{13}, v_{14}, v_{17}, v_{19}, v_{23}, v_{25}, v_{26}$

TABLE IV
RECONSTRUCTION VECTOR NUMBER EACH SECTOR

Sector Number	Vectors Candidate
	Clock Wise Condition
1	$v_0, v_1, v_3, v_4, v_5, v_6, v_7, v_8, v_9, v_{10}, v_{15}, v_{17}, v_{21}, v_{22}, v_{24}$
2	$v_0, v_1, v_5, v_6, v_7, v_8, v_9, v_{10}, v_{11}, v_{12}, v_{16}, v_{18}, v_{22}, v_{23}, v_{25}$
3	$v_0, v_7, v_8, v_9, v_{10}, v_{11}, v_{12}, v_{13}, v_{14}, v_{17}, v_{19}, v_{23}, v_{24}, v_{25}, v_{26}$
4	$v_0, v_3, v_4, v_9, v_{10}, v_{11}, v_{12}, v_{13}, v_{14}, v_{18}, v_{20}, v_{21}, v_{23}, v_{25}, v_{26}$
5	$v_0, v_3, v_4, v_5, v_6, v_{11}, v_{12}, v_{13}, v_{14}, v_{15}, v_{19}, v_{22}, v_{23}, v_{25}, v_{26}$
6	$v_0, v_1, v_2, v_3, v_4, v_5, v_6, v_7, v_8, v_{13}, v_{14}, v_{16}, v_{20}, v_{23}, v_{26}$
	Counter Clock Wise Condition
1	$v_0, v_1, v_3, v_4, v_9, v_{10}, v_{11}, v_{12}, v_{13}, v_{14}, v_{18}, v_{20}, v_{21}, v_{24}, v_{26}$
2	$v_0, v_1, v_2, v_3, v_4, v_5, v_6, v_{11}, v_{12}, v_{13}, v_{14}, v_{15}, v_{19}, v_{22}, v_{25}$
3	$v_0, v_3, v_4, v_5, v_6, v_7, v_8, v_{13}, v_{14}, v_{16}, v_{20}, v_{22}, v_{23}, v_{25}, v_{26}$
4	$v_0, v_3, v_4, v_5, v_6, v_7, v_8, v_9, v_{10}, v_{15}, v_{17}, v_{21}, v_{22}, v_{23}, v_{24}$
5	$v_0, v_5, v_6, v_7, v_8, v_9, v_{10}, v_{11}, v_{12}, v_{16}, v_{18}, v_{22}, v_{23}, v_{24}, v_{25}$
6	$v_0, v_1, v_7, v_8, v_9, v_{10}, v_{11}, v_{12}, v_{13}, v_{14}, v_{17}, v_{19}, v_{23}, v_{25}, v_{26}$

In Table 4, it can be seen that the number of candidate vectors was reduced to 15. Implicitly, we can say that it is sufficient to reduce the computational load of FSMPC by 45%. What is more? Reducing the number of candidate vectors refers to each sector, so **Algorithm 1** can no longer be used. The following sub-section will discuss in detail the redesign of the FSMPC.

C. Redesign FSMPC

The primary difference between the proposed FSMPC and conventional FSMPC is the selected candidate vector during the optimization process. In the proposed FSMPC, candidate vectors are selected based on the sector position at time k. To simplify the optimization algorithm due to the addition of the selection procedure, a particular function is designed as in **Algorithm 2**.

Algorithm 2: Sector-based Selection Vector Candidate

function_selection(s_{CWx},s_{CCWx}, ω_{mr}^k, s_c)
  if $\omega_{mr}^k \geq 0$
    switch s_c
      case 1
      S = s_{CW1};
      ⋮
      case 6
      S = s_{CW6};
    end
  elseif $\omega_{mr}^k < 0$
    switch s_c
      case 1
      S = s_{CCWx};
      ⋮
      case 6
      S = s_{CCW6};
    end
  end
return S

Algorithm 3: Proposed FSMPC

Measure x^k, ω_m^k v_{C1}^k, and v_{C2}^k;
Obtain reference signals ω_{mr}^k, T_{er}^{k+1} and ψ_{sr}^{k+1};
S = zeros(3,15);
Obtain sector s_c;
Define s_{CW1}, ..., s_{CW6} and s_{CCW1}, ..., s_{CCW6} as voltage vectors using Table 4;
  for n=1 to 15
    function_selection(s_{CWx},s_{CCWx}, ω_{mr}^k, s_c);
    Calculate v_α and v_β using (20);
    Predict the state variables using (14);
    Predict $\alpha\beta$ stator flux using (19);
    Predict the capacitor voltage using (15);
    Predict the torque using (18);
    Predict the amplitude of stator flux using (17);
    Calculate g^k(n);
  end
$g_{opt} = \arg\min(g)$; $\mathbf{S}_{opt} = \mathbf{S}(:, g_{opt})$;

There is additional information in **Algorithm 2**, namely the rotational speed reference ω_{mr}. The value of these variables is needed to determine the motor in CW or CCW conditions. Based on Table 4, this information is necessary because the candidate vectors on the CW and CCW motors conditions are clearly different. In addition, s_c sector position information is needed to determine which candidate vector to be chosen (between 1 and 6). The use of **Algorithm 2** in the proposed FSMPC is found in Algorithm 3. Similar to conventional FSMPC, the proposed FSMPC algorithm has three main stages, those are measuring state variables, defining candidate vectors, and the process to obtain optimal control signals. In **Algorithm 3**, the definition of vectors in each sector both on the CW or CCW conditions are carried out before or outside the optimization process. It aims to avoid repeated definitions during the optimization process.

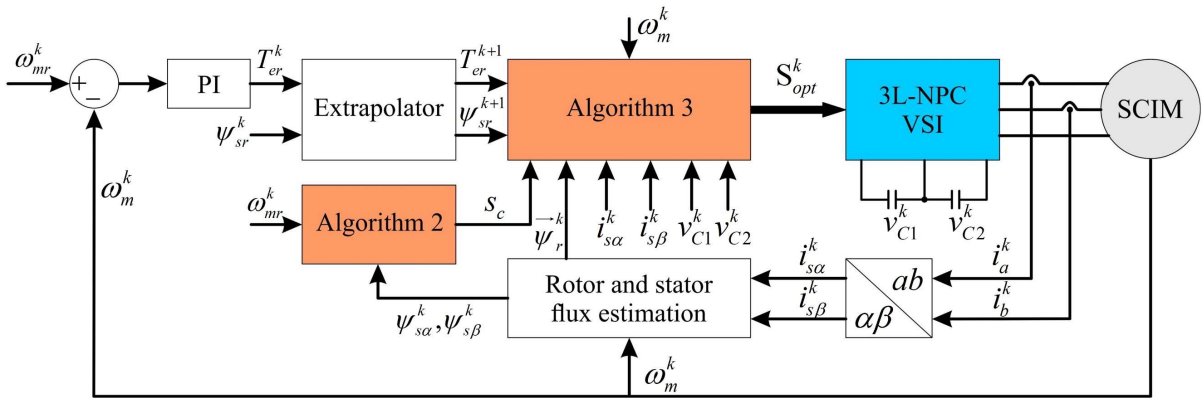


Fig. 6. Proposed System

Overall, the proposed system is shown in Fig. 6.

To produce a complete system, the system is designed to control the speed of SCIM. This study uses discrete PI to ensure the speed produced by SCIM is close to the reference value. With the PI controller, the system has two loops. The first loop, which can be called the inner-loop, is a torque control that utilizes the proposed FSMPC. The second loop that can be called the outer-loop, is used for speed control. In detail, the outer-loop use can be seen in literature [33]. To determine the performance of the system built, more detail on system testing is described in the next section.

V. Result and Discussion

Hardware in the Loop (HIL) is a technology that can be used to verify a control algorithm. System performance verification using HIL has also been utilized in research 1, where there are three microcontrollers each used as a controller, plant and observer [34]. This study utilizes this technology to determine the performance of the proposed FSMPC. In simple terms, the HIL test is shown in Fig. 7.

Generally, to be able to test the system using HIL requires two devices. The first device is used as a plant, while the second is used as a controller. However, in this study, only one device was needed to test the entire system. The plant model and proposed FSMPC are embedded in one microcontroller.

Specifically, the Plant model is embedded in core-1, while the controller algorithm is embedded in core-2. This condition is possible because the microcontroller is a 32-bit TMS320F28379D microcontroller with a dual-core CPU and works with a clock frequency of 200MHz and a total processing of 800MIPS. The two cores exchange data through Inter-Processor Communication (IPC). Core-2 sends data S_{opt} as system input, core-1 receives the data and sends back system state data as feedback. Apart from being a controller, core-2 also sends system responses to the host PC. The data is transmitted via Serial Communication by hand-shacking. Core-2 was chosen for this work because the set point or reference signal is also sent from the PC to the core-2 through communication.

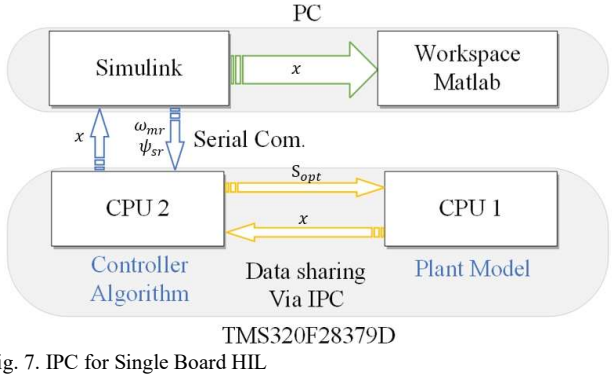


Fig. 7. IPC for Single Board HIL

Four verification schemes are used to claim the performance of the proposed system. The first mechanism is about steady-state performance analysis, the second is speed response capability, the next is the robustness system, and the fourth is computation time analysis. In the following sub-section, we discuss about the steady-state performance system. The SCIM reference parameters are shown in Table 5, while the controller parameters for the conventional FSMPC and the proposed FSMPC, and the PI controller are shown in Table 6.

TABLE V
SCIM Model Reference

Parameter	Value
R_s	11.2Ω
R_r	8.3Ω
L_m	$0.57H$
L_s	$0.6155H$
L_r	$0.638H$
Z_p	2
J_m	$0.00214kg.m^2$
f_d	$0.0041N.m.s$
C_1, C_2	$470\mu F$
V_{dc}	$415V$

TABLE VI
Controller Parameters

Parameter	Value
k_P	0.5
k_I	0.001
λ_T	0.05
λ_ψ	10
λ_{DC}	0.01

A. Steady State Analysis

The steady-state analysis is performed when the motor is rotating at 100rad/s. At that speed, the motor is also given a load of 2N.m to determine the system's performance under non-ideal conditions. The system response is shown in Fig.5. From the top to the bottom is the estimated electrical torque signal, stator flux, current, and DC-link capacitor voltage. The overall response of these parameters shows that the proposed FSMPC produces good performance. The indicator shown from the ripple torque produced is 0.92, with a stator

flux ripple of 0.06. When compared with conventional FSMPC (Fig. 8 (b)), it can be seen that the value of $\Delta\hat{T}_e$ of the proposed system has a slight difference. However, the stator flux ripple value has a much better value, at the figure of 0.06. In addition, the value of THD stator current in steady-state conditions produces a value of 8%. This indicates that the proposed FSMPC has superior performance compared to its predecessor.

From the DC-link capacitor voltage side, we know that $\Delta v_{C(p-p)} \approx 0$ in the proposed FSMPC, where $\Delta v_{C(p-p)} = |(\max(v_{C1}) - \min(v_{C1})) - (\max(v_{C2}) - \min(v_{C2}))|$. While in the conventional FSMPC $\Delta v_{C(p-p)} = 0.012V$. This condition occurs because the average frequency produced by conventional FSMPC is less than the average frequency of the proposed FSMPC. More details regarding this are explained in sub-section D about computation time.

B. Speed Response Capability

Speed response investigation is carried out when the motor is given a reference speed input $\omega_{mr} = 50\text{rad/s}$ while $t < 0.5\text{s}$ and $\omega_{mr} = -50\text{rad/s}$ while $t \geq 0.5\text{s}$. It can be seen that the proposed FSMPC and conventional FSMPC produced a fairly good response, as shown in Fig. 9. Under such extreme changing conditions, the system can adjust less than the indicated 0.05s of each system parameter. Such condition can also be achieved since the system is at a without load state. Based on the electrical torque estimation, it can be seen that the ripple torque for the proposed FSMPC is more than the conventional FSMPC. Interestingly, the response of the estimated stator flux in conventional FSMPC does not seem to change when there is a change in speed. As in the validation, when the steady state condition, the stator flux, stator current, and DC-link capacitor voltage response on the proposed FSMPC produces better than conventional FSMPC. As for the system responses when $t < 0.5\text{s}$ and $t \geq 0.5\text{s}$ produce $\Delta\hat{T}_e$, $\Delta\psi_s$, THD, and $\Delta v_{C(p-p)}$ which is not much different from the steady state conditions for both systems.

C. Robustness Investigation

At this stage, the system is tested with a constant load of 3.5Nm when rotating at a speed of 100rad/s. The system runs for 1s with a load of 0Nm when $0.5 \leq t$, and is loaded when $t < 0.5$. Based on Fig. 10, it can be noticed that both systems can maintain speed with a fairly good response. The electric torque response in the proposed approach produces a more significant torque ripple than conventional systems. However, the stator current in the proposed method has a smaller THD than conventional systems. This phenomenon can be said to be consistent in steady state and speed response tests. Interestingly, the proposed approach produces a faster response in the face of interference, especially load torque. This can be seen from the change in speed when given the load on the proposed system can more quickly (less than 0.05s) restore the motor speed according to the reference compared to the conventional FSMPC.

D. Computational Time Analysis

When designing an FSMC algorithm, one of the main factors is the overall computational time required to obtain the optimal signal. If the computation time required is longer than the sampling time, the system will produce a delay,

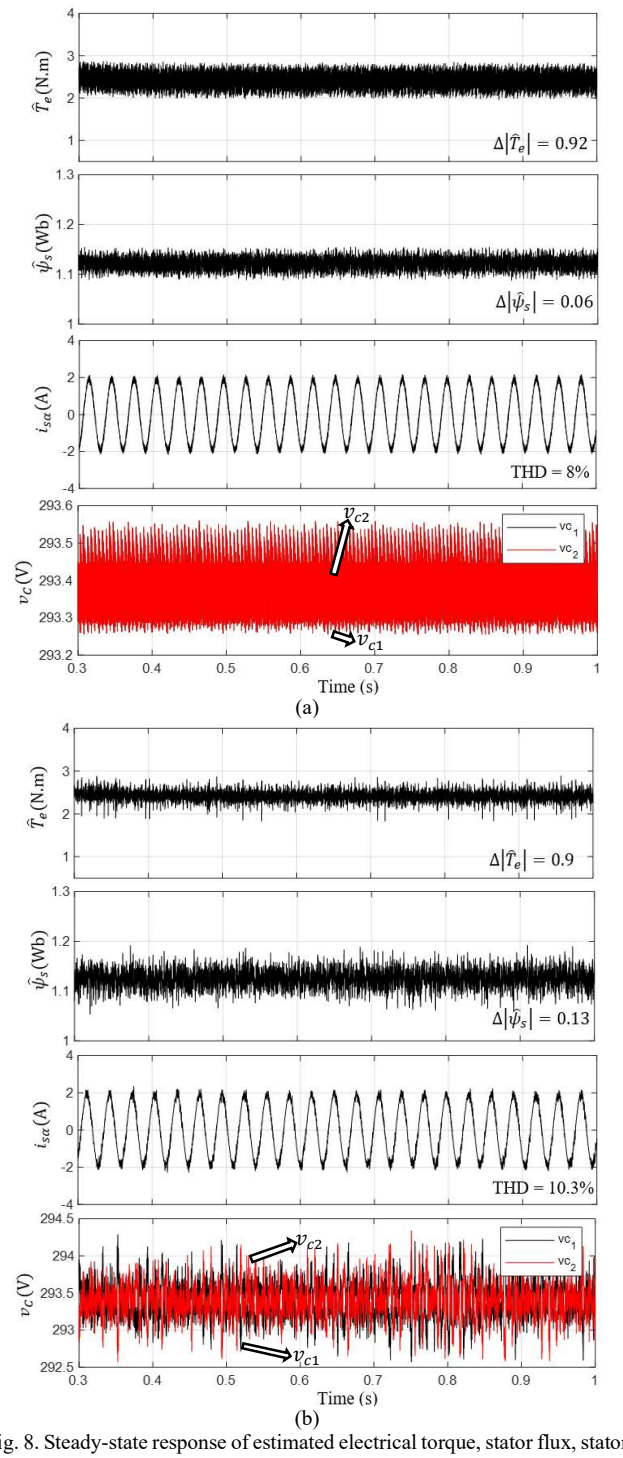


Fig. 8. Steady-state response of estimated electrical torque, stator flux, stator current, and DC-link capacitor voltage (form top to bottom). (a) Proposed FSMPC and (b) Conventional FSMPC

resulting in the stator current's THD value. This study utilizes HIL technology to test the proposed algorithm's effectiveness. By eliminating the length of time for data retrieval from the current sensor and SCIM speed, the data on the comparison of the length of the computational time between the proposed FSMPC and conventional FSMPC is shown in Table 7. When referring to the time sampling value used in the two algorithms, both conventional and proposed algorithms produce a time computing exceeding 100µs. This shows that the average PWM frequency generated by the two algorithms is strongly influenced by the length of the computation time. This is also related to the THD produced by both algorithms of more than 5%. Nevertheless, the

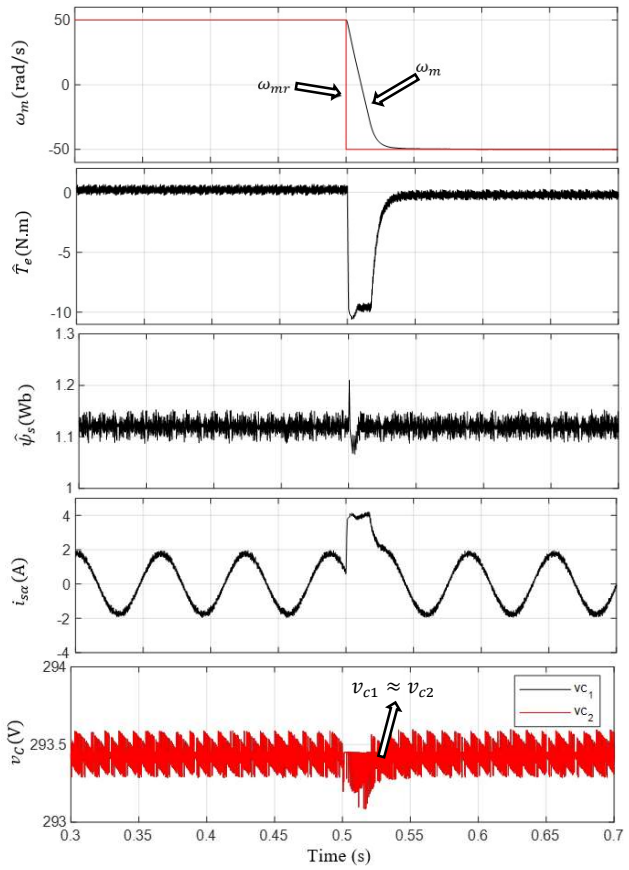


Fig. 9. Speed response capability when the rotational speed reference significantly change. (a) Proposed FSMPC and (b) Conventional FSMPC

proposed FSMPC dominates in terms of speed of computing time, which can reduce the computational load by more than 43% despite the addition of sector selection. This condition also affects the THD and robustness of the system, which is better than conventional algorithms.

TABLE VII
EXECUTION TIME COMPARISON

Index	Execution Time (μs)	
	Conventional FSMPC	Proposed FSMPC
Rotor flux estimation	0.7	0.7
Sector selection	0	5.6 (14)
Prediction and optimization	1941.3	1091.7
Total	1942	1098

VI. CONCLUSION

This paper proposes a new mechanism to reduce the computational load on the FSMPC. The reduction is made by reducing the number of candidate vectors. The effectiveness of the proposed algorithm is validated by utilizing single-board HIL technology. The system being tested is SCIM speed control with 3L-NPC. Four validations are carried out: steady-state analysis, speed response capability, robustness investigation, and computation time analysis. Based on the test results, it can be seen that the proposed FSMPC can maintain positive performance from the conventional algorithm. This is indicated by the state responses, which are not much different from conventional algorithms.

Moreover, the proposed stator current THD algorithm produces a better value. The superiority is also known from the speed response when loaded. Another improvement is that the proposed algorithm can significantly reduce the computational load by more than 43%.

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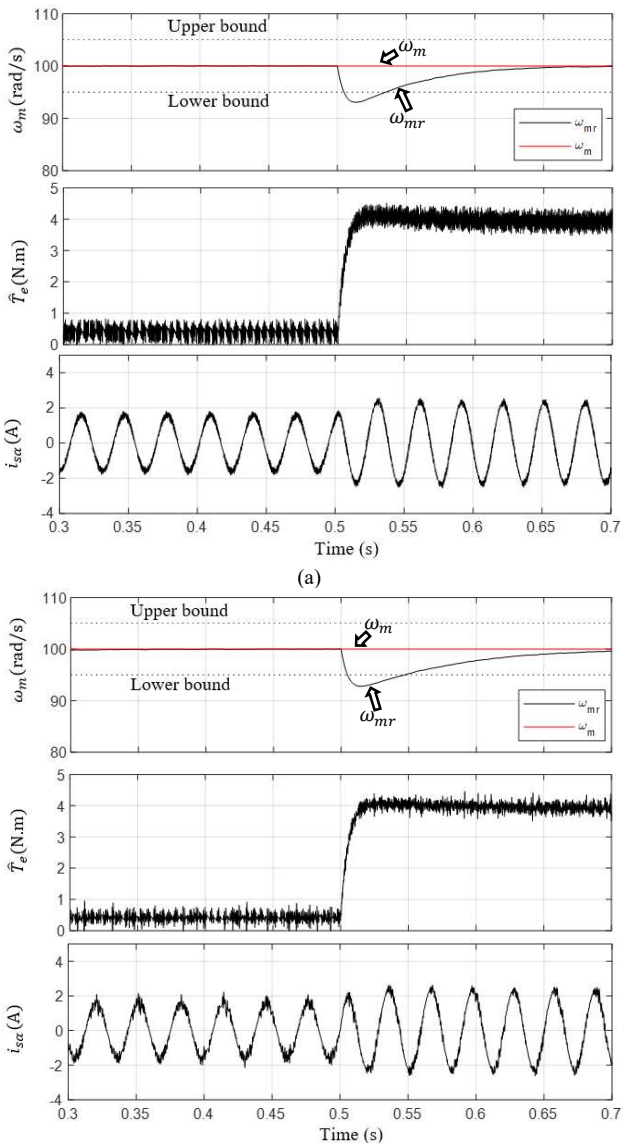

Fig. 10. Robustness system based on the response of rotational speed, electrical torque andstator current. (a) Proposed FSMPC and (b) Conventional FSMPC