A Forward Error Correcting System for Wireless E1 ATM Links

Sasirekha GVK, Gangaraju KM

***Abstract*— Asynchronous Transfer Mode (ATM) is a technology designed for wired media where the BER is of the order 1 in 10^8 or better. When ATM is used over wireless links where the order of errors is 1 in 1000, the performance degrades. In order to maintain the performance it is required to utilize a Forward Error Correcting (FEC) scheme. This paper describes an FEC system called "Link Performance Enhancer (LPE)" consisting of RS encoder/Decoder along with block synchronization scheme. The BER is improved from 1 in 10^3 to 1 in 10^8. At its input LPE has been designed to accept the E1 data as per G.703 & G.704 standards while at the output the interface to the radio is as per G.703. Reed Solomon (RS) Forward Error Correction scheme of (n, k) of (255, 235) coupled with a novel block synchronization scheme for successful decoding, ensures performance improvement from $1/10^3$ to $1/10^8$ with a probability of false alarm of 1 in 10 days, probability of detection 0.9999.. and minimal overhead.**

***Index Terms*—Asynchronous Transfer Mode (ATM), Forward Error Correction (FEC), Link Performance Enhancer (LPE), Bit Error Rate (BER)**

I. INTRODUCTION

ATM was originally designed for fiber-optic transmission links, where the Bit Error Rate (BER) is 1 in 10^8 or better. Availability of better links pushed the requirement for error detection and flow control to the upper layers, thereby making ATM switching faster. This assumption no longer holds true when ATM switches are used in wireless environment, where the wire links have a typical BER of 1 in 1000. The performance of ATM thus degrades. In order to improve the BER from 1 in 1000 to 1 in 10^8 or better an error control mechanism is required. The "Link Performance Enhancer (LPE)" is a system designed to cater for this requirement.

In this paper we describe the design of an FEC system, LPE, built using FPGAs. LPE allows the usage of commercial ATM switches in wireless environments. It incorporates an RS Encoder/Decoder and a robust block synchronization scheme that achieves a BER improvement from 10^{-3} to 10^{-8} with minimal overhead. LPE provides efficient bandwidth utilization, improves link quality and increases application throughput over noisy wireless links. Fiber-like quality with improved bandwidth utilization is achieved through the use of Reed-Solomon (RS) based forward error correction (FEC) and robust block synchronization mechanism. The system corrects burst errors found in such links, thus providing a BER of 10^{-8} and better. The described LPE works transparently in an existing communication link and therefore can be seamlessly integrated to a communication network. It does not require any changes to end user equipment or protocols. Figure 1 shows the typical usage scenario of the proposed LPE.

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The system is designed as a System On Programmable Chip (SOPC) wherein the complete logic for cell level processing is implemented in a single Field Programmable Gate Array (FPGA). The system supports E1-ATM interfaces (G.703, G.704, and G.804) to the ATM switch. Connectivity to Radio equipment is achieved using a 'raw' E1 (unstructured mode) interface. LPE thereby enables interconnection of standard ATM equipment over 2048 Kbps wireless links. Under adverse link conditions, the LPE supports throughput of ATM cells at sustained rate, up to 98 percent of E1 link bandwidth.

LPE has the switch side interface where the BER is always 10^{-8} or better as long as the media side BER is 10^{-3} or better, as shown in Figure 1.

Some of the prior work in this regard can be found in [1] to [4]. In [1] authors describe error protection for ATM-based wireless networking systems using Rate Compatible Punctured Code (RCPC). [2] discusses protocol aided concatenated forward error control for wireless ATM using RS encoding/decoding at ATM Adaptation Layer (AAL). [3] describes a Reed-Solomon encoder/decoder ASIC for wireless ATM. [4] describes an error control scheme for tactical ATM which is applied at ATM layer. Though [4] describes implementation at AAL level, it involves complicated processing requiring segmentation & reassembly, common part convergence sub layer, service specific convergence sub layers for AAL1, AAL2, AAL5 etc. Implementation at ATM layer would allow a choice of FEC for payload only, header only, header + payload options. However, for multimedia applications the preferred choice would be to error protect both header and payload. Our objective is to propose a physical layer implementation in which the ATM cells are concatenated into data blocks for the encoding. This results in a simplified scheme.

Towards this objective, we present a "Link Performance

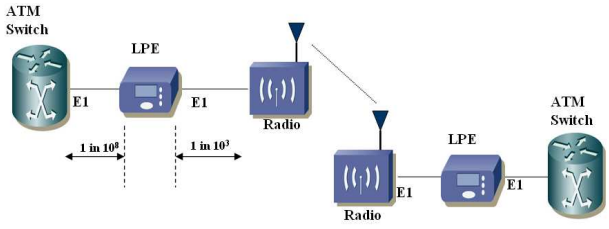

Figure 1: Usage scenario of the proposed LPE

Enhancer" including block synchronization scheme for E1 ATM links with 1 in 10 day probability of false alarm and 0.9999.. probability of detection with minimal bandwidth overhead.

The organization of this paper is as follows. Section II gives the system design details. Section III describes the system architecture along with its sub-blocks. Section IV presents the implementation details. Testing and results are discussed in section V. Finally, our conclusions are presented in section VI.

II. SYSTEM REQUIREMENTS AND DESIGN DETAILS

The LPE is required to improve the Bit Error Rate (BER) from 10^{-3} to 10^{-8} or better. The selected error correction code characterizes this performance improvement. The graph (Figure 2) shows the input error rate to output error rate improvement for various redundancy values. The symbol size is 8 bits and the block size is 255 symbols. After the study it was seen that the Reed Solomon (255,235) would be the optimal forward error control coding scheme for the LPE. This code has the advantages of BER improvement from 1 in 1000 to 1 in 10^8, minimal overhead (7%) and Intellectual Property (IP) core for FPGAs availability.

A mechanism is needed for identification of block boundaries. For this we propose a unique synchronization pattern to be prefixed to each block before transmitting. The receiver logic can hunt for this pattern and find the block boundaries. This is described in detail in Section II A.

A. Block Synchronization design issues

The design of the synchronization involves the addressing twin issues. They are:

(a) Selection of the length of unique word

(b) Selection of frequency of transmission of unique word

Table I indicates the probability of detection P_d for different unique word lengths n in bits. The entries in the Table I are generated using the formula given below

$$P_d = \sum_{i=0}^{t} {}^{i}C_{48}\, P_e^{\,i}(1-P_e)^{48-i}$$

Where t is the error tolerance threshold and P_e is the probability of error of the channel.

P_d for BER of 1 in 10^2 and for $t = 0$

$$P_d = (1-P_e)^{48} = (1-.01)^{48} = 0.61729014$$

While for a $t = 1$:

$$P_d = 48\, P_e\, (1-P_e)^{47} + 0.61729014$$

It can be observed that the probability of missing sync is = (1 - 0.9999914) = 0.0000086 = 8.6 x 10^{-6} or 1 in 116279.

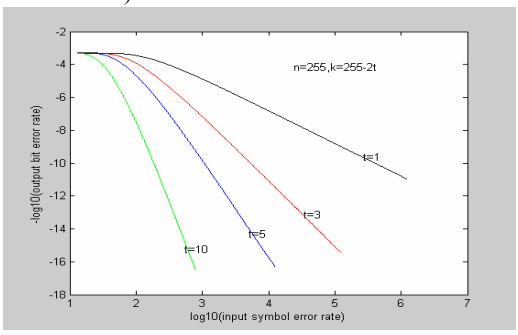

Figure 2: Input symbol error rate Vs. output BER for RS codes[5]

B. Calculation of probability of occurrence of false alarm

The Probability of False alarm P_f can be calculated using the formula

$$P_f = \frac{1}{2^n} \sum_{i=0}^{t} {}^{i}C_n$$

Table II shows the probability of false alarm. Further, Let T = 488.28 * 10^(-9) *i.e.* E1 data rate N = 255*8*6; i.e. one sync word sent for every 6 encoded blocks where each encoded block is 255 bytes *i.e.* 255 x 8 bits.

$$x = 1/P_f$$

$$D = ((T*N)x)/(24*60*60)$$

where D is the no. of days within which 1 false alarm can occur. Therefore, for the chosen unique word length of 48 bits and the frequency of transmission of once for every 6 blocks of 255 bytes, D is 10 days .Table III shows the number of days per false alarm.

C. Bandwidth Analysis

This sub section describes the analytical study carried out for the design. This include the bandwidth analysis to find out the required amount of idle cells that need to be dropped to account for the extra redundancy added, study and selection of suitable error correcting code and performance analysis. The selected code is RS (255,235) and the block synchronization pattern of 48 bits (6 bytes) is added for every 6 blocks of encoded data. The extra bandwidth required for the redundancy added by the encoder and block synchroniza-

Table I: Probability of Detection

t	n=32	n=48	n=64
0	0.72498033	0.61729014	0.52559648
1	0.95931741	0.91658233	0.86537603
2	0.99600655	0.98762643	0.97348770
3	0.99971252	0.99862990	0.99605647
4	0.99998392	0.99988029	0.99953297
5	0.99999927	**0.99999144**	0.99995437

Table II: Probability of false alarm

t	n=32	n=48	n=64
0	2.3283e-010	3.5527e-015	5.4210e-020
1	7.6834e-009	1.74082970e-013	3.5236e-018
2	1.2316e-007	4.18154399e-012	1.1281e-016
3	1.2780e-006	6.56292797e-011	2.3714e-015
4	9.6505e-006	7.56916307e-010	3.6815e-014
5	5.6537e-005	6.84024215e-009	4.5014e-013

Table III: Frequency of occurrence of false alarm in days

t	n=32	n=48	n=64
1	9.0029	3.9736e+005	1.9631e+010
2	0.5616	1.6542e+004	6.1317e+008
3	0.0541	1.0540e+003	2.9169e+007
4	0.0072	91.3879	1.8789e+006
5	0.0013	**10.1127**	1.5367e+005

tion is obtained by dropping the frame sync and signaling information from the frame. E1 frame format is shown in Figure 5. Further bandwidth can be obtained by dropping the idle cells from the incoming stream. The ATM switch generates idle cells when there is no user data. This is to prevent the loss of synchronization of ATM cells for 'cell delineation' at other end ATM switch. This process of cell delineation is explained in section III B. Lack of user data in the idle cells allows us to drop them to cater for the required bandwidth at the encoder side. The required rate of idle cells is then inserted after the decoding at the receiver side to prevent loss of physical layer synchronization, resulting in loss of cell delineation at the switch end.

The minimum rate of idle cells required for the correct operation of the device is calculated as follows:

Let 'x' denote the rate of arrival of idle cells from the switch and'd' be rate of arrival of valid data. The total rate at the output of the framer is 1920kbps (since each timeslot carries 64kbps, 30 timeslots will take 30*64=1920kbps)

$$i.e.\ d + x = 1920 \qquad (1)$$

Some of the idle cells have to be dropped in order to accommodate for the overhead added by the encoder. Rest of the idle cells can be allowed to pass through and is encoded along with the data. Let 'x1' denote the rate of idle cells that pass through and 'x2' denote the rate of the idle cells that are dropped.

$$x1 + x2 = x \qquad (2)$$

$$d + x1 + x2 = 1920 \qquad (3)$$

The encoder receives data at a rate equal to'd+ x1' since some of the idle cells are dropped (of rate = x2)
Thus rate at encoder is

$$d + x1 = 1920 - x2 \qquad (4)$$

The encoder adds an overhead of 21 bytes (average over 6 blocks) for every 235 bytes it receives (20 bytes of FEC overhead + 1 byte of sync word overhead)

Thus the rate at the output of the encoder + sync block will be,

$$\text{input rate} + (\text{input rate})*21/235$$

$$= (1920 - x2) + (1920 - x2)*21/235$$

Since the output rate of the interface is 2048kbps (64*32time slots), equating the above expression to 2048 and solving for x2 will give the rate at which idle cells have to be dropped.

$$i.e.\ \ (1920 - x2) + (1920 - x2)*21/235 = 2048 \text{ kbps}$$

$$\Rightarrow x2 = 40 \text{ kbps}$$

As a ratio this rate w.r.t E1 data rate can be expressed as 40/2048 which is approximately 1/50. *i.e.* for every 50 ATM cells we assume an occurrence of idle cell on an average. This average rate of occurrence of idle cell will ensure that there is no overhead because of FEC and block synchronization.

Another approach for the bandwidth analysis is described in this paragraph. The E1 frame format has 30 data slots + 1 frame sync slot + 1 signaling slot. The frame sync information is not required over the wireless link as block sync provides the necessary data boundaries. It is required by the receive E1 switch interface where it can be reinserted. Signaling in E1 ATM is in the form of AAL5 Protocol Data Units carried as ATM cells. Therefore, a payload reduction of 2 bytes is achieved for every 32 bytes. For every 6 consecutive blocks, 6 bytes of block synchronization pattern is inserted. The no. of bytes gained for every six blocks by dropping slot 0 and slot 16 *i.e.* E1 frame sync slot is 94 bytes (there are about 47 frames in 6 blocks). As mentioned earlier, the RS encoding scheme of (255, 235) requires an overhead of 20 bytes for every 235 bytes of data. If we transmit block sync pattern of 6 bytes for every 6 blocks, the total overhead would be 20x 6 + 6 *i.e.* 126 bytes for 6 blocks. Therefore, the mechanism can do the BER improvement with overhead of 32 bytes per 6 blocks. To combat this overhead of about 2%, one idle cell needs to be removed before transmission out of every 50 cells (on an average).

III. Description of the System Architecture

The Figure 4 shows the internal blocks of the proposed LPE. In the forward path, the E1 frames from an ATM switch received by the switch interfaces are de-multiplexed after the detection of the frame sync slot. The data from the 30 user slots of E1 frame is collected. The collected data is then encoded by a RS-encoder (255,235) to form 255 byte blocks. For every 6 consecutive blocks, 6 bytes of block synchronization information is inserted. The data is then sent to media interface for onward transmission. In the receive path, block boundaries are identified by the Sync Detect logic. Sync Detect logic gives the required block alignment marker. The aligned block of data is then decoded. This data is then transmitted via switch interface. The design details of the block synchronization mechanism were presented section II. The Physical Media Dependent (PMD) functions and E1 frame handling functions are taken care in the interface block of Figure 4. The interfaces, switch and media, consist of E1 Line Interface Units and Transmit and Receive Framers. The details of each of these blocks are explained in the following subsections.

A. Switch interface

The functions of the switch interface block are to transmit and receive the E1 frames to/from the ATM switch. On the receive side the HDB3 data is converted to TTL and clock is recovered. The frame boundary is identified and a frame marker signal is generated. The data aligned with the frame marker is sent for further processing. On the transmit side the buffered data is packed into E1 frames, converted to HDB3 and then sent to the switch. Figure 5 shows the E1 frame format.

B. Cell delineator

The removal of idle cells involves finding the cell boundaries and then checking the header information. "Cell Delineation" is the process that allows identification of cell

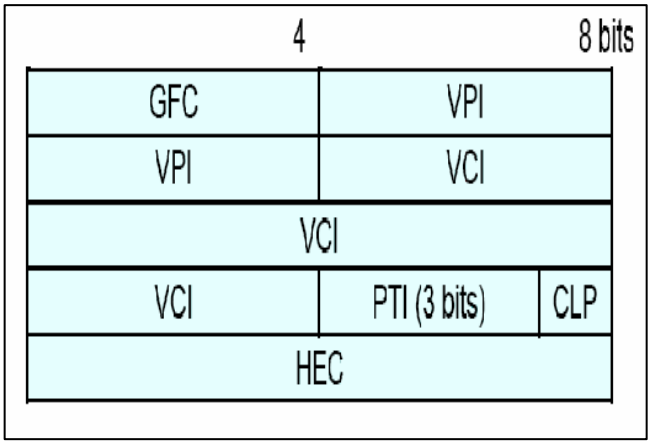

Figure 3: ATM Cell Header Format

boundaries from data received at an interface to a channel. (for details refer [13]-[17]). Traditionally, framing of packets in digital transmission technologies employ a 'framing word' which is a unique synchronization sequence located at a specific point within a packet that can be used to indicate the frame boundary. Since ATM uses relatively small packet size, 53 bytes, compared with other transmission technologies, employing a 'framing word' would prove to be costly. Instead, ATM makes use of the HEC byte, which has a dual purpose by also providing single-bit error correction and multi-bit error detection over the header bits. This eliminates the requirement for a specific 'Frame word'. ATM cell header format is shown in Figure 3. ATM cells may be carried in two formats (Figure 23 & [9]):

- As a continuous stream of cells in a cell-based format (Cell-based Physical Layer)
- As cells carried within a SDH (Synchronous Digital Hierarchy)-based frame structure (SDH-based Physical

1) Serial Cell Delineation Algorithms

Serial algorithms are generally associated with cell-based format since SDH-based frame structures provide knowledge of byte-boundaries of contained cells allowing the use of octet-parallel algorithms. Cell delineation algorithms utilize the correct HEC byte of an uncorrupted cell for boundary detection and operate as follows: The receiver initially operates in the HUNT state and searches for a valid header. (see Figure 6). Since byte-boundaries are unknown, this occurs on a bit-by-bit basis over the previous 40-bits. Upon detecting a valid HEC the receiver enters the PRESYNC state and cell delineation is performed every 53 bytes (cell-by-cell). This process continues until the HEC has been consecutively confirmed δ times, at which point the receiver enters the SYNC state. If an incorrect HEC is found while operating in PRESYNC, the process returns to HUNT. While in the SYNC state, if an incorrect HEC is consecutively obtained α times cell delineation is lost. Recommended values for these parameters are, $\alpha = 7$ and $\delta=8$.

2) Octet-Parallel Cell Delineation Algorithms

SDH-based frame structure enables the utilization of possibly pre-existing transmission equipment by allowing ATM cells to be carried in the payload portion of an SDH STM-1 frame. This provides knowledge of byte-boundaries of contained cells and enables cell delineation to take place on a byte-by-byte rather than bit-by-bit basis. With today's high-speed transmission links, performing cell delineation on a bit-serial basis might prove to be too much of a bottleneck. The data rates required are becoming too fast for clock frequencies to keep up if processed serially, thus alternative architectures must be considered. Generally this is achieved through parallelism, processing 8 bits, 16 bits or even 32 bits at a time. This can significantly increase the data processing rate with only a minimal increase in hardware complexity; however this can only be achieved if knowledge of byte-boundaries is available. The parallel approach to speed up the CRC algorithm is to perform a number of operations in a single clock cycle.

As indicated in ITU-T recommendation 1.432.1[10], the HEC byte in the cell header is an 8-bit Cyclic Redundancy Check (CRC) based on a generator polynomial $G(x) = x^8+x^2+x+1$. Before transmitting a packet, the transmitter must calculate an appropriate code word for insertion into the HEC field. The code word is the remainder of the product of $x^8 * A(x)$ (the polynomial representing the first four octets in the cell header), divided by (modulo-2) the generator polynomial, $G(x)$. $x^8A(x) = D(x)G(x)+H(x)$. $D(x)$ is the dividend and $H(x)$ is the remainder. The ATM Cell delineation is illustrated in the Figure 6 and its implementation is shown in Figure 7. In the HUNT state, the cell delineation is performed by checking bit-by-bit for the correct HEC (i.e. syndrome equals zero) for the assumed header field. This checking can be performed byte-by-byte if the byte-boundaries are available.

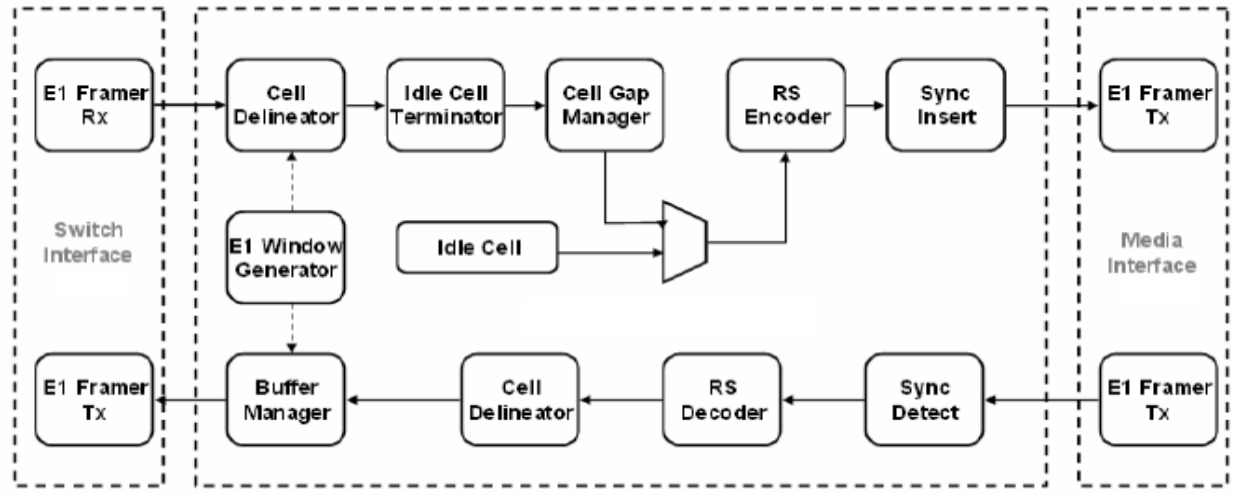

Figure 4: Block diagram of LPE

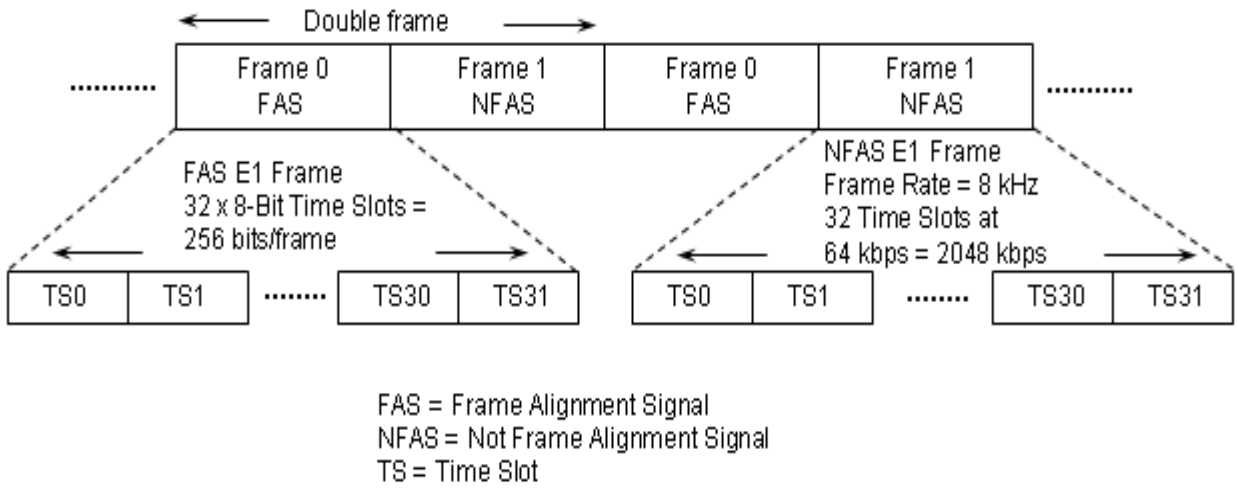

Figure 5: E1 frame format [8]

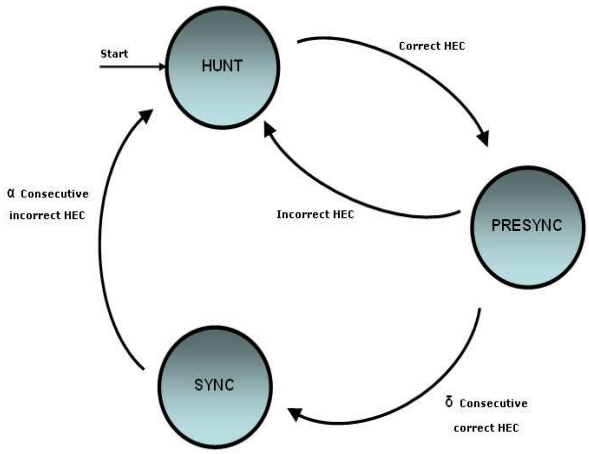

Figure 6: Cell Delineation State diagram

In the PRESYNC state, the cell delineation process is performed by checking cell-by-cell for the correct HEC. (Figure 6). This process continues until the HEC has been consecutively confirmed δ times, at which point the receiver enters the SYNC state. If an incorrect HEC is found while in the PRESYNC state, the process returns to the HUNT state.

While in SYNC state, if an incorrect HEC is consecutively obtained α times, synchronization is declared lost. The parameters α and δ are chosen to make the cell delineation process as robust and secure as possible while satisfying the performance criteria. Robustness against false indications of misalignments due to bit errors in the channel depends on α, while robustness against false delineation in resynchronization process depends on δ. For cell-based formats it is recommended that α=7 and δ=8, while for SDH-based frame structures, it is recommended that α =7 and δ =6. The value of α has been chosen to achieve a probability of false delineation better than 10^{-14}, independent of bit-errors in the channel.

Hunt Engine (Figure 8): The heart of the Hunt Engine is a Moving Window CRC detector. The detector circuit is based on Linear Feedback Shift Register (LFSR) with memory and logic to negate the effects created by previous bits. An optional Coset polynomial processing is also provided. The syndrome generated by the CRC logic is compared with standard values – 85 if coset is enabled, 0 if not. Pulse filter logic is also incorporated to prevent false positives when the data is all zeros. The Hunt Engine is always on, since the other state engines use its output.

Pre-sync engine (Figure 9): pre-sync engine takes the output of Hunt Engine and checks for false matches. It checks for delta consecutive matches with predetermined time periods. The number of matches to look for can be configured. Once a valid match is found the control logic is informed and the state machine gives control to the Sync engine. If a valid match is not found the state machine resets the engine.

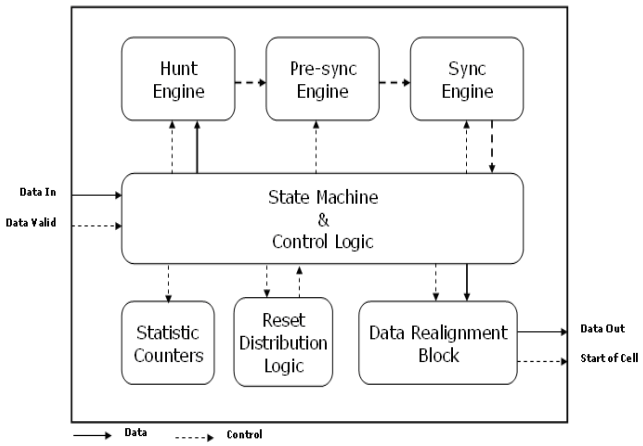

Figure 7: Cell Delineator Block Diagram

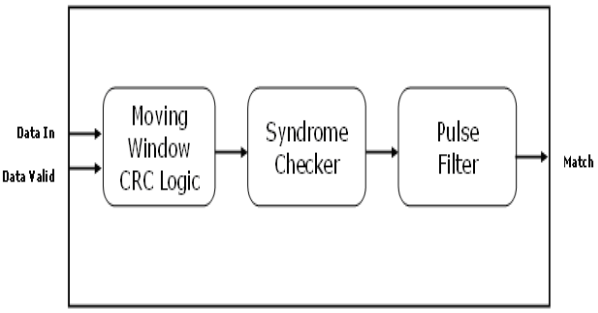

Figure 8: Hunt Engine

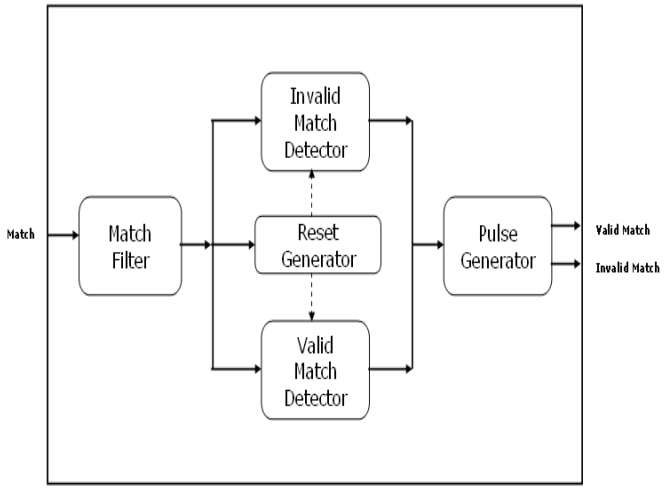

Figure 9: Pre-sync engine

Sync Engine: It is enabled by the state machine once the Pre-sync engine detects a valid match. In the Sync state the cell delineation will be assumed to be lost if an incorrect HEC is obtained alpha times consecutively. The value of alpha can be configured.

C. Idle cell terminator

Idle cell terminator logic shown in Figure 10, is used to detect and discard all idle cells from the incoming stream. Contents of an idle cell are depicted in Figure 11. The termination of idle cells is to cater for the extra redundancy required by the Reed-Solomon encoder. It uses the cell delineator's output to extract the header from the incoming ATM cells. After identifying the header, idle cells are identified by the standardised pattern for the cell header shown in Figure 11. Since match result is obtained after the cell start, the data need to be realigned before giving the output. Data is delayed by the required value, so that it realigns with the Start-of-Cell. The Data Realignment block also generates continuous Start-of-Cell when the state machine is in the SYNC state. This prevents re-synchronisations in the presence of single bit errors while the number of incorrect matches is below the threshold value of α .

D. Cell gap manager

The cell gap manager consists of Cell FIFO and the related control logic. It stores the ATM cells containing data in the FIFO. The ATM data cells and idle cells are then multiplexed in such a way that there are no un-necessary cell gaps formed because of the termination of idle cells. This gives the ATM cells concatenated to form blocks of 235 bytes required by the RS encoder.

E. RS Encoder/Decoder

Reed-Solomon (RS) codes are *non-binary cyclic* codes with symbols made up of *m*-bit sequences, where *m* is any positive integer having a value greater than 2. RS (*n*, *k*) codes on *m*-bit symbols exist for all *n* and *k* for which

$$0 < k < n < 2m + 2$$

where *k* is the number of data symbols being encoded, and *n* is the total number of code symbols in the encoded block (refer [5], [6] for details). For the most conventional RS (*n*, *k*) code,

$$(n,k) = (2^m - 1,\ 2^m - 1 - 2t)$$

where *t* is the symbol-error correcting capability of the code and $n - k = 2t$ is the number of parity symbols. The code is capable of correcting any combination of *t* or fewer errors, where *t* can be expressed as:

$$t = \left\lfloor \frac{d_{\min} - 1}{2} \right\rfloor = \left\lfloor \frac{n - k}{2} \right\rfloor$$

The above equation illustrates that for the case of R-S codes, correcting *t* symbol errors requires no more than 2*t* parity symbols.The RS decoded symbol-error probability, P_E, in terms of the channel symbol-error probability, *p*, can be written as follows

$$P_E \approx \frac{1}{2^m - 1} \sum_{j=t+1}^{2^m - 1} j \binom{2^m - 1}{j} p^j (1-p)^{2^{m-1-j}}$$

where *t* is the symbol-error correcting capability of the code, and the symbols are made up of *m* bits each [5].

The RS encoder/decoder chosen is of n=255 bytes and k = 235 bytes. The data from the ATM cell FIFO is read as chunks of 235 bytes. These 235 bytes are encoded to 255 byte block. RS decoder takes in block aligned data of 255 bytes and decodes to data of 235 bytes.

F. Sync insert /detect

The encoded blocks are multiplexed by a 48 bit (6 byte) block synchronization pattern, one pattern for every 6 blocks. This pattern is detected by a correlator with an error threshold of 5 (t). The sync detect logic output generates a block marker signal used by the RS decoder to mark the block boundaries.

G. Media interface

The media interface block converts the RS encoded and block synchronization data to E1 data stream. In the received E1 data stream the clock is recovered and data is converted from HDB3 to TTL. The re-timed data is used for further processing.

IV. IMPLEMENATION DETATILS

The proposed LPE was implemented using a System On Programmable Chip approach on an Altera Cyclone II device. The RS encoder/decoder '*megafunction*' was an intellectual property of ALTERA. This has an advantage of quick prototyping, flexibility to make it adaptive, and also facilitates easy translation to a structured ASIC. The diagram (Figure 12) shows the design flow adopted for the design.

The design was captured using Altera Quartus II development software. The tool provided a complete design environment for System-On-a-Programmable-Chip (SOPC) design. The design was then synthesized to generate a gate-level netlist. This netlist was then mapped to the particular technology used in the selected device. Then the design is routed and placed and a floor plan is created. This performed is such a way that the timing constraints are met. Configuration bit stream is then generated which is used to configure the FPGA.

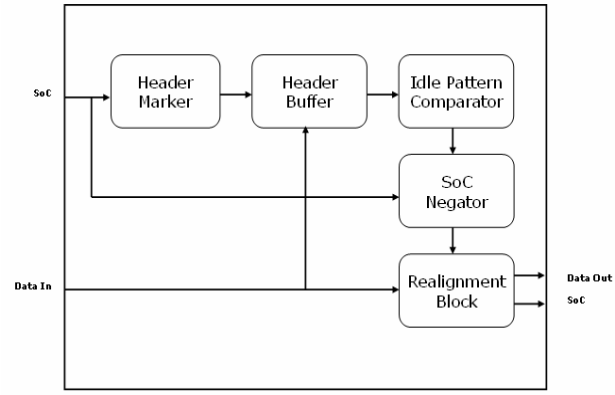

Figure 10: Idle Cell Terminator Block Diagram

A. Switch interface (Electrical/Physical)

The cable between the Switch Interface and the LPE must meet the following standard E1 attenuation and transmission requirements:

- 120 Ohm
- Two twisted pairs, category 3 or better
- 26 AWG or larger
- Maximum length: 200 m (655 feet)

The cable must include an RJ45 plug at the end dedicated to the LPE. It must also provide the appropriate plug or cabling system at the end dedicated to the ATM Switch. The ATM Switch and the LPE must be configured with several common parameters to interoperate. The Switch Interface's E1 parameters are in accordance with the ITU-T I .431 recommendations, as follows:

- Line coding: HDB3, according to ITU-T G.703[7]
- Frame format: Framed format (Data is carried in all timeslots except on TS0 and TS16) according to ITU-T G.704
- CRC4 to Non-CRC4 operation: not supported
- Line I/O impedance: 120 Ohm ± 5%

B. Media Interface(Electrical/physical)

The cable between the Media Interface and the Radio must meet the following standard E1 attenuation and transmission requirements:

- 120 Ohm
- Two twisted pairs, category 3 or better
- 26 AWG or larger
- Maximum length: 200 m (655 feet)

The cable must include an RJ45 plug at the end dedicated to the LPE. It must also provide the appropriate plug or cabling system at the end dedicated to the Radio.

The Media Interface's E1 parameters are in accordance [7] as follows:

- 120 Ohm
- Two twisted pairs, category 3 or better
- 26 AWG or larger
- Maximum length: 200 m (655 feet)

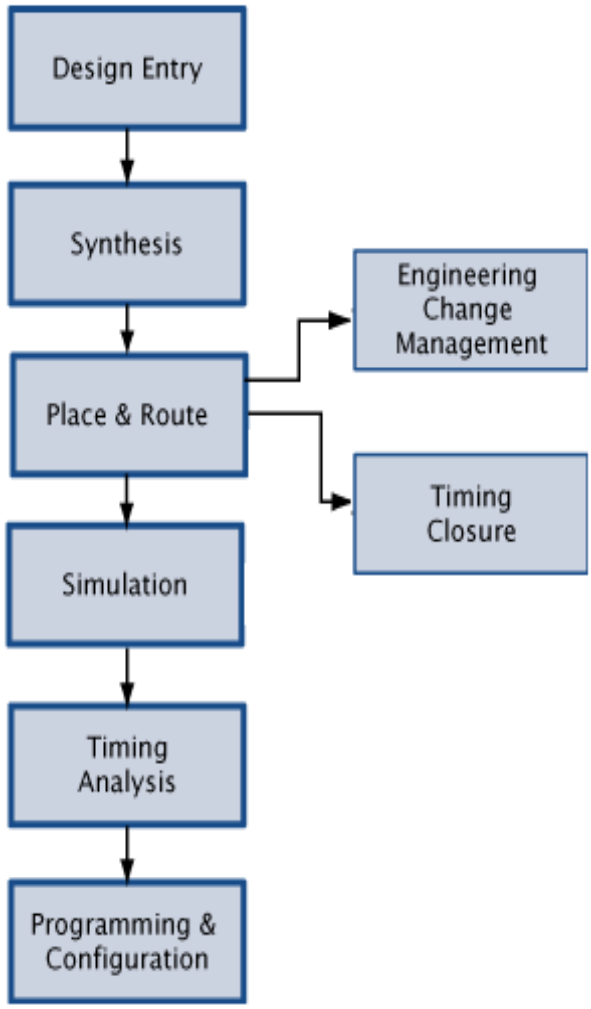

Figure 12: FPGA Block Diagram

The Radio and the LPE must be configured with common parameters to interoperate.

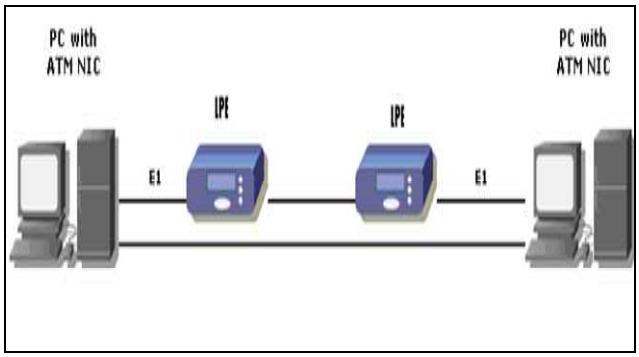

Figure 13: *Functional test setup 1*

	Octet 1	Octet 2	Octet 3	Octet 4	Octet 5
Header pattern	00000000	00000000	00000000	00000001	HEC = Valid code 01010010
NOTE 1 – The content of the information field is "01101010" repeated 48 times.					

Figure 11: Header pattern for Idle Cell identification [10]

V. TESTING & RESULTS

This section presents the theoretical calculations, experimental setups and the observed measurements.

A. Theoretical Calculations:

Cell Error Rate (CER) corresponding to the required Bit Error Ratio (BER) was calculated. This is required since the standard tests [11] give only the CER.

A Cell Error is declared when one or more bits in the ATM payload gets corrupted. Payload corruption is detected using CRC in O.191 tests.

$$CER = \sum_{i=1}^{n} \left\{ {}^{i}C_{384} \, P_e^{\,i} (1 - P_e)^{384 - i} \right\}$$

$$n = 384 \text{ (ATM Payload size)}$$

P_e= Probability of bit-error (≈ BER)

Calculated CERs corresponding to the required BERs are given in Table IV.

B. Functional Testing

Functional tests were carried out as shown in Figure 13 and Figure 14 to validate the data integrity and Phase Lock Loop (PLL) operations. These tests were carried out using ATM Network Interface Cards (NICs) installed on general purpose machines.

1) Test Setup 1

In setup 1 one of the links (transmit to receive) is transported through the LPEs as shown in Figure 13. The other link is connected directly. Permanent Virtual Circuit (PVC) is configured between the end-hosts in a point-to-point manner. The NIC is configured in such a way that any IP packet destined for the other ends host machine is directed to the PVC. This setting provides an IP over ATM connection between the hosts, thus enabling the use of any IP based services to test the LPE.

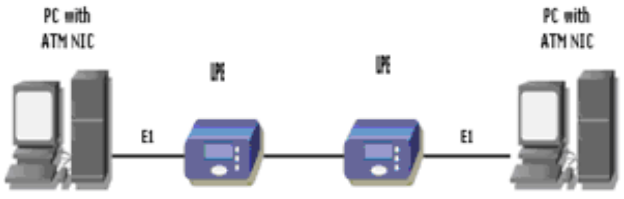

Figure 14: *Functional test setup 2*

Table IV: BER Vs. CER

BER	CER
10^{-3}	0.31899942
10^{-8}	3.8399926×10^{-6}

Ping application was used to test the functionality of the LPE. This program sends an ICMP echo request to a host and expects back an ICMP echo reply. This gives an opportunity to find dropped packets. A packet drop can occur because of faulty buffer management design. This test also verifies the data integrity issues of the device. Any modifications to the data transported through the LPE will result in a corrupted cell, which will be discarded at the receiving end and notified.

Ping test was performed with various payload sizes and no packet drops were observed, thus proving the functionality of the device in terms of logic and data integrity.

2) Test Setup 2

In test setup2, both transmit and receive of the NICs are *via.* the LPE as shown in Figure 14. Permanent Virtual Circuit (PVC) is configured between the two PCs in a point-to-point manner. The NIC is configured in such a way that any IP packet destined for the other PC is directed to the PVC. The same setting that was used for setup 1 was used, providing an IP over ATM connection between the hosts. This setup is characterized by multiple PLLs in the round trip path. Each of the interface cards uses a PLL to extract clock from the received data. This test emulates the normal usage scenario.

C. Performance testing

Performance tests were carried out to determine the BER improvement and latency under various traffic load conditions. The test setup employed for this purpose is shown in Figure 15. Referring to Figure 15, a Network Analyzer was used to generate and monitor ATM E1 traffic. ITU-T O.191[11] tests were carried out to find various error parameters and the latency. Channel Simulator was used to emulate the radio link characteristics in the laboratory settings. The channel simulator used is capable of generating various random errors and burst errors required for evaluation and testing.

In another setup (with LPE), where in the Switch Interface was connected to the network analyzer and the Media Interface connected to the Channel Simulator (shown in Figures 16 and 17).

The following tests were carried out to evaluate the performance of the LPE:

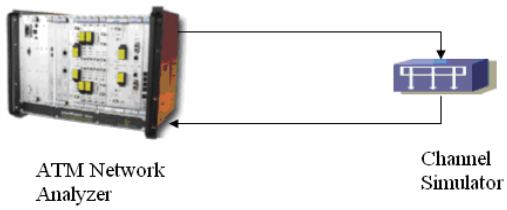

Figure 15: Channel Simulator test setup

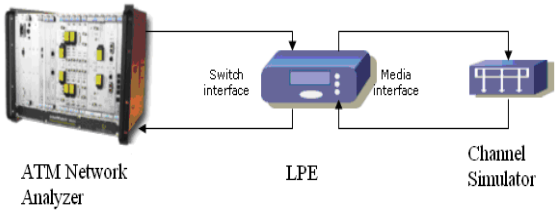

Figure 16: Performance test setup with media loop back

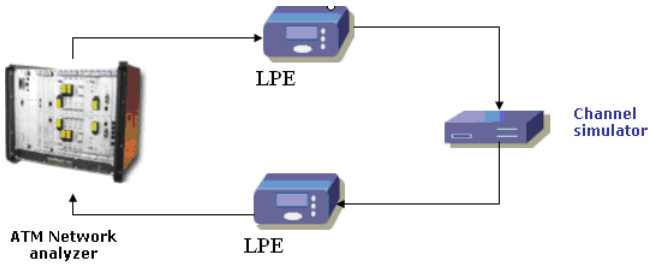

Figure 17: Performance test setup with channel simulator

BER improvement testing: Measures BER improvements for various input BERs.

- Load testing: Measures the system's ability to handle various types of traffic loads.
- Latency testing: Measures the round trip latency of the transmission path.
- Volume testing: Subjects the system to larger amounts of data to determine its point of failure.

The settings of the parameters were as follows

Traffic Profile

- Type: CBR
- Start Idle: 0
- Period: 0
- Utilization: 50
- Bandwidth: 0.959999

Block Size

- 16384

ATM QoS Test was run for various time intervals in setup with and without cell hardener. The following error-related network performance parameters (defined in Recommendations I.356) were measured:

- Cell Error Ratio
- Cell Loss Ratio
- Severely Errored Cell Block Ratio
- Cell Mis-insertion Rate

Network performance parameter definitions [12]

LPAC

The Loss of Performance Assessment Capability indicates that the ATM Measuring Equipment is no longer capable of measuring network performance parameters with sufficient confidence.

Cell Error Ratio

Cell Error Ratio (CER) is the ratio of total errored cells to the total of successfully transferred cells, plus tagged cells, plus errored cells in a population of interest. Successfully transferred cells, tagged cells, and errored cells contained in severely errored cell blocks are excluded from the calculation of cell error ratio.

Cell Loss Ratio

Cell Loss Ratio (CLR) is the ratio of total lost cells to total transmitted cells in a population of interest. Lost cells and transmitted cells in severely errored cell blocks are excluded from the calculation of cell loss ratio.

Cell Mis-insertion Rate

Cell Mis-insertion Rate (CMR) is the total number of ministered cells observed during a specified time interval divided by the time interval duration (equivalently, the number of mis-inserted cells per connection second). Mis-inserted cells and time intervals associated with severely errored cell blocks are excluded from the calculation of cell mis-insertion rate.

Severely Errored Cell Block

A cell block of size N shall be declared a severely errored cell block if the sum of errored, lost or mis-inserted cell outcomes, as detected by the ATM Measuring Equipment, within the cell block is greater than M=N/32.

Severely Errored Cell Block Ratio

Severely Errored Cell Block Ratio (SECBR) is the ratio of total severely errored cell blocks to total cell blocks in a population of interest.

NOTE – The severely errored cell block outcome and parameter provide a means of quantifying bursts of cell transfer failures and preventing those bursts from influencing the observed values for cell error ratio, cell loss ratio, cell mis-insertion rate, and the associated availability parameters.

D. Results of performance testing

The results obtained are tabulated and presented in this section. The theoretical calculations are presented in Table IV. The Cell Error Ratio observed in all the four experiments and the values obtained for various run times are tabulated in Tables VI-IX. The summary of all the measurements is in Table V. The measured values of CER matched with the theoretical calculations. (Tables IV and V) of the results.

Table V: Results Summary

BER	**Observed CER**			
min	*2*	*5*	*10*	*20*
10^{-3} Without LPE	0.3166	0.3161	0.3163	0.3156
10^{-8} With LPE	4.08×10^{-6}	9.17×10^{-6}	7.449×10^{-6}	5.94×10^{-6}

1) Test time: 2 Minutes

Table VI: Results with test time 2 min.

1/1024 BER	Without LPE	With LPE
Cells/Sec	2262.907	2246.532
Mbps	0.9595	0.9525
LPAC	OK	OK
Min Delay (us)	41.24	3754.28
Max Delay (us)	45.28	3977.04
Avg Delay (us)	43.67	3870.85
2Pt Delay	4.04	222.72
Total	242131	244872
Cells Lost	127	7
Ratio	0.0005242	2.859xE-5
Mis-insertion	0	0
Rate	0	0
Errored Cells	76662	1
Rate	0.316614	4.084xE-6
Severely Errored Blocks	14	0
Ratio	1	0

2) Test time: 5 Minutes

Table VII: Results with test time 5 min.

1/1024 BER	Without LPE	With LPE
Cells/Sec	2256.588	2264.031
Mbps	0.9568	0.9599
LPAC	OK	OK
Min Delay (us)	41.24	3754.24
Max Delay (us)	45.28	3977.04
Avg Delay (us)	43.67	3871.16
2Pt Delay	4.04	222.72
Total	652154	654305
Cells Lost	359	18
Ratio	0.00055	2.7509xE-5
Mis-insertion	0	0
Rate	0	0
Errored Cells	206116	6
Rate	0.3160542	9.17xE-6
Severely Errored Blocks	39	0
Ratio	0.9286	0

3) Test time: 10 Minutes

Table VIII: Results with test time 10 min.

1/1024 BER	Without LPE	With LPE
Cells/Sec	2259.38	2264.044
Mbps	0.95798	0.95996
LPAC	OK	OK
Min Delay (us)	41.24	3754.24
Max Delay (us)	45.28	3977.04
Avg Delay (us)	43.62	3871.13
2Pt Delay	4.04	222.72
Total	1330776	1333522
Cells Lost	676	28
Ratio	0.0005077	2.09966xE-5
Mis-insertion	0	0
Rate	0	0
Errored Cells	420871	10
Rate	0.3162598	7.49894xE-6
Severely Errored Blocks	81	0
Ratio	0.8617	0

4) Test time: 20 Minutes

Table IX: Results with test time 20 min.

1/1024 BER	Without LPE	With LPE
Cells/Sec	2261.338	2264.05
Mbps	0.9588	0.9599
LPAC	OK	OK
Min Delay (us)	41.24	3754.2
Max Delay (us)	45.28	3977.04
Avg Delay (us)	43.62	3871.17
2Pt Delay	4.04	222.76
Total	2684208	2691952
Cells Lost	1278	53
Ratio	0.000476	1.969xE-5
Mis-insertion	0	0
Rate	0	0
Errored Cells	847025	16
Rate	0.31556	5.9436xE-6
Severely Errored Blocks	163	0
Ratio	0.75814	0

E. Conformance Test

1) G.703 Conformance testing (for120 Ω twisted pair 2048 kbit/s interface):

G.703 recommendation specify the physical/electrical characteristics of hierarchical digital interfaces.

General characteristics:

Bit rate: 2048 kbit/s ± 50 ppm.

Code: High density bipolar of order 3 (HDB3)

Interface specifications:

The template for the transmitted pulse, as specified in G.703, is shown in Table IX. The nominal peak voltage of a mark is 3 volts for 120 Ω twisted pair applications and 2.37 volts for 75 Ω coax applications. The ratio of the amplitude of the transmit pulses generated by TTP and TRING is between 0.95 and 1.05. The interface specification parameters were measured for the E1 interfaces of Switch Interface and Media Interface. The results are shown in Table X, Table XII, Figures 19-22. .

Switch and media Interface measurements:

Table X: Measurements at switch interface

Parameter	Value
Pair(s) in each direction	*One symmetrical pair*
Test load impedance	120 ohms resistive
Nominal peak voltage of a mark (pulse)	2.72 V
Peak voltage of a space (no pulse)	0.28 V
Nominal pulse width	243 ns
Ratio of the amplitudes of positive and negative pulses at the centre of the pulse interval	1.01
Ratio of the widths of positive and negative pulses at the nominal half amplitude	0.99

Table XI: Template of transmitted pulse

Pulse shape (nominally rectangular)	All marks of a valid signal must conform to the mask (see Figure above) irrespective of the sign. The value V corresponds to the nominal peak value.	
Pair(s) in each direction	*F. One coaxial pair*	*G. One symmetrical pair*
Test load impedance	75 ohms resistive	120 ohms resistive
Nominal peak voltage of a mark (pulse)	2.37 V	3 V
Peak voltage of a space (no pulse)	0 ± 0.237 V	0 ± 0.3 V
Nominal pulse width	244 ns	
Ratio of the amplitudes of positive and negative pulses at the centre of the pulse interval	0.95 to 1.05	
Ratio of the widths of positive and negative pulses at the nominal half amplitude	0.95 to 1.05	

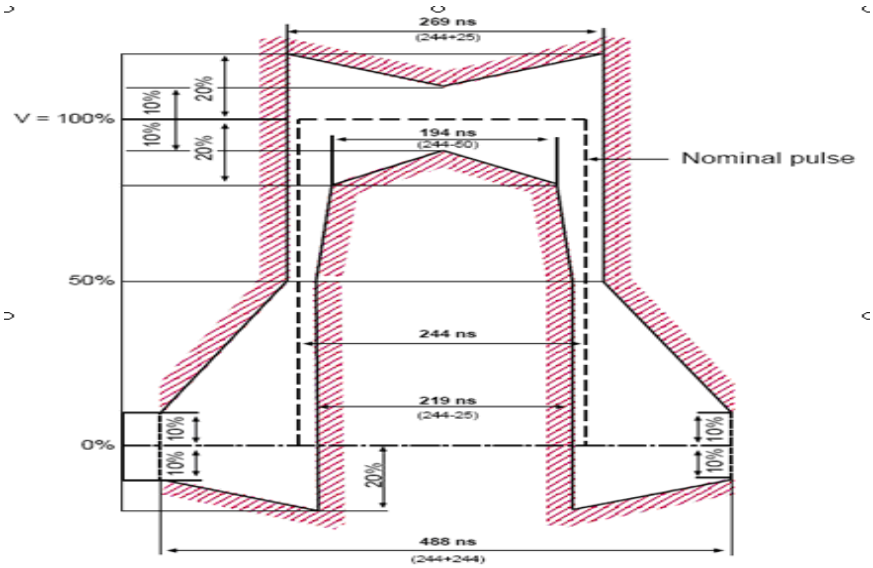

Figure 18: Mask of the pulse at the 2.048 Mbps interface [7]

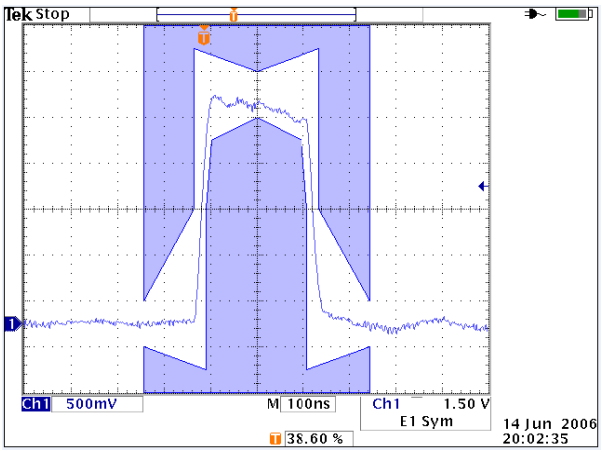

Figure 19: Mask of the pulse switch interface E1 interface

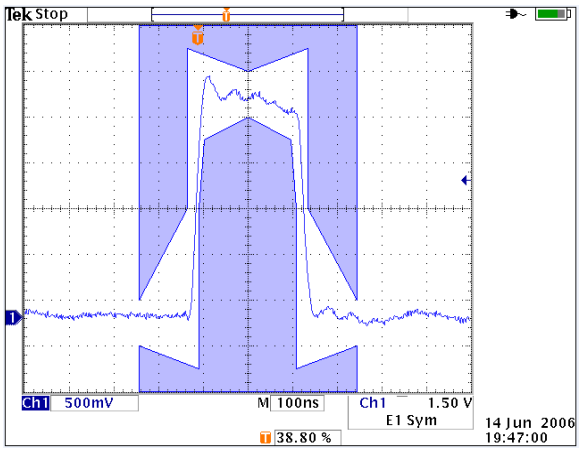

Figure 20: Mask of the pulse media interface E1 interface

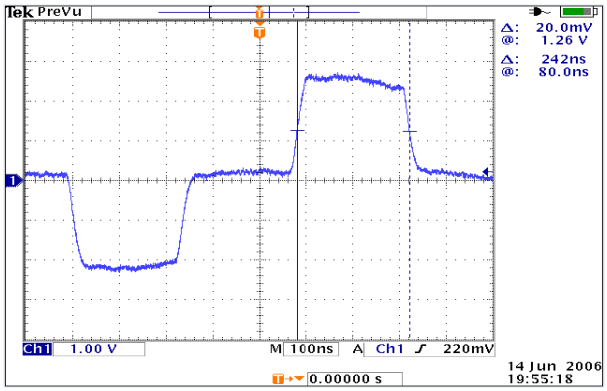

Figure 21: Waveform at Switch Interface E1 interface

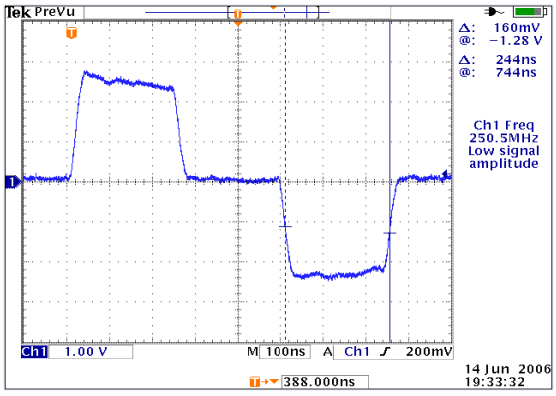

Figure 22: Waveform at media interface E1 interface

Table XII: Measurements at media interface

Parameter	\Value
Pair(s) in each direction	*One symmetrical pair*
Test load impedance	120 ohms resistive
Nominal peak voltage of a mark (pulse)	2.76 V
Peak voltage of a space (no pulse)	0.17 V
Nominal pulse width	244ns
Ratio of the amplitudes of positive and negative pulses at the centre of the pulse interval	1.01
Ratio of the widths of positive and negative pulses at the nominal half amplitude	0.99

The values obtained are matching with the values specified in the G.703 recommendation.

E1 Mask Template

The pulses generated by E1 equipment should fall within the template shown in Table XII & Figure 18. Therefore, E1 Mask test was performed on the E1 interfaces of Switch Interface and Media Interface

2) G.704 Conformance Testing (for 2048 kbit/s interface)

G.704 recommendation specifies the synchronous frame structures used at 1544, 6312, 2048, 8488 and 44.736 kbit/s hierarchical levels.

Basic Frame structure is used for all interfaces. All timeslots except TS0 and TS16 are used for carrying data.

Specification:

The frames generated by the various interfaces were given to an E1 analyzer. Framed mode tests were performed successfully on Switch Interface. Unframed mode tests were performed on Media Interface successfully.

3) G.804 Conformance testing (for 2048 kbit/s interface)

G.804 recommendation specifies the mapping to be used for this transport of ATM cells on the different PDH bit rates for both 1544 and 2048 kbit/s hierarchies. The ATM cell is mapped into bits 9 to 128 and bits 137 to 256 (i.e. time slots 1 to 15 and time slots 17 to 31 described in Recommendation G.704) of the 2048 kbit/s frame with the octet structure of the cell aligned with the octet structure of the frame.

Test setup

To verify that the Switch Interface E1 interface conforms to the G.804 standard, the setup shown in Figure 24 was used. ATM traffic generator was used to generate ATM traffic. This traffic is routed to the first LPE through its Switch Interface. The Media Interface of the first LPE is connected to the Media Interface of the second LPE. The Switch Interface of second LPE is connected to a host machine with ATM/E1 interface. The traffic generated by the ATM analyzer was received correctly at the host. This test verifies the conformance to the standard.

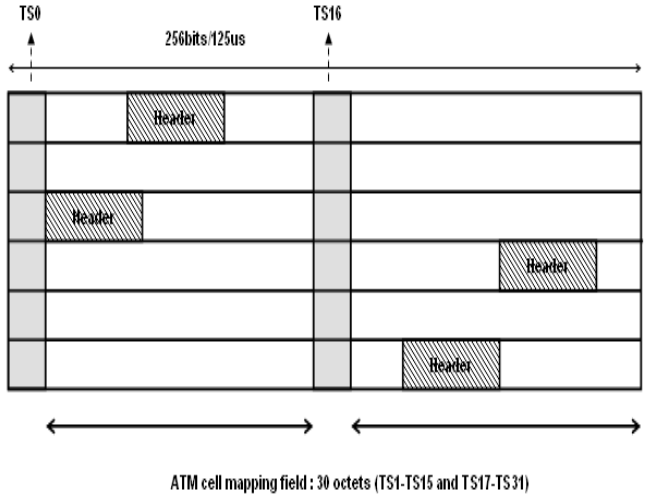

Figure 23: Frame structure for 2048 kbit/s used to transport ATM cells [9]

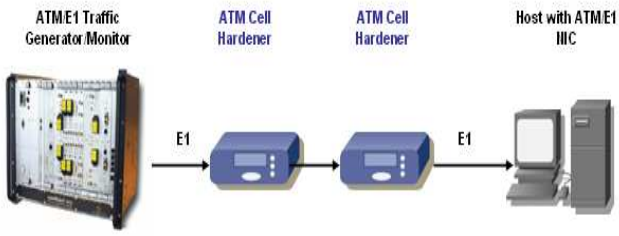

Figure 24: G.804 conformance test setup

VI. CONCLUSIONS

The usage scenario of the Link Performance Enhancer was described. The specifications were derived for this particular usage scenario. Several error correcting codes were studied and the choice was RS (255,235) code. The block synchronization was designed and the bandwidth handling was done intelligently to minimize the overhead. This paper presents the specification, design architecture, and implementation details of the LPE. Test results obtained were tabulated and analyzed. Test results included the outputs of functional, performance and conformance tests recommended by the standards.

Further, this work can be extended to support any E1 links, the FEC can be made adaptive and an enhanced user interface can be developed.

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