

Rule-Based Synthesis of Ternary Reversible Up/Down Counters

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Abstract—A ternary bijective logic function can be implemented as a reversible circuit using ternary reversible gates. These gates can be constructed using existing technologies as well as quantum technology. Considerable amount of works have been reported in the literature on synthesis of ternary reversible combinational circuits. In comparison, synthesis of ternary reversible sequential circuits is in the infancy. In this paper, we present a truth table based rule generation and then rule based synthesis of n -qutrit ternary reversible level-triggered synchronous up/down counters. The presented method produces better circuits than those reported in the literature in terms of both quantum cost and ancilla inputs needed.

Index Terms—Ternary reversible circuits, Ternary reversible counters, Rule generation, Rule based circuit synthesis, Ternary reversible gates.

I. INTRODUCTION

A TERNARY n variable reversible logic function is a bijective function $f : \{0, 1, 2\}^n \mapsto \{0, 1, 2\}^n$ such that each of the 3^n input combinations are uniquely mapped to one of the 3^n output combinations. In such a function each output combination can also be uniquely mapped back to one of the input combinations. Circuit implementation of an n variable reversible ternary logic function has n inputs and n outputs. This type of logic circuits are called ternary reversible logic circuits. Theoretically, ternary reversible circuits can be implemented using any existing technology. However, ternary reversible logic synthesis using unary and Muthukrishnan-Stroud (M-S) quantum gates [1] has become very popular in the literature.

Like binary logic circuits, ternary logic circuits are also of two types, combinational circuits and sequential circuits. A remarkable number of works have been reported in the literature on ternary reversible combinational circuit synthesis. These works can be categorized into three types, such as general synthesis methods for arbitrary ternary reversible circuits, testable synthesis methods for arbitrary ternary reversible circuits, and special design of practically important medium scale modular ternary reversible circuits.

The non-exhaustive but representative works on general synthesis methods for arbitrary ternary reversible circuits are reported in [2]–[17]. Readers may see these references for details of the trends and techniques of general synthesis methods for ternary reversible combinational circuit.

Testable designs of arbitrary ternary reversible combinational circuits are reported in [18]–[20].

It has been found that general design techniques produce larger circuits for different practically important medium

scale modular circuits. Therefore, special design techniques are used for synthesis of such circuits, which produce better circuits. Some non-exhaustive works on such special designs are mentioned here. Designs of ternary reversible adder and adder/subtractor are reported in [21]–[23]. Designs of ternary reversible encoder and decoder are reported in [24]. Designs of ternary reversible multiplexer and demultiplexer are reported in [25]. Designs of ternary reversible comparator are reported in [26], [27]. Design of ternary reversible barrel shifter is reported in [28]. Design of ternary reversible systolic array is reported in [29].

Unlike ternary reversible combinational circuit synthesis, only a few works have been reported in the literature on ternary reversible sequential circuit synthesis. Similar to the ternary reversible combinational circuit synthesis methods, two approaches of ternary reversible sequential circuit synthesis have been reported in the literature, such as general design method for arbitrary ternary reversible sequential circuit and special design method for practically important modular ternary reversible sequential circuits. A general design method for arbitrary ternary reversible sequential circuits is presented in [30].

It has also been found that designing practically important modular ternary reversible circuits using special technique rather than using general design technique produces better result. In [31], design of a ternary reversible T flip-flop is presented. Then two approaches of design of n -trit (*ternary digit*) ternary reversible up counter is presented. The second approach produces better designs in terms of both quantum cost and ancilla inputs needed. In this paper, we present a new approach of design of n -trit ternary reversible up counter, which produces better circuits than those reported in [31] in terms of both quantum cost and ancilla inputs needed. We also present design method for n -trit ternary reversible down counter. Combining these two techniques, finally, we present design of n -trit ternary reversible up/down counter. As our designs require very few ancilla inputs, it will be more suitable for quantum realization than the designs in [31].

The rest of the paper is organized as follows. In Section II, we introduce preliminary concepts on ternary reversible logic and circuit synthesis, which will be needed to understand the rest of the paper. In Section III, we present our synthesis method for ternary reversible up counters. In Section IV, we present our synthesis method for ternary reversible down counters. In Section V, we present our synthesis method for ternary reversible up/down counters. Finally, in Section VI, we conclude the paper with direction to future work.

II. PRELIMINARY CONCEPTS

In this section, we discuss basic concepts on ternary reversible logic and circuit synthesis.

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TABLE I
 TERNARY REVERSIBLE UNARY OPERATIONS

x	+0	+1	+2	01	02	12
0	0	1	2	1	2	0
1	1	2	0	0	1	2
2	2	0	1	2	0	1

A. Galois Field 3 Operations

Galois field 3 (GF3 in short) is a finite field, which has the set of values $T = \{0, 1, 2\}$ with two binary operations as defined below [6], [9], [12]:

Addition: $a + b \text{ (GF3)} = (a + b) \bmod 3$

Multiplication: $a \cdot b \text{ (GF3)} = ab \text{ (GF3)} = (a \times b) \bmod 3$

GF3 addition and multiplication operations are commutative and associative. GF3 multiplication is distributive over addition.

Readers should note that, in this paper, $+$ and \cdot signs are used in both arithmetic and GF3 context. When used in GF3 context, they are explicitly indicated by appending (GF3) at the end of the expression as shown above.

B. Ternary Reversible Unary Operations

When an operation is applied on a single operand, then the operation is called a unary operation. Ternary reversible unary operations changes the value of an operand in bijective manner. The $3! = 6$ ternary reversible unary operations are shown in Table I [12]. In this paper, we will use only +1 and +2 operations.

C. Ternary Reversible Unary Gates

A gate is a physical device or circuit that changes the input value(s) to the output value(s) based on the operation associated with the gate. A ternary reversible unary gate changes the value of a single input to a single output based on the ternary reversible unary operations shown in Table I [12]. Therefore, there are six ternary reversible unary gates. The symbol of ternary reversible unary gates is shown in Fig. 1, where $U \in \{+0, +1, +2, 01, 02, 12\}$ is a ternary reversible unary operation and Ux is the output value after application of the ternary reversible unary operation U on the input value x . A ternary reversible unary gate with +0 operation is a wire. Theoretically ternary reversible unary gates can be realized using any existing technology. However, most of the works refer to the quantum realization [1] of these gates. In this paper, we will use these gates as generic gates without considering their realization issues. This type of gate is considered as an elementary gate and its realization cost is assumed to be 1. As in most of the works this type of gate is assumed to be quantum realizable [1], its realization cost is called quantum cost (QC) and its QC is considered to be 1. In this paper, we will indicate the circuit realization cost using the QC metric, although we assume that these circuits can be realized using any existing technology.

D. Ternary Reversible Controlled Unary Gates

In a ternary reversible controlled unary gate, a single input (called the target input) value is changed using a

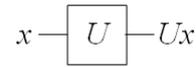


Fig. 1. Symbol of ternary reversible unary gate

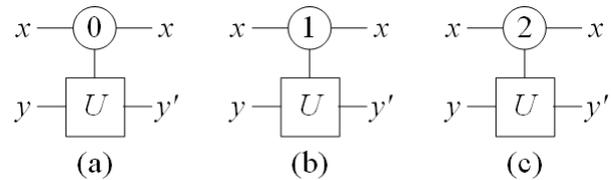


Fig. 2. Symbols of ternary reversible controlled unary gates

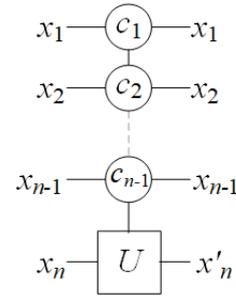


Fig. 3. Symbol of ternary reversible multiple-controlled unary gate

ternary reversible unary operation $U \in \{+1, +2, 01, 02, 12\}$ conditional on the value of another input (called the control input). Symbols of three ternary reversible controlled unary gates are shown in Fig. 2. In Fig. 2, the input x is the control input and is passed unchanged to the output. The input y is the target input and is changed using the ternary reversible unary operation U only when the value of x is equal to the specified control value, that is, $y' = Uy$. Otherwise the target input value is passed unchanged to the output, that is, $y' = y$. For example, in Fig. 2(a), the control value is 0. The value of control input x is passed unchanged to the output. When $x = 0$, then $y' = Uy$, otherwise $y' = y$. The operations of the other two ternary reversible controlled unary gates in Fig. 2(b) and (c) can be explained in a similar way.

The ternary reversible controlled unary gate in Fig. 2(c) is quantum realizable [1] and is called Muthukrishnan-Stroud (M-S) gate. It is considered to be an elementary gate with QC of 1. However, in this paper, we assume that this gate is a generic gate and is realizable using any existing technology.

The ternary reversible controlled unary gates in Fig. 2(a) and (b) can be realized using two ternary reversible unary gates and one M-S gate resulting into a QC of 3 [16], [17], [24].

E. Ternary Reversible Multiple-Controlled Unary Gates

The symbol of an n -trit ternary reversible multiple-controlled unary gate is shown in Fig. 3, where x_1, x_2, \dots, x_{n-1} are control inputs with corresponding control values c_1, c_2, \dots, c_{n-1} ; x_n is the target input; $U \in \{+1, +2, 01, 02, 12\}$ is the unary operation; and x'_n is the target output. All the $(n - 1)$ control inputs are passed unchanged to the corresponding outputs. The target output is $x'_n = Ux_n$ only when $(x_1 = c_1 \wedge x_2 = c_2 \wedge \dots \wedge x_{n-1} = c_{n-1})$, otherwise $x'_n = x_n$.

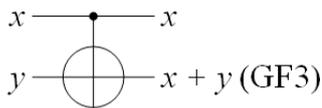


Fig. 4. Symbol of a ternary Feynman gate

The n -trit ternary reversible multiple-controlled unary gate of Fig. 3 is called Generalized Toffoli gate in [22], [23], [25], [26]. But this type of gate is called multiple-controlled unary gate in [16], [17]. In this paper, we will use ternary reversible multiple-controlled unary gate to refer to this type of gate.

Realizations of n -trit ternary reversible multiple-controlled unary gate of Fig. 3 using ternary reversible unary gates and M-S gates are presented in [16], [17], [22], [23], [25], [26]. All realization methods are basically similar and produce similar circuits, but the realization approaches are slightly different. Analyzing all realization approaches, we have determined the circuit complexity of an n -trit ($n \geq 3$) ternary reversible multiple-controlled unary gate as in (1) and (2). Design of a reversible circuit often requires additional constant-initialized working inputs in addition to the primary inputs. These constant-initialized working inputs are called Ancilla (Anc) inputs.

$$\begin{aligned} \text{QC} &= 5 + (n - 3) \times 4 + 2 \times \text{number of non-2 control inputs} & (1) \\ \text{Anc} &= n - 2 & (2) \end{aligned}$$

F. Ternary Feynman Gate

The symbol of a ternary Feynman gate is shown in Fig. 4, where x is the control input and is passed unchanged to the output; y is the target input; and the target output is $x + y$ (GF3). Realization of a ternary Feynman gate using ternary reversible unary gates and M-S gates is presented in [22], [23], [25], [32], [33], where the QC of the realization is 4 and no Anc is required.

In reversible circuit, fan-out of a signal is not allowed. In that case, a copy of the signal is generated along a 0-initialized Ancilla input. For this purpose, the ternary Feynman gate is used. When the target input is $y = 0$, then the target output is $x + y$ (GF3) = $x + 0$ (GF3) = x , which is a copy of the control input x .

III. SYNTHESIS OF TERNARY REVERSIBLE UP COUNTERS

In this section, we present our synthesis method for ternary reversible up counters.

We design a level-triggered synchronous counter, that means, when the clock signal is $C = 2$, then all the outputs are simultaneously updated to the next count value and when the clock signal is $C = 0$ or $C = 1$, then the outputs remain unchanged.

A. 2-Trit Up Counter

The truth table of a 2-trit up counter is shown in Table II, where $Q1Q0$ is the present state and $Q1'Q0'$ is the next state. The next state is used as the counter output. From an analysis of the truth table, we develop the two rules shown in (3) and (4).

 TABLE II
TRUTH TABLE OF A 2-TRIT UP COUNTER

$Q1Q0$	$Q1'Q0'$
00	01
01	02
02	10
10	11
11	12
12	20
20	21
21	22
22	00

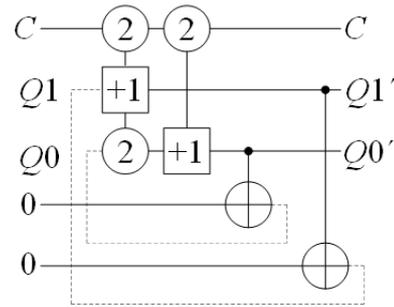


Fig. 5. Realization of a 2-trit up counter

$$Q0 = 2 \Rightarrow Q1' = Q1 + 1 \text{ (GF3)} \quad (3)$$

$$Q0' = Q0 + 1 \text{ (GF3)} \quad (4)$$

Based on the rules in (3) and (4), we design the circuit of a 2-trit up counter as shown in Fig. 5. The rule in (3) is realized using a 3-trit multiple-controlled unary gate, where the clock input C and the fed-back input $Q0$ are control inputs with control value 2; and the fed-back input $Q1$ is the target input with a +1 unary operation. The rule in (4) is realized using a controlled unary gate, where the clock input C is the control input with control value 2 and the fed-back input $Q0$ is the target input with a +1 operation. The fed-back inputs are generated using two Feynman gates as copying gates. We assume that the feedback lines (dashed lines) have a delay exactly equal to the duration of the clock $C = 2$, otherwise the output of the counter will be changed more than ones during the clock application. When the clock input is $C = 0$ or $C = 1$, then both the 3-trit multiple-controlled unary gate and the controlled unary gate will be inactive. Thus, the fed-back values of $Q1$ and $Q0$ will be passed unchanged to the outputs maintaining the counter output unchanged. When the clock input is $C = 2$ and $Q0 = 2$, then the 3-trit multiple-controlled unary gate will implement the rule in (3) by incrementing the fed-back value of $Q1$ to produce $Q1'$ output. When the clock input is $C = 2$, then the controlled unary gate will implement the rule in (4) by incrementing the fed-back value of $Q0$ to produce $Q0'$ output.

In Fig. 5, the QC of the 3-trit multiple-controlled unary gate is $(5 + (3 - 3) \times 4 + 2 \times 0) = 5$ (see (1)), the QC of the controlled unary gate is 1, and the QC of each of the ternary Feynman gate is 4. Thus, the quantum cost of the 2-trit up counter is $\text{QC} = (5 + 1 + 2 \times 4) = 14$. The realization of the 3-trit multiple-controlled unary gate requires $\text{Anc} = (3 - 2) = 1$

TABLE III
 TRUTH TABLE OF A 3-TRIT UP COUNTER

$Q_2Q_1Q_0$	$Q_2'Q_1'Q_0'$
000	001
001	002
002	010
010	011
011	012
012	020
020	021
021	022
022	100
100	101
101	102
102	110
110	111
111	112
112	120
120	121
121	122
122	200
200	201
201	202
202	210
210	211
211	212
212	220
220	221
221	222
222	000

(see (2)) and each of the copying Feynman gate requires one 0-initialized working input. Thus, the total Ancilla inputs of the 2-trit up counter is $Anc = (1 + 2 \times 1) = 3$.

B. 3-Trit Up Counter

The truth table of a 3-trit up counter is shown in Table III, where $Q_2Q_1Q_0$ is the present state and $Q_2'Q_1'Q_0'$ is the next state. From an analysis of the truth table, we develop the three rules shown in (5), (6), and (7).

$$Q_1Q_0 = 22 \Rightarrow Q_2' = Q_2 + 1 \text{ (GF3)} \quad (5)$$

$$Q_0 = 2 \Rightarrow Q_1' = Q_1 + 1 \text{ (GF3)} \quad (6)$$

$$Q_0' = Q_0 + 1 \text{ (GF3)} \quad (7)$$

Based on the rules in (5), (6), and (7), we design the circuit of a 3-trit up counter as shown in Fig. 6. The rules in (5), (6), and (7) are realized using a 4-trit multiple-controlled unary gate, a 3-trit multiple-controlled unary gate, and a controlled unary gate, respectively. The operation of the circuit in Fig. 6 is similar to that in Fig. 5.

In Fig. 6, the QC of the 4-trit multiple-controlled unary gate is $(5 + (4 - 3) \times 4 + 2 \times 0) = 9$; the QC of the 3-trit multiple-controlled unary gate is $(5 + (3 - 3) \times 4 + 2 \times 0) = 5$; the QC of the controlled unary gate is 1; and the QC of each of the ternary Feynman gate is 4. Thus, the quantum cost of the 3-trit up counter is $QC = (9 + 5 + 1 + 3 \times 4) = 27$. The realization of the 4-trit multiple-controlled unary gate requires $Anc = (4 - 2) = 2$ and the 3-trit multiple-controlled

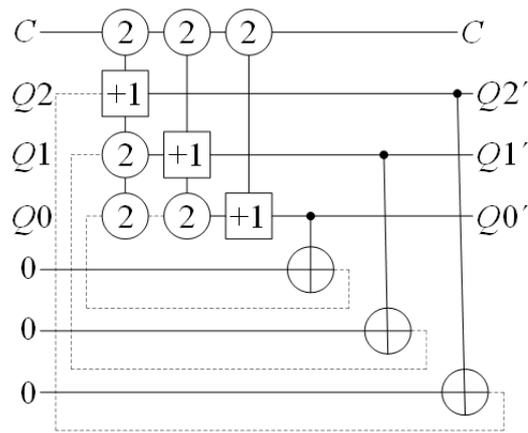


Fig. 6. Realization of a 3-trit up counter

unary gate requires $Anc = (3 - 2) = 1$ (see (2)). As the 2 Ancilla inputs required for the 4-trit multiple-controlled unary gate are restored at the output, these Ancilla inputs can be reused for the 3-trit multiple-controlled unary gate. Thus, the Ancilla input required by all multiple-controlled unary gates is equal to the Ancilla inputs required by the largest multiple-controlled unary gate. Each of the copying Feynman gate requires one 0-initialized working input. Thus, the total Ancilla inputs of the 3-trit up counter is $Anc = (2 + 3 \times 1) = 5$.

C. n-Trit Up Counter

From the rules in (3), (4), (5), (6), and (7), we can generalize the rules for an n -trit up counter as in (8) and (9). An n -trit up counter requires a total of n rules. The rule in (8) generates $(n - 1)$ rules and the rule in (9) generates another rule resulting into a total of n rules.

$$\text{For } i = 1, 2, \dots, (n - 1),$$

$$Q(i - 1)Q(i - 2) \cdots Q_1Q_0 = 22 \cdots 22 \quad (8)$$

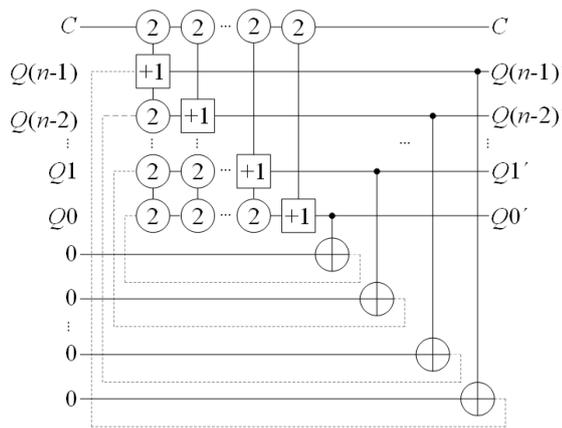
$$\Rightarrow Q_i' = Q_i + 1 \text{ (GF3)}$$

$$Q_0' = Q_0 + 1 \text{ (GF3)} \quad (9)$$

Based on the rules in (8) and (9), the circuit structure of an n -trit up counter is shown in Fig. 7. The QC and Anc for an n -trit up counter are given in (10) and (11), respectively.

$$\begin{aligned}
 QC &= \sum_{i=3}^{(n+1)} QC \text{ of } i\text{-trit multiple-controlled unary gate} \\
 &\quad + QC \text{ of one controlled unary gate} \\
 &\quad + n \times QC \text{ of Feynman gate} \\
 &= \sum_{i=3}^{(n+1)} (5 + (i - 3) \times 4 + 2 \times 0) + 1 + 4n \\
 &= \sum_{i=3}^{(n+1)} (4i - 7) + 1 + 4n
 \end{aligned} \quad (10)$$

$$\begin{aligned}
 Anc &= Anc \text{ for } (n + 1)\text{-trit multiple-controlled unary gate} \\
 &\quad + \text{Number of Feynman gates} \\
 &= (n + 1 - 2) + n \\
 &= 2n - 1
 \end{aligned} \quad (11)$$


 Fig. 7. Realization of an n -trit up counter

D. Comparison With Previous Work

In [31], designs of ternary reversible up counters were presented. The authors designed a ternary T flip-flop using a 3-trit multiple-controlled unary gate and a Feynman gate as copying gate (see Fig. 7 in [31]) and used the ternary T flip-flop as the building block of ternary reversible up counters. They assumed that QC of a Feynman gate is 1. Thus, they assumed that QC of a ternary T flip-flop is $(5 + 1) = 6$. They counted only the 0-initialized constant input of the copying Feynman gate as Ancilla input. However, the 3-trit multiple-controlled unary gate requires an Ancilla input. For comparing the circuit complexity with our designs, we recalculated that QC of a ternary T flip-flop is $(5 + 4) = 9$ and Anc is $(1 + 1) = 2$.

The authors presented two approaches of designing ternary reversible up counters. The second approach is more cost effective. So, we compare our designs with that of the second approach in [31].

In the second approach in [31], the authors designed an n -trit up counter using n number of ternary T flip-flops and $(n - 1)$ number of 3-trit multiple-controlled unary gates (see Fig. 11 in [31]). The authors calculated the quantum cost of an n -trit up counter to be $QC = n \times 6 + (n - 1) \times 5 = 11n - 5$. However, under our QC assumption of a ternary T flip-flop to be 9, the quantum cost of an n -trit up counter will be $QC = n \times 9 + (n - 1) \times 5 = 14n - 5$. The authors counted constant inputs to be $n \times 1 + (n - 1) \times 2 = 3n - 2$. But the authors did not count the constant input required for the design of a 3-trit multiple-controlled unary gate. Moreover, they counted one constant input for each ternary T flip-flop. But, the constant input required for a ternary T flip-flop is 2. Thus, the Ancilla inputs required for an n -trit up counter will be $n \times 2 + (n - 1) \times 3 = 5n - 3$.

The comparison of the circuit complexity of our design of an n -trit up counter with that in [31] is tabulated in Table IV for $n = 2, 3, 4, 5, 6, 7$. From Table IV, we see that in case of the designs in [31], the QC is incremented by 14 and the Anc is incremented by 4 for going from n to $(n + 1)$. In case of our designs, from (10) and (11), we see that the QC is incremented by $(n + 2) \times 4 - 3$ and the Anc is incremented by 2 for going from n to $(n + 1)$. For $n = 2, 3, 4$, our designs require less QC; for $n = 5$, our design requires equal

 TABLE IV
COMPARISON OF THE CIRCUIT COMPLEXITY OF OUR DESIGN OF AN n -TRIT UP COUNTER WITH THAT IN [31]

n	Design in [31]		Our Design	
	QC	Anc	QC	Anc
2	23	7	14	3
3	37	12	27	5
4	51	17	44	7
5	65	22	65	9
6	79	27	90	11
7	93	32	119	13

 TABLE V
TRUTH TABLE OF A 2-TRIT DOWN COUNTER

$Q1Q0$	$Q1'Q0'$
00	22
01	00
02	01
10	02
11	10
12	11
20	12
21	20
22	21

QC; and for $n > 5$, our designs require more QC than that in [31]. However, for all ns our designs require very less Anc than that in [31]. Overall, our designs are better than that in [31] for $n = 2, 3, 4$ in respect to both QC and Anc. However, our designs are much better than that in [31] for all ns in respect to Anc. In quantum realizations, creating large number of quantum states (representing the inputs/outputs of the quantum circuit) is more difficult than creating large number of elementary quantum gates [34]. Thus, our designs of ternary reversible up counters will be more favorable for quantum realizations than those in [31].

IV. SYNTHESIS OF TERNARY REVERSIBLE DOWN COUNTERS

In this section, we present our synthesis method for ternary reversible down counters.

A. 2-Trit Down Counter

The truth table of a 2-trit down counter is shown in Table V, where $Q1Q0$ is the present state and $Q1'Q0'$ is the next state. From an analysis of the truth table, we develop the two rules shown in (12) and (13).

$$Q0 = 0 \Rightarrow Q1' = Q1 + 2 \text{ (GF3)} \quad (12)$$

$$Q0' = Q0 + 2 \text{ (GF3)} \quad (13)$$

Based on the rules in (12) and (13), we design the circuit of a 2-trit down counter as shown in Fig. 8. The rule in (12) is realized using a 3-trit multiple-controlled unary gate with a control value of 2 for the clock input C and a control value of 0 for the fed-back input $Q0$, where the fed-back input $Q1$ is the target input with a +2 unary operation. The rule in (13) is realized using a controlled unary gate with a control value

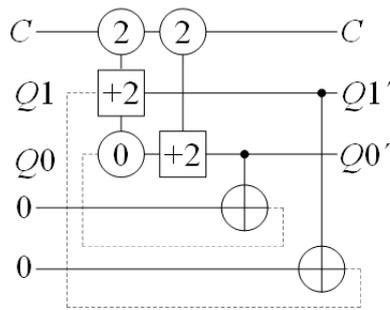


Fig. 8. Realization of a 2-trit down counter

of 2 for the clock input C and the fed-back input Q_0 as the target input with a +2 operation. The operation of the circuit in Fig. 8 is similar to that in the circuit in Fig. 5.

In Fig. 8, the QC of the 3-trit multiple-controlled unary gate is $(5 + (3 - 3) \times 4 + 2 \times 1) = 7$ (see (1)), the QC of the controlled unary gate is 1, and the QC of each of the ternary Feynman gate is 4. Thus, the quantum cost of the 2-trit down counter is $QC = (7 + 1 + 2 \times 4) = 16$, which is 2 more than that of a 2-trit up counter. The realization of the 3-trit multiple-controlled unary gate requires $Anc = (3 - 2) = 1$ (see (2)) and each of the copying Feynman gate requires one 0-initialized working input. Thus, the total Ancilla inputs of the 2-trit down counter is $Anc = (1 + 2 \times 1) = 3$, which is same as that of a 2-trit up counter.

B. n -Trit Down Counter

Like an n -trit up counter, we can generalize the rules for an n -trit down counter as in (14) and (15). An n -trit down counter requires a total of n rules. The rule in (14) generates $(n - 1)$ rules and the rule in (15) generates another rule resulting into a total of n rules.

$$\begin{aligned} \text{For } i = 1, 2, \dots, (n - 1), \\ Q(i - 1)Q(i - 2) \dots Q_1Q_0 = 00 \dots 00 \quad (14) \\ \Rightarrow Qi' = Qi + 2 \text{ (GF3)} \end{aligned}$$

$$Q0' = Q0 + 2 \text{ (GF3)} \quad (15)$$

Based on the rules in (14) and (15), the circuit structure of an n -trit down counter is shown in Fig. 9. The QC and Anc for an n -trit down counter are given in (16) and (17), respectively. The QC and Anc of an n -trit down counter is tabulated in Table VI for $n = 2, 3, 4, 5, 6, 7$. From (16) and (17), we see that the QC is incremented by $(n + 2) \times 6 - 7$ and the Anc is incremented by 2 for going from n to $(n + 1)$.

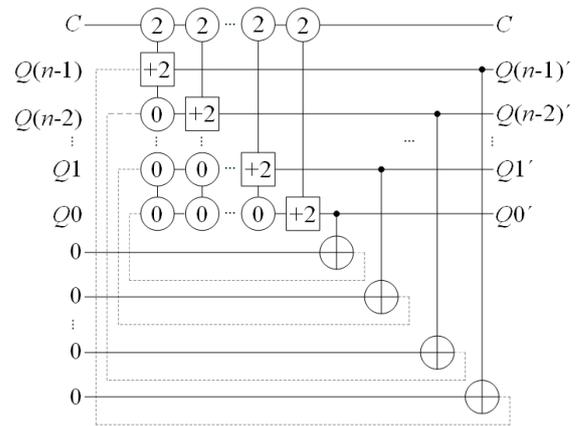

 Fig. 9. Realization of an n -trit down counter

TABLE VI
QC AND ANC OF OUR DESIGN OF AN n -TRIT DOWN COUNTER

n	QC	Anc
2	16	3
3	33	5
4	56	7
5	85	9
6	120	11
7	161	13

$$\begin{aligned} QC &= \sum_{i=3}^{(n+1)} \text{QC of } i\text{-trit multiple-controlled unary gate} \\ &\quad \text{with one 2 control and} \\ &\quad (i - 2) \text{ number of 0 controls} \\ &\quad + \text{QC of one controlled unary gate} \\ &\quad + n \times \text{QC of Feynman gate} \\ &= \sum_{i=3}^{(n+1)} (5 + (i - 3) \times 4 + 2 \times (i - 2)) + 1 + 4n \\ &= \sum_{i=3}^{(n+1)} (6i - 11) + 1 + 4n \end{aligned} \quad (16)$$

$$\begin{aligned} \text{Anc} &= \text{Anc for } (n + 1)\text{-trit multiple-controlled unary gate} \\ &\quad + \text{Number of Feynman gates} \\ &= (n + 1 - 2) + n \\ &= 2n - 1 \end{aligned} \quad (17)$$

V. SYNTHESIS OF TERNARY REVERSIBLE UP/DOWN COUNTERS

A ternary reversible up/down counter can be designed using multiplexing between up and down counters as shown in Fig. 10 for a 2-trit up/down counter. For multiplexing, another selection input S is added. When $S = 2$, then the gates of the Up Counter part of the circuit will be active and the gates of the Down Counter part of the circuit will be inactive, thus implementing an up counter. When $S = 0$, then the gates of the Up Counter part of the circuit will be

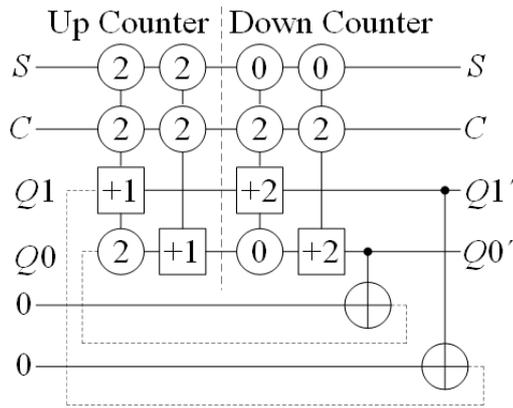


Fig. 10. Realization of a 2-trit up/down counter

inactive and the gates of the Down Counter part of the circuit will be active, thus implementing a down counter.

In a similar way, an n -trit up/down counter can be designed. The Up Counter part of an n -trit up/down counter requires n number of i -trit multiple-controlled unary gates with $i = 3, 4, \dots, (n+2)$, where all $(i-1)$ controls are 2. Similarly, the Down Counter part of an n -trit up/down counter requires n number of i -trit multiple-controlled unary gates with $i = 3, 4, \dots, (n+2)$, where one control for C is 2 and other $(i-2)$ controls are 0. The n -trit up/down counter requires n number of ternary Feynman gates. Thus, the QC of an n -trit up/down counter can be estimated as in (18). The Anc of an n -trit up/down counter can be estimated as in (19). The QC and Anc of an n -trit up/down counter is tabulated in Table VII for $n = 2, 3, 4, 5, 6, 7$. From (18) and (19), we see that the QC is incremented by $(n+3) \times 10 - 14$ and the Anc is incremented by 2 for going from n to $(n+1)$.

$$\begin{aligned}
 \text{QC} &= \sum_{i=3}^{(n+2)} \text{QC of } i\text{-trit multiple-controlled unary gate} \\
 &\quad \text{with all 2 controls} \\
 &+ \sum_{i=3}^{(n+2)} \text{QC of } i\text{-trit multiple-controlled unary gate} \\
 &\quad \text{with one 2 control and} \\
 &\quad (i-2) \text{ number of 0 controls} \\
 &+ n \times \text{QC of Feynman gate} \\
 &= \sum_{i=3}^{(n+2)} (5 + (i-3) \times 4 + 2 \times 0) \\
 &+ \sum_{i=3}^{(n+2)} (5 + (i-3) \times 4 + 2 \times (i-2)) + 4n \\
 &= \sum_{i=3}^{(n+2)} (10i - 18) + 4n
 \end{aligned} \tag{18}$$

$$\begin{aligned}
 \text{Anc} &= \text{Anc for } (n+2)\text{-trit multiple-controlled unary gate} \\
 &\quad + \text{Number of Feynman gates} \\
 &= (n+2-2) + n \\
 &= 2n
 \end{aligned} \tag{19}$$

 TABLE VII
 QC AND ANC OF OUR DESIGN OF AN n -TRIT UP/DOWN COUNTER

n	QC	Anc
2	42	4
3	78	6
4	124	8
5	180	10
6	246	12
7	256	14

VI. CONCLUSION

We have developed truth table based rules for ternary counters and then used those rules for synthesis of ternary reversible level-triggered synchronous up/down counters using ternary multiple-controlled unary gates, controlled unary gates, and Feynman gates.

We have presented rules for ternary up counters derived from truth tables and then based on those rules we have designed n -trit reversible up counters. Our design results for n -trit up counters have shown that our circuits require less Quantum Cost (QC) for $n = 2, 3, 4$, equal QC for $n = 5$, and moderately larger QC for $n > 5$ than those of the previous work in [31]. However, our circuits require much less Ancilla Inputs (Anc) for all n than those in [31]. Although we have assumed that our circuits can be implemented using any existing technology, most of the works in the literature usually refer to quantum realizations of reversible circuits. It is well known that, in quantum realizations, creating and maintaining large number of quantum states, which represent the inputs/outputs of the quantum circuit, is more difficult than creating large number of elementary quantum gates [34]. Thus, our circuits of ternary reversible up counters will be more favorable for quantum realizations than those in [31].

We have also presented rules for ternary down counters derived from truth tables and then based on those rules we have designed n -trit reversible down counters. The n -trit down counters require slightly more QCs than those of n -trit up counters. However, the number of Anc is same for both up and down counters.

Finally, we have designed n -trit up/down counters by multiplexing up and down counters. The up/down counters require moderately more QCs than the sum of QCs of corresponding up and down counters needed for the multiplexing. However, up/down counters require only one more Anc than that of corresponding up and down counters.

In general, our design approach is rule based and very easy to understand and implement. As the macro-level quaternary gates like Toffoli gates and Feynman gates are realizable using quaternary M-S and unary gates [33], [35], our future work will focus on realizing quaternary multiple-controlled unary gates using M-S and unary gates and then synthesizing quaternary reversible up/down counters using those gates.

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