A Link Performance Enhancer for Wireless E1 ATM links

Sasirekha GVK, Gangaraju KM

***Abstract*— Wireless radio links have a typical BER of 1 in 1000. In order to enhance the BER on such links, usage of error correcting code is essential. This paper describes a SOPC based architecture of a Link Performance Enhancer (LPE) meant to improve the Bit Error Rate of the Wireless links from 1 in 10^4 to 1 in 10^8. At its input LPE has been designed to accept the E1 data as per G.703 & G.704 standards while at the output the interface to the radio is as per G.703. Reed Solomon (RS) Forward Error Correction scheme of (*n, k*) of (255, 249) coupled with a novel Block Synchronization scheme for successful decoding, ensures performance improvement with a probability of false alarm of 1 in 10 days and probability of detection 0.9999.. with less than 2% bandwidth overhead.**

***Index Terms*—Asynchronous Transfer Mode (ATM), Bit Error Rate(BER) , System on Programmable Chip(SOPC)**

I. INTRODUCTION

A Link Performance Enhancer is described in this paper that allows the usage of commercial ATM switches in wireless environments, where the Bit Error Rates (BER) are typically of the order of 1 in 1000. It incorporates a Forward Error Correction scheme and a robust synchronization scheme that achieves a BER improvement from 10^{-4} to 10^{-8}. The proposed LPE works transparently in an existing communication link and therefore can be seamlessly integrated to a communication network. The system is designed as a System On Programmable Chip(SOPC) wherein the complete logic for cell level processing is implemented in a single Field Programmable Gate Array (FPGA). Figure 1 shows the typical usage scenario of the proposed LPE.

Some of the prior work in this regard can be found in [1] to [4]. In [1] authors describe Error protection for ATM-based wireless networking systems using Rate compatible Punctured Code (RCPC). [2] discusses protocol aided concatenated forward error control for wireless ATM using RS encoding/decoding at ATM Adaptation Layer (AAL). [3] describes a Reed-Solomon encoder/decoder ASIC for wireless ATM. [4] describes an error control scheme for tactical ATM which is applied at ATM layer. Though [4] describes implementation at AAL level, it involves complicated processing requiring segmentation & reassembly, common part convergence sub layer, service specific convergence sub layers for AAL1, AAL2, AAL5 etc. Implementation at ATM layer would allow a choice of FEC for payload only, header only, header + payload options. However, for multimedia applications the preferred choice would be to error protect both header and payload. Our objective is to propose a physical layer implementation in which the ATM cells are concatenated into data blocks for the encoding. This results in a simplified scheme.

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Sasirekha G V K, Gangaraju K M are scientists with Center for Artificial Intelligence and Robotics, Bangalore, India. (Phone no.91-080-25254288 ext.1201, Fax no.91-080-25244288, srekha@cair.drdo.in, g_raju@cair.drdo.in).

Towards this objective, we propose a "Link Performance Enhancer" including Block synchronization scheme for E1 ATM links with 1 in 10 day probability of false alarm and 0.9999.. probability of detection with <2% bandwidth overhead.

The organization of this paper is as follows. Section II gives a brief theoretical background on RS Codes. Section III describes the system architecture of the proposed LPE. Section IV presents the results and analysis. Finally, our conclusions are presented in Section V.

II. THEORETICAL BACKGROUND ON RS CODING

Reed-Solomon (RS) codes are *non-binary cyclic* codes with symbols made up of *m*-bit sequences, where *m* is any positive integer having a value greater than 2. RS (*n, k*) codes on *m*-bit symbols exist for all *n* and *k* for which

$$0 < k < n < 2m + 2$$

where *k* is the number of data symbols being encoded, and *n* is the total number of code symbols in the encoded block (refer [5], [6] for details). For the most conventional RS (*n*, *k*) code,

$$(n,k) = (2^m - 1, 2^m - 1 - 2t)$$

where *t* is the symbol-error correcting capability of the code, and $n - k = 2t$ is the number of parity symbols.

Figure 2 shows the input error rate to output error rate improvement for various redundancy values. We propose a symbol size of 8 bits thus restricting the block size to 255 symbols (bytes). With this choice, the LPE provides a Bit Error Rate improvement from 10^{-4} to 10^{-8} or better. The selected Error Correction Code (255, 249) with t = 3 satisfies this requirement.

A mechanism is needed for identification of block boundaries. For this we propose a unique synchronization pattern to be prefixed to each block before transmitting. The receiver logic can hunt for this pattern and find the block boundaries. This is described in detail in Section III A.

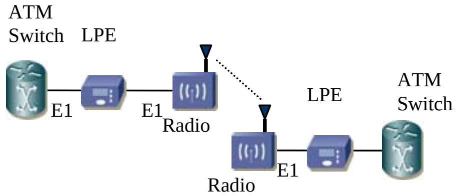

Figure 1: usage scenario of the proposed LPE

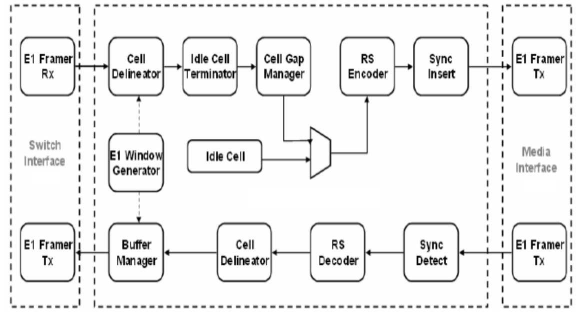

Figure 3: Block diagram of LPE

III. DESCRIPTION OF THE ARCHITECTURE OF THE PROPOSED LPE

The Figure 3 shows the internal blocks of the proposed LPE. In the forward path, the E1 frames from an ATM switch received by the switch interfaces are de-multiplexed after the detection of the frame sync slot. The data from the 30 user slots of E1 frame is collected. The collected data is then encoded by a RS-encoder (255,249) to form 255 byte blocks. For every 6 consecutive blocks, 6 bytes of block synchronization information is inserted. The data is then sent to media interface for onward transmission.

In the receive path, block boundaries are identified by the Sync Detect logic. Sync Detect logic gives the required block alignment marker. The aligned block of data is then decoded. This data is then transmitted via switch interface card. The design details of the Block Synchronization mechanism are presented following subsections.

A. Block Synchronization design issues

The design of the synchronization involves the addressing twin issues. They are:

(a) Selection of the length of unique word

(b) Selection of frequency of transmission of unique word

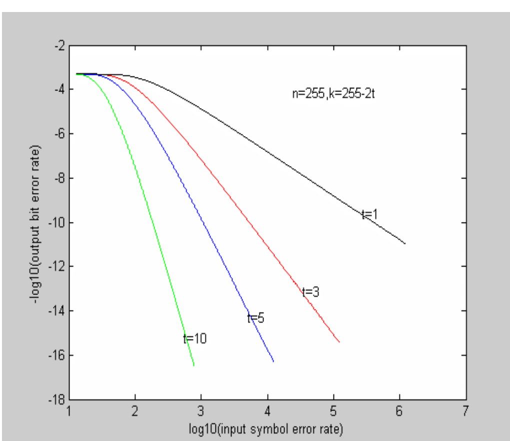

Figure 2. Input symbol error rate Vs. Output bit error rate

Table I indicates the probability of detection P_d for different unique word lengths n in bits. The entries in the Table I are generated using the formula given below

$$P_d = \sum_{i=0}^{t} {}^{48}C_i \, P_e^{\,i} (1-P_e)^{48-i}$$

Where t is the error tolerance threshold and P_e is the probability of error of the channel.

P_d for BER of 1 in 10^2 and for $t = 0$

$$P_d = (1-P_e)^{48} = (1-0.01)^{48} = 0.61729014$$

While for a $t = 1$:

$$P_d = 48 \, P_e \, (1-P_e)^{47} + 0.61729014$$

It may be observed from Table I that the probability of missing sync is

= (1 - 0.9999914) = 0.0000086 = 8.6 x 10^{-6} or 1 in 116279.

B. Calculation of bandwidth overhead in the proposed scheme

The E1 frame format has 30 data slots + 1 frame sync slot + 1 signaling slot. The frame sync information is not required over the wireless link as block sync provides the necessary data boundaries. It is required by the receive E1 ATM interface where it can be reinserted. Signaling in E1 ATM is in the form of AAL5 Protocol Data Units carried as ATM cells. Therefore, a payload reduction of 2 bytes is achieved for every 32 bytes. This as a ratio is 2/32 = 1/16. As mentioned earlier, the RS encoding scheme of (255, 249) requires an overhead of 6 bytes for every 249 bytes of data. If we transmit block sync pattern of 6 bytes for every 6 blocks, the total overhead would be 6x 6 + 6 ie 42 bytes.

Table I: Probability of Detection

T	n=32	N=48	n=64
0	0.72498033	0.61729014	0.52559648
1	0.95931741	0.91658233	0.86537603
2	0.99600655	0.98762643	0.97348770
3	0.99971252	0.99862990	0.99605647
4	0.99998392	0.99988029	0.99953297
5	0.99999927	**0.99999144**	0.99995437

This as a ratio is 42/(249 x 6) = 1/35 approx. Thus it is seen that the payload reduction is greater than the overhead required.

C. *Calculation of probability of occurrence of false alarm*

The Probability of False alarm P_f can be calculated using the formula

$$P_f = \frac{1}{2^n} \sum_{i=0}^{t} {}^{i}C_n$$

Table II shows the probability of false alarm. Further, Let T = 488.28 * 10^(-9) *ie.* E1 data rate N = 255*8*6; ie one sync word sent for every 6 encoded blocks where each encoded block is 255 bytes *ie*. 255 x 8 bits.

$$x = 1/P_f$$

$$D = ((T*N)/x)/(24*60*60)$$

where D is the no. of days within which 1 false alarm can occur. Therefore, for the chosen unique word length of 48 bits and the frequency of transmission of once for every 6 blocks of 255 bytes, D is 10 days .Table III shows the number of days per false alarm.

D. *Implementation details*

The proposed LPE was implemented using a System On Programmable Chip approach on an Alterra Cyclone II device.

The RS encoder/decoder '*megafunction*' was an intellectual property of ALTERA. This has an advantage of quick prototyping, flexibility to make it adaptive, and also facilitates easy translation to a structured ASIC.

Table II: Probability of false alarm

t	n=32	n=48	n=64
0	2.3283e-010	3.5527e-015	5.4210e-020
1	7.6834e-009	1.74082970e-013	3.5236e-018
2	1.2316e-007	4.18154399e-012	1.1281e-016
3	1.2780e-006	6.56292797e-011	2.3714e-015
4	9.6505e-006	7.56916307e-010	3.6815e-014
5	5.6537e-005	6.84024215e-009	4.5014e-013

Table III: Number of days per false alarm.

t	n=32	n=48	n=64
1	9.0029	3.9736e+005	1.9631e+010
2	0.5616	1.6542e+004	6.1317e+008
3	0.0541	1.0540e+003	2.9169e+007
4	0.0072	91.3879	1.8789e+006
5	0.0013	**10.1127**	1.8789e+006

IV. THEORETICAL ANALYSIS AND COMPARISON OF RESULTS

This section presents the theoretical calculations, experimental setups and the observed measurements.

A. *Theoretical Calculations:*

Cell Error Rate (CER) corresponding to the required Bit Error Ratio (BER) was calculated. This is required since the standard tests (O.191) give only the CER.

A Cell Error is declared when one or more bits in the ATM payload gets corrupted. Payload corruption is detected using CRC in O.191 tests.

$$CER = \sum_{i=1}^{n} \left\{ {}^{384}C_i P_e^{\,i} \left(1 - P_e\right)^{384-i} \right\}$$

$n = 384$ (ATM Payload size)

$P_e =$ Probability of bit-error

Calculated CERs corresponding to the required BERs are given in Table IV.

B. *Experimental Setups*

Performance tests were carried out to determine the BER improvement and latency under various traffic load conditions. The test setup employed for this purpose is shown in Figure 4. Referring to Figure 4, a Network Analyzer was used to generate and monitor ATM E1 traffic. ITU-T O.191 tests were carried out to find various error parameters and the latency. Channel Simulator was used to emulate the radio link characteristics in the laboratory settings.

In another setup (with ATM Cell hardener) , where in the Switch Interface was connected to the network analyzer and the Media Interface connected to the Channel Simulator (shown in Figures 5 and 6), Full Duplex and Half Duplex testing were performed out.

The following tests were carried out to evaluate the performance of the ATM Cell Hardener:

- BER improvement testing: Measures BER improvements for various input BERs.
- Load testing: Measures the system's ability to handle various types of traffic loads.

Table IV: BER Vs. CER

BER	CER
10^{-3}	0.31899942
10^{-8}	3.8399926×10^{-6}

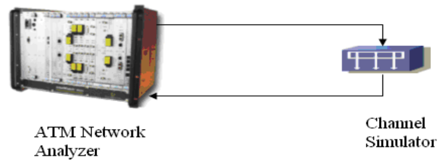

Figure 4: Channel Simulator test setup

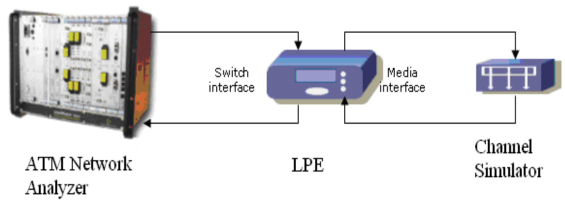

Figure 5: Performance test setup with media loop back

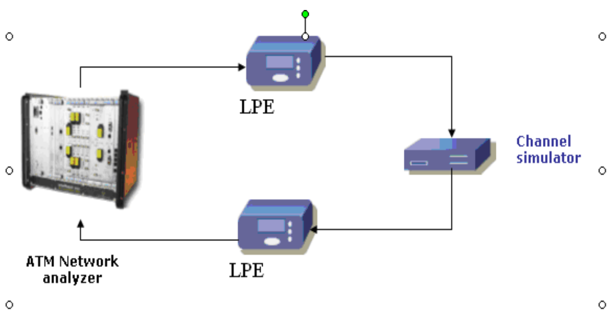

Figure 6: Performance test setup with channel simulator

- Latency testing: Measures the round trip latency of the transmission path.
- Volume testing: Subjects the system to larger amounts of data to determine its point of failure

The settings of the parameters were as follows

Traffic Profile

- Type: CBR
- Start Idle: 0
- Period: 0
- Utilization: 50
- Bandwidth: 0.959999

Block Size

- 16384

ATM QoS Test was run for various time intervals in setup with and without cell hardener. The following error-related network performance parameters (defined in Recommendations I.356) were measured:

- Cell Error Ratio
- Cell Loss Ratio
- Severely Errored Cell Block Ratio
- Cell Mis-insertion Rate

Table V: Performance test results

BER	**Observed CER**				**Calculated CER**
	2 mins	5 mins	10 mins	20 mins	
10^{-3}	0.3166	0.3161	0.3163	0.3156	0.3189
10^{-8}	4.08×10^{-6}	9.17×10^{-6}	7.449×10^{-6}	5.94×10^{-6}	3.84×10^{-6}

C. Results

The results obtained are tabulated below. The Cell Error Ratio observed in all the four experiments and the values obtained by analysis are tabulated in Table V. The measured values of CER matched with the theoretical calculations.(Tables IV and V) of the results.

V. CONCLUSIONS

A scenario which necesstiates usage of Link Performance Enhancer (LPE) has been presented. A design of the LPE was implemented, tested and evaluated for its performance. The results obtained are in agreement with the theoretical analysis thus validating our design.

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