Co-Ordination of SVC and on Load Tap Changing Transformer for Reactive Power Control in Power Systems

E. Vidyasagar, N. Ramu and A. Prasad Raju

Abstract—**The static var compensator (SVC) has fast response characteristic and can hold system voltage at near rated value following disturbances providing reactive power reserve with a SVC is essential to provide reactive power requirements during system disturbances. This paper presents a new SVC control strategy with two of regulation slopes Will be discussed. The control holds the voltage between a prescribed range. The aim of this control is to limit the reactive power output from the SVC with in the desired value during the steady-state operation. It would compensate the reactive power requirement from the upstream networks with the under-load tap changer (ULTC).When the voltage deviates from the steady-state voltage range, due to a disturbance the SVC will react to support the system voltage. When a disturbance results in a new operating point, with a steady-state reactive-power output, the variable voltage reference control effectively changes the SVC output slowly and returns it within the steady-state margin.**

Index Terms— **Coordinated control, static var compensator (SVC), under-load tap changer (ULTC) SVC, variable reference control.**

I. Introduction

Now a days, SVC is one of the key elements in the power system that provides the opportunity to improve power quality and reliability due to its fastness. SVC has the functional capability to handle dynamic conditions, such as transient It is common to install a ULTC (Under Load Tap Changer) at the distribution substation to regulate load voltage against the variation of load demand. Although components of the ULTC control system are simple devices, its overall system is complex due to the presence of nonlinearity such as time delay, dead band, etc. When both SVC and other slow response voltage regulators [e.g., under-load tap changers (ULTCs)] are used to control system voltage, the SVC reacts to the voltage deviation faster than the ULTC. If the SVC output reaches the maximum capacity limit, it loses active control and behaves similar to a shunt capacitor bank. The SVC output may reach its maximum output due to the steady-state load increase or system disturbance.

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This paper proposes the coordinated control system between the SVC and ULTC of the distribution substation. This control reserves the SVC operating margin without increasing the tap position; however, the resetting of SVC output reactive power has not been taken into consideration, the objective of this new proposed SVC control strategy is to limit the steady-state reactive-power output of the SVC to a desired value during the steady-state voltage range. However, the SVC changes output rapidly to counteract transient disturbances by the remaining reserve margin. When a disturbance results in a new operating point with a steady var output, the variable reference voltage control effectively changes the voltage reference value and thereby activates slow voltage regulators to return back for operation within the steady-state margin stability and power oscillation damping in addition to providing voltage regulation.

II. CONVENTIONAL SVC V-I CHARACTERISTICS

They are defined by the slope reactance when the controlled voltage is within the control range.

The conventional SVC V-I Characteristics

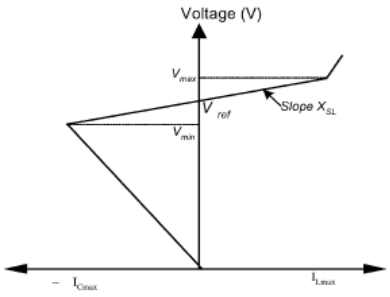


Fig 1: conventional svc v-I characteristics

The V-I characteristics are described by the following three equations:

Within control range ($-I_{cmax} \le Isvc \le I_{Lmax}$)

$$V = V_{ref} - X_{sL} I_{svc} \quad (1)$$

When $V<V_{min}$, the SVC will reach its capacitive limit

$$B = -B_{cmax} \quad (2)$$

When $I_{svc}>I_{Lmax}$, the SVC will reach its inductive limit

$$B = B_{Lmax} \quad (3)$$

PROPOSED SVC V-I CHARACTERISTICS

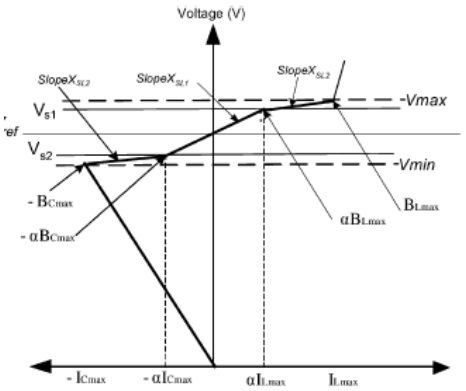


Fig 2: Proposed SVC V-I characteristics

The proposed SVC V-I characteristics are shown in Fig. 2. They are defined by the two-regulation slopes $X_{sL1}$and X_{sL2}

$$X_{sL1} = (V_{s1}-V_{ref})/\alpha I_{Lmax} = (V_{s2}-V_{ref})/-\alpha I_{cmax} \quad (4)$$

$$X_{sL2} = (V_{max}-V_{s1})/(1-\alpha)I_{Lmax} = (V_{min}-V_{s2})/(1-\alpha)I_{cmax} \quad (5)$$

The proposed V-I characteristics are described by the following three equations within the steady-state margin ($-I_{cmax} \le Isvc \le I_{Lmax}$)

$$V = V_{ref} - X_{sL} I_{svc} \quad (6)$$

when $V=V_{s2}$, the SVC will reach its steady-state capacitive limit

$$B= - \alpha B_{cmax} \quad (7)$$

when $V=V_{s1}$, the SVC will reach its steady-state inductive limit

$$B= - \alpha B_{Lmax} \quad (8)$$

The SVC output is limited to the desired steady-state margin as the controlled voltage reaches its switching points (steady-state voltage range).

The V-I characteristics are described by the following four equations outside the steady-state margin:

Within the control range ($\alpha I_{Lmax} \le I_{svc} \le I_{Lmax}$)

$$V = V_{s1} - X_{sL2} (I_{svc} - \alpha I_{Lmax}) \quad (9)$$

Within the control range ($\alpha I_{cmax} \le I_{svc} \le I_{cmax}$)

$$V = V_{s2} - X_{sL2} (I_{svc} + \alpha I_{cmax}) \quad (10)$$

When $V<V_{min}$, the SVC will reach its capacitive limit

$$B= -B_{cmax} \quad (11)$$

When $Isvc > I_{Lmax}$, the SVC will reach its inductive limit

$$B= B_{Lmax} \quad (12)$$

III. PROPOSED SVC CONTROLLER

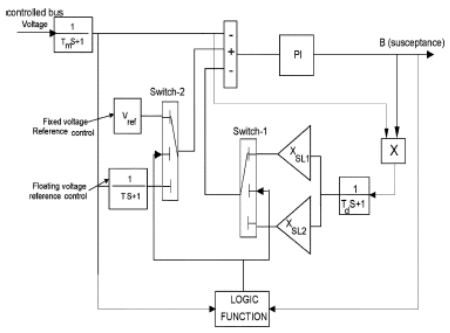


fig 3 : Proposed SVC controller

Proposed SVC Controller System

The proposed controller of the SVC is shown in Fig. 3. Two switches are used. Switch-1 is used to changeover the regulation slope X_{sL1} to X_{sL2} , and switch-2 is used to changeover the fixed-voltage reference control to variable (floating) voltage reference control.

The fixed-voltage reference control is used to regulate the voltage within the steady-state margin. When the controlled voltage crosses out the switching points (steady-state voltage range), the floating-voltage reference control is utilized to rapidly regulate the voltage and slowly return the SVC output back to the steady-state margin

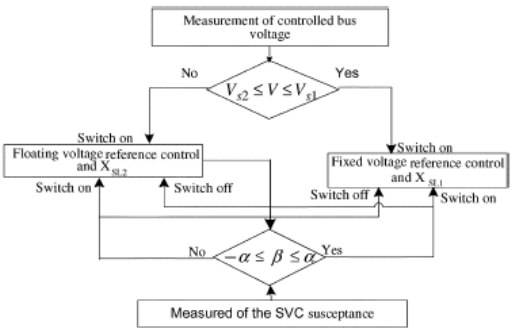


Fig 4: Flow chart for proposed control logic function

The output of the logic function, shown in Fig. 4, mainly aims to switch between the fixed-voltage reference control with regulation slope X_{sL1} and X_{sL2} the floating-voltage reference control with regulation slope as follows.

1. When the controlled-bus voltage is within the desired SVC switching points (V_{S1}, Vs2), the fixed-voltage reference control with the slope is switched on.
2. When the controlled-bus voltage crosses out the desired switching points, the floating-voltage reference control with the X_{sL2} slope is switched on.
3. The changeover from the floating-voltage reference control X_{sL2} with to a fixed-voltage reference control with X_{sL1} is utilized when the SVC output is returned back to the steady-state margin. The switch mechanism from the floating-voltage reference control to a fixed-voltage reference control may change according to the criteria of power system design.

Variable (Floating) Voltage Reference Control

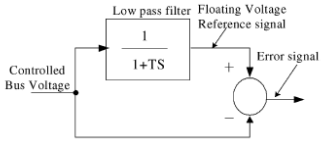


Fig 5: Floating voltage reference control

The floating-voltage reference signal is a low-pass filter with an initial output (setting value). The input signal to the low-path filter is the controlled-bus voltage to which the SVC is connected. Fig. 5 shows the proposed floating-voltage reference control.

When the input signal of the low-pass filter changes rather fast and takes time less than the time constant T of the low-pass filter, the output of the low-pass filter does not change despite its input signal. Therefore, the SVC output reacts against the fast voltage change. Initially, the error signal rises very quickly to be equal Initial error signal = $LPF_{IO} - V_{controlled\ bus}$ Where LPF_{IO} is the initial output value of the low-pass filter (setting value). Consequently, the output of the low-pass filter is going to rise and the error signal is going to return slowly. Therefore, the floating voltage reference control does not try to hold the steady-state system voltage just prior to switching the floating-voltage reference control. It reacts initially to hold the initial output of the low-path filter, which is a setting value. When the input signal of the low-pass filter changes slowly, and takes time longer than the time constant T of the low-pass filter, the output of the low-pass filter changes in accordance with its input signal. This is the reason why the signal is called the floating-voltage reference. Therefore, the error signal to the SVC output controller is 0 and the SVC output does not react against the slow voltage change only within the resetting time Fig. 6 shows the change in the low path filter output and also the change in the error signal to step change in the input signal (0.02 p.u.). The initial output of the low-path filter is equal to 1.0 p.u. This step change simulates the signal rises by the switching mechanism from the fixed-voltage reference control to the floating-voltage reference control.

It is clearly seen that the error signal rises very quickly, and initially equals 0.02 p.u. Because the output of the low-pass filter is going to rise, the error signal is going to return slowly. As the output of low-pass filter reaches its saturated value (1.02 p.u.),the error signal also reaches zero.

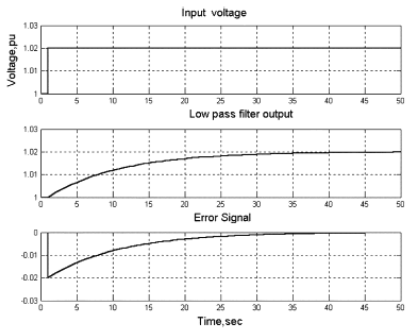


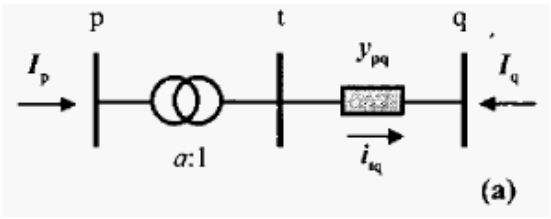
Fig 6: step response test of the floating – voltage reference control

Under load tap changer:

Most power systems are nowadays operated very near to their operating limits due to increase in consumption, while economic and environmental constraints have limited construction of new generation facilities and lines. Usually substations are provided with transformers with tap-changers facilities. It was long believed that transformers with tap changers could eliminate or minimize effectively voltage instabilities

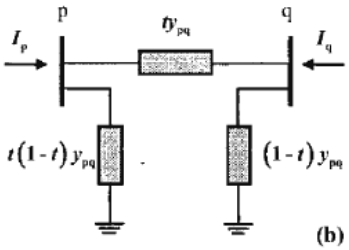
ULTC MODELLING

A transformer with off nominal turn ratios can be represented by its admittance or (impedance), connected in series with an ideal auto transformer as shown in Figure**.**



Equivalent circuit of ULTC model

An equivalent ∏ circuit can be obtained from this representation to be used in power flow studies and voltage stability analysis, and the elements of the equivalent *II* circuit, can be treated in the same manner *as* line elements. The parameters of the equivalent *II* circuit are presented in Figure.



Equivalent ∏ circuit of ULTC model with parameters In the equivalent л circuit of ULTC *t* is off-nominal tap-ratio and is given by*(t=1/a)a*nd *a* is the turns ratio of the ideal equivalent auto transformer , At normal transformer tapping, the ratio *a* tends to unite and consequently the transformer model turns to its series admittance Y_{pq}**.** The two shunt elements are neglected.

IV. COORDINATION BETWEEN PROPOSED SVC AND ULTC:

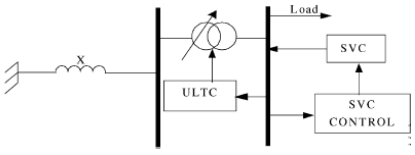


Fig 7: power system model

When the bus voltage is controlled concurrently by a conventional SVC control and ULTC, both having completely different time-response scales, the SVC reacts to the voltage deviations before ULTC. consequently, when the SVC output reaches the maximum capacity limit during the steady-state voltage variation, the SVC loses its functionality during the dynamic voltage variation. The newly proposed SVC control, against the conventional SVC control having a different time response than ULTC, would improve the coordination with ULTC by adapting the following settings.

1) *The SVC reference voltage has to be equal to the ULTC reference voltage.*

2) *The switching points V_{s1} (and) V_{s2} have to be outside the specified dead band of the ULTC.*

As a result of utilizing these settings, the following occurs.

1) When the controlled-bus voltage crosses out the ULTC dead band but is still within the SVC switching points for time equal to the ULTC time delay, the tap changes.
2) The number of the tap movements depends on the margins between the ULTC dead band and The SVC switching points

V. SIMULATION RESULTS

Three numerical simulation cases are studied to verify the effects of the proposed SVC control using system model shown in Fig. 7 and the following typical parameter values:

transmission-line impedance : 185 p.u.;
SVC control range : BLmax =1.0 p.u.
Bcmax = -1 p.u

steady-state stability margin : α = 0.2 p.u.;
upper-point switching voltage : 1.03 p.u.;
lower-point switching voltage : 0.97 p.u.;
V_{max} = 1.05 p.u.
V_{min} =0.95 p.u.

from equations 4 and 5 : XsL1 = 0.15 p.u.
XsL2= 0.025 p.u.

ULTC transformer data:
Turns ratio step : 0.017 p.u.;
Number of taps : 21;
Time delay : 15 s;
Motor time delay : 5 s;
Regulator dead band : 0.02 p.u.;

Case 1: Comparison Between the Conventional and Proposed SVC Control in the Steady-State

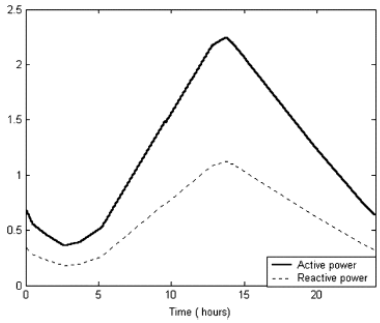


Fig 8 : Proposed daily load curve

The proposed periodic load data shown in Fig. 8 are utilized to compare the coordination of both conventional and proposed SVC control with ULTC in the steady-state.

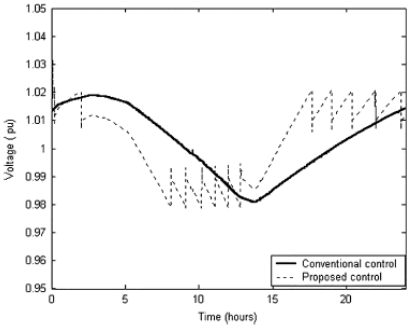


Fig 9: Steady – state controlled –bus voltage change

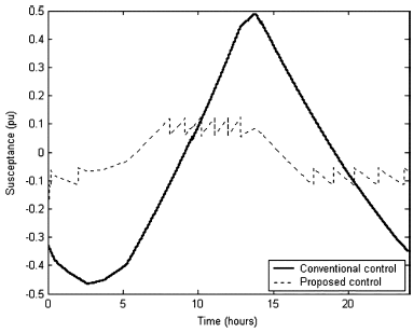


Fig 10 : steady – state SVC suseptance

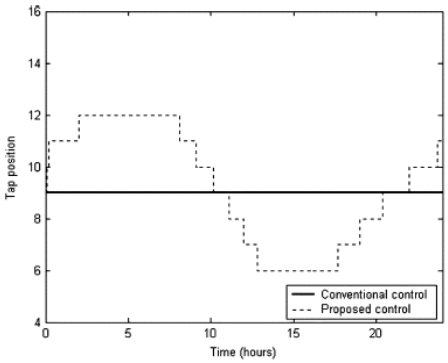


Fig 11: steady – state tap movements

Figs. 9–11 show the changes of the controlled bus voltage, the SVC susceptance, and the tap movements. Table I shows the summary of the simulation results the summary of the simulation results.

TABLE I
SUMMARY OF CASE-1 SIMULATION

Control method	Max. SVC output, pu	Min. SVC output, pu	No. of tap movements
Conventional control system	0.5	-0.45	0
Proposed control system	0.11	-0.1	13

1) *For the proposed SVC control, the SVC output remains within the desired steady-state margin (0.2 p.u.), and the voltage regulation is shared between the SVC and ULTC.*

2) In the case of the conventional control system, the SVC output reaches 0.5 p.u. and the tap does not change

Case 2: Effect of Changing the Switching Points (Vs1and Vs2) on the Number of ULTC Movements

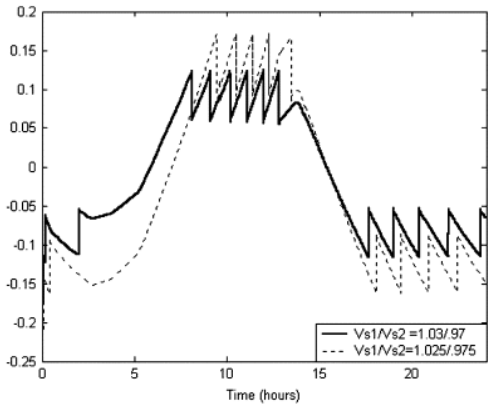


Fig 12 : SVC suseptance change

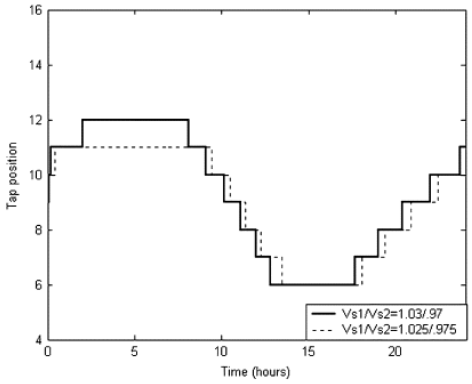


Fig 13 : Tap Movements

The upper and lower switching points V_{s1} and V_{s2} , respectively, are changed from 1.03 p.u. and 0.97 p.u. to 1.025 p.u. and 0.975 p.u. The consequent effects on the maximum and minimum SVC susceptance and the number of tap movements are illustrated in Figs. 12 and 13.

It is concluded from Table II that the reduction of the margins between the ULTC dead band and the SVC switching points results in minimizing the number of the tap movements while the SVC susceptance increases but is still within the steady-state margin.

TABLE II
SUMMARY OF CASE-2 SIMULATION

Vs1/Vs2	Max. SVC output, pu	Min. SVC output, pu	No. of tap movements
1.03/.97	0.11	-0.1	13
1.025/.975	0.17	-0.15	11

Case 3: Mechanism of Restoring the SVC Reserve Margin: In this case, the simulation of the load injection results in the controlled-bus voltage decrease to 0.966 p.u. behind the lower switching point (V_{s2}=0.97) . Accordingly, the SVC control is switched from the fixed-voltage reference control with regulation slope (X_{sL1}=0.15 p.u.) to the floating-voltage reference control with regulation slope (XsL2=0.025 p.u.).

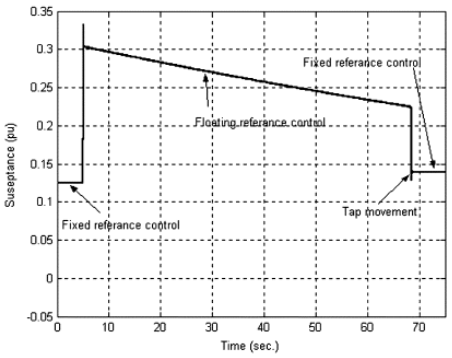


Fig 14 :SVC susceptance change

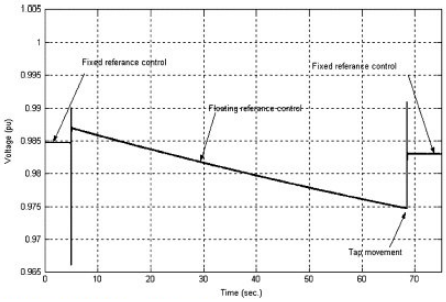


Fig. 15. Controlled-bus voltage change.

Figs. 14 and 15 show the change stages of both voltage and susceptance starting from the predisturbance steady-state condition up to the new operating point within the steady-state margin as follows:

Stage-1 Predisturbance Steady-State: The SVC susceptance is within the steady-state margin (0.125 p.u.) and the voltage of the controlled bus is 0.985 p.u. The SVC is controlled by the fixed-voltage reference.

Stage-2 Control Switching Following Load Injection: When the controlled-bus voltage crosses out the lower switching point (0.97 p.u.) due to load injection, the changeover from fixed-voltage reference control with regulation slope (X_{sL1}=0.15 p.u .) to the floating-voltage reference control with regulation slope (XsL2=0.025 p.u.) is utilized. Consequently, the SVC responds very fast to the voltage variation due to the quick rise of the error signal. As the SVC susceptance changes from 0.125 to 0.33 p.u. thereby, the voltage changes from 0.966 to 0.99 p.u. in 100 ms.

Stage-3 Coordination of SVC and ULTC: As the output of the low-pass filter is going to rise, the error signal returns slowly; consequently, the SVC susceptance and the voltage are reduced slowly. When the voltage crosses out the ULTC dead band (±0.02) for time equal to 20 s, the tap changes.

4) Stage-4 Resetting SVC Reserve Margin: As a result of the tap change, the SVC susceptance changes from 0.22 to 0.14 p.u., which is within the steady-state margin; thereby, the SVC controller Changeover is from the floating-voltage reference controller to the fixed-voltage reference control.

VI. CONCLUSION

A newly proposed SVC control strategy is realized by using two regulation slopes and a combination of the fixed-voltage

reference control and floating-voltage reference control which has the following advantages:

1) *limiting the SVC output during the steady-state to the* desired range;
2) better coordination between the SVC and slow-response automatic voltage regulators, such as the ULTC;
3) resetting the SVC after disturbance to be within the steady-state margin.

NOMENCLATURE

$_{BLm}$ maximum SVC inductive susceptance,
B_{Cma} maximum SVC capacitive susceptance,
I_{Lmax} maximum SVC inductive current,
I_{cmax} maximum SVC capacitive current
I_{svc} SVC compensation current;
T_m Time constant of voltage measurement System in sec
T_d average time delay due to thyristor valves firing in sec
T low-pass filter time constant in sec
V voltage of the controlled bus;
V_{ref} reference voltage magnitude of SVC;
V_{s1} desired upper switching point
V_{s2} desired lower switching point
X_{sL} regulation slope;
α steady-state operating margin in per unit;

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