

A Novel Argument to Use 8-BIT Media Processor for Low Power VLSI Design

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ABSTRACT: A novel idea pertaining to the selection of a processor size for low power IC applications has been proposed. 8-bit processors were introduced in the beginning by Intel. Later, technology has rapidly advanced forcing the designers to go for 32-bit and 64-bit processors for edge cutting, high performance technologies. In this paper, it has been proposed that an 8 bit media processor can perform the same applications that the others do, at reduced power consumption and hence is more advantageous than other processor sizes. The main concept of the paper is that, once a VHDL or a Verilog code is designed for any media processing application, its Xilinx synthesis report is converted to transistor level net list by careful observation. This transistor level net list is implemented in Tanner Tools EDA and the power can be easily calculated. By this method, the experimental results have proved that 8-bit processor consumes less power than others and hence can be used in place of 16-bit and 32-bit processor chips.

Index Terms: Low Power, Media Processor, 8-Bit Processor, Synthesis Report, Tanner Tools, Power Calculation

I. INTRODUCTION

Low power has always been the main and foremost goal of any chip designer. When the chip is designed for a particular application, a Hardware Description Language Code is first written which can be dumped into the IC, which then works as per the designed application. Then the IC works as per the designed application. Before dumping the code into the IC, it has to be ensured that the code which was designed consumes the least amount of power and least memory [5]. It should also be ensured that there are no hot-spots which would otherwise cause uneven distribution of heat

There are many methods to find the power consumption of a VHDL or a Verilog code. Some of the software's are Synopsis and Mentor Graphics. Tanner Tools is an Electronic Automation Tool, which provides a schematic design entry, whose power [7] can be calculated. It is simple and can be downloaded easily through the internet.

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A. Media encryption processors at the chip level

Media processing has seen the most rapid development in recent years, especially in media encryption for data security. Hence media processors [1] are now being designed at the chip level on a large scale. 8-bit processors were introduced in the beginning by Intel. Later, technology has rapidly advanced forcing the designers to go for 32-bit and 64-bit processors for edge cutting, high performance [6] media technologies [4].

This paper proposes that an 8 bit media processor [3] can perform the same applications that the others do, at reduced power consumption and hence is much more advantageous than other processor sizes.

The proposal of this paper is that once a VHDL or a Verilog code is designed for any media processing [8] application, its Xilinx synthesis report is converted to transistor level net list by careful observation. This transistor level net list is implemented in Tanner Tools EDA and the power can be easily calculated. Our results have shown that an 8-bit processor consumes lesser power, while performing the same functions and hence highly efficient than the other processor sizes.

II. PROBLEM FORMULATION

32-bit and 16-bit processors are used these days to lure people towards high technology [2] and edge cutting media applications. But these processors consume high amount of power. Even though software's like Mentor Graphics Synopsis are available to find the power consumption of a VHDL or a Verilog Code, they are very costly and cannot be readily available for a normal student for his research. Hence this paper aims to bring out an argument that 8 bit processor can be used instead and it consumes less amount of power than the others. An easy method of power calculation is also introduced.

III. METHODOLOGY OF THE PAPER

➤ An 8 bit audio and a 16 bit video data in binary form are the incoming signals. The media processor has to reconfigure itself to the incoming bit stream and invert the bits and send them.

➤ Firstly, the Verilog code is designed on a 8 bit chip, for the simple application, operating on customized word-length audio and video data. The main concept is that all operations take place on 8 bit signals and 8 bit buses.

IV. EXPERIMENTAL RESULTS

- ❖ The 16 bit audio data is handled by two separate 8 bit data path's in this case.
- ❖ The 8 bit video data is handled directly.

➤ Secondly, the Verilog code is designed on a 16 bit chip, for the simple application, operating on customized word-length audio and video data. The main concept is that all operations take place on 16 bit signals and busses.

- ❖ The 16 bit audio data is handled directly.
- ❖ For the 8 bit video data, 8 bits of a data-path are used and the rest are used for other purposes like carrying control signals.

➤ Thirdly, the Verilog code is designed on a 32 bit chip, for the simple application, operating on customized word-length audio and video data. The main concept is that all operations take place on 32 bit signals and busses.

- ❖ Both 8 bit video and 16 bit audio are handled by 32 bit busses, the free bits are used for control purposes.

➤ The synthesis reports of all the three codes are studied carefully and their corresponding transistor level net lists are drawn.

➤ These transistor level net lists are implemented in Tanner Tool EDA and the schematic entry is done for all the three codes.

➤ Once the schematic entry is done the T-Spice is run which will give the net-list. The power consumption for each circuit is calculated by the command

```
.model pmos pmos  
.model nmos nmos  
.tran 4n 400n  
.print p( / output node number / )
```

➤ Converting the net lists into circuit level entry

This is done by designing a Verilog program for a simple DSP application of 'Inversion of bits' on an 8 bit, 16 bit and a 32 bit processor assuming that the incoming audio signal is of 16 bits and video signal is of 8 bit length and converting the Xilinx synthesis report to transistor level net list and implementing it in Tanner tool and hence select which processor size gives low power. Experimental results show that an 8 bit processor consumes less power than the others.

The application selected in this paper is related to media processing. We consider an 8 bit video and a 16 bit audio digital data coming together. Normally, sound travels faster than video. Hence audio data reaches the processor first. Once the processor detects the audio data, it starts operating on the data. A simple media operation "Inversion of the bits" is taken in our application. Once video signal is received, the processor has to switch immediately to the video and perform both audio and video inversion simultaneously. Once a particular data stops, the processor has to use its free resources to service the other data.

The main concept that has been introduced in the coding was that the 8 bit processor handles the 8 bit video data directly. The 16 bit audio data is handled by two 8 bit data paths. It has been thus proved that 8 bit processor can be used for the same high-end media operations with the added advantage that it consumes less amount of power. Hence the paper makes an argument that instead of using higher processor sizes, 8 bit processor could be used to perform 16 or even higher bit operations as any other processor size with efficiency and reduced power consumption.

This code is designed for an 8 bit, 16 bit and a 32 bit chip separately and the corresponding tanner implementations for 8 bit, 16 bit and 32 bit processor are shown in Figure.1, Figure.2, and Figure.3 respectively. Also the power consumption waveforms for 8 bit, 16 bit and 32 bit processor is shown in Figure.4, Figure.5, Figure.6 respectively and the comparison results are shown in Table.1.

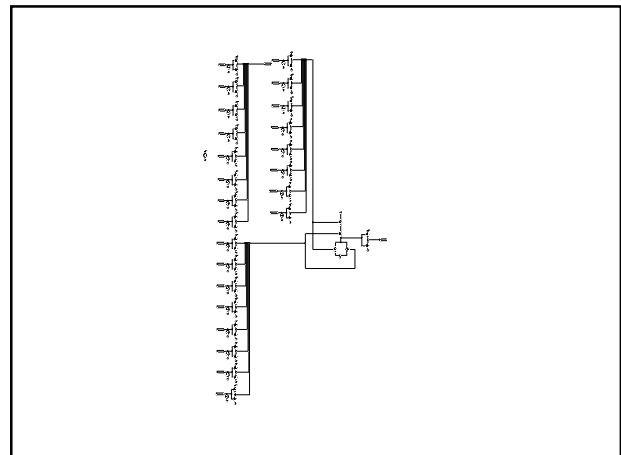


Figure 1. Tanner implementation for an 8 bit processor inverting the 8 bit video and 16 bit audio data

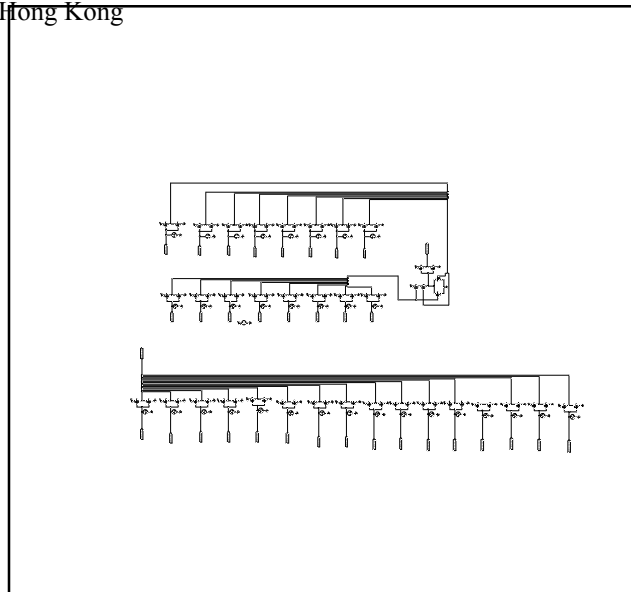


Figure 2. Tanner implementation for a 16 bit processor inverting the 8 bit video and 16 bit audio data

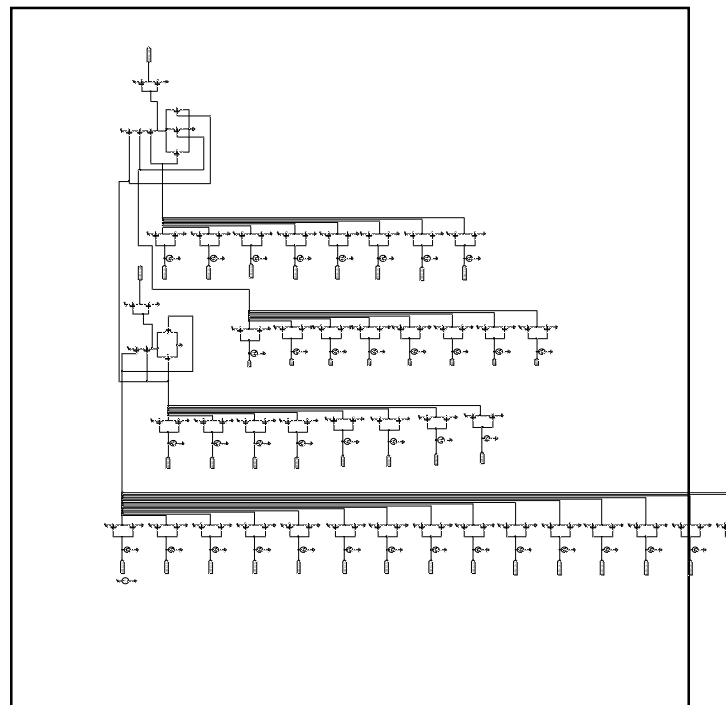


Figure 3. Tanner implementation for a 32 bit processor inverting the 8 bit video and 16 bit audio data

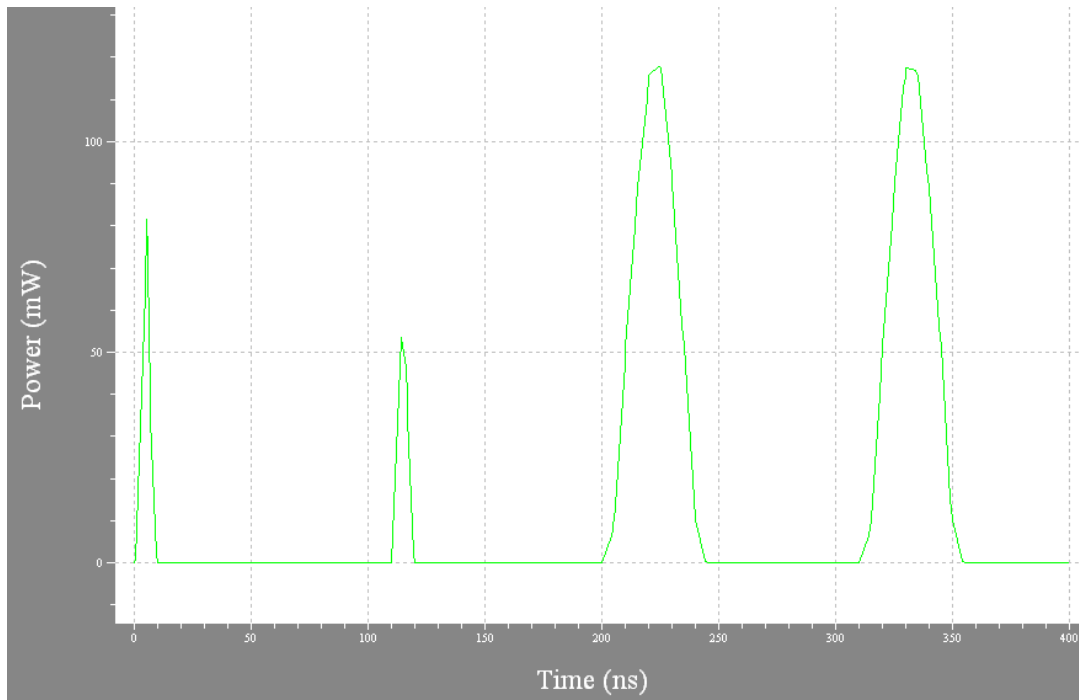


Figure 4. Power waveform for an 8 bit chip inverting the 8 bit video and 16 bit audio data

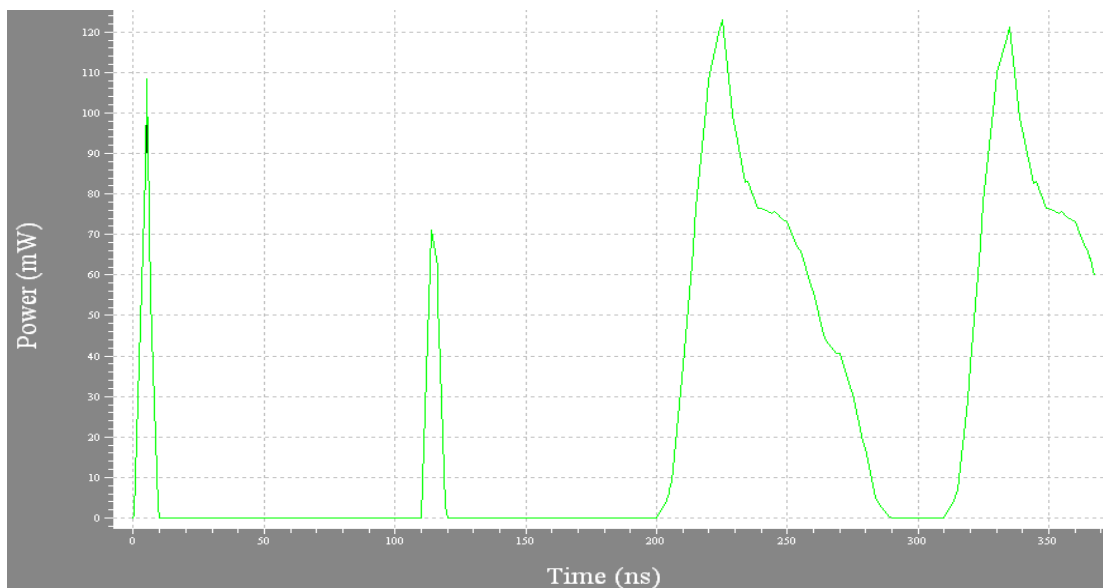


Figure 5. Power waveform for a 16 bit chip inverting the 8 bit video and 16 bit audio data

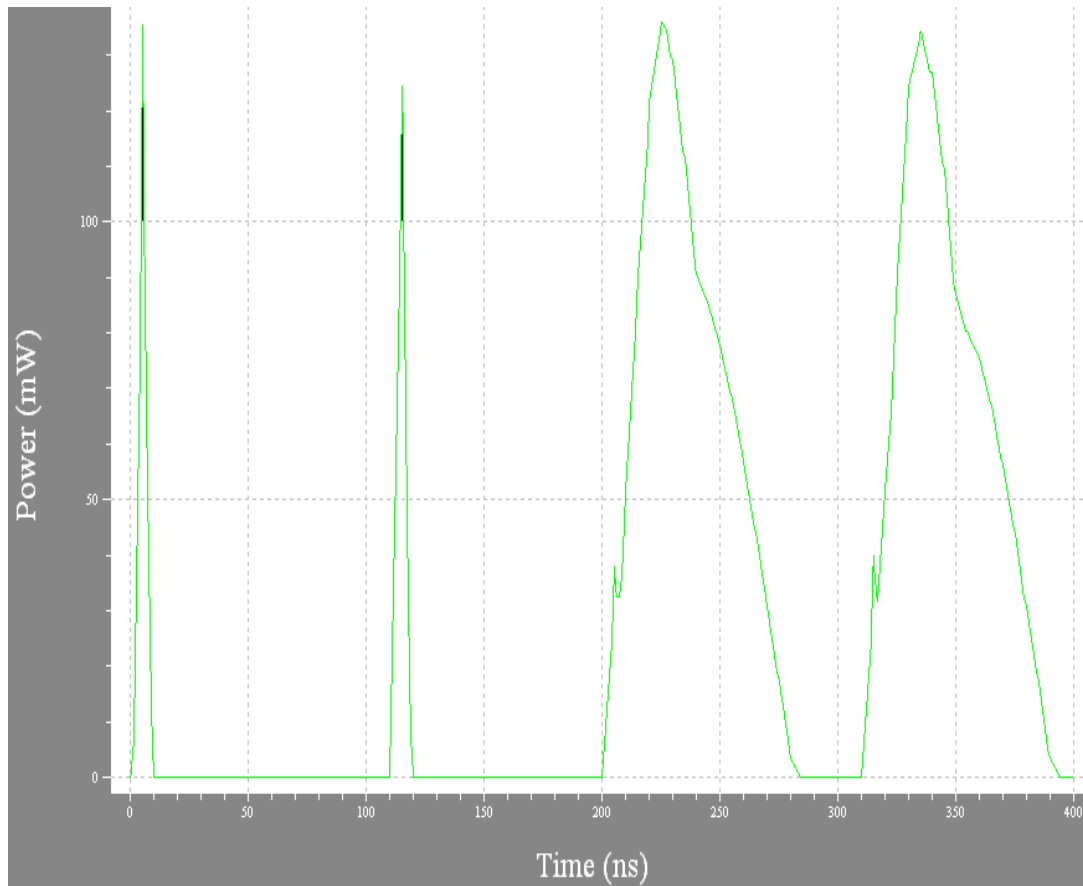


Figure 6. Power waveform for a 32 bit chip inverting the 8 bit video and 16 bit audio data

Table 1. Experimental results for different processor Size to invert 8 bit video and 16 bit audio data

PROCESSOR SIZE	POWER CONSUMPTION(mW)
8 BIT	118
16 BIT	125
32 BIT	135

From the Table 1, it can be proved that an 8 bit chip consumes less amount of power than the other processor sizes. But using 8 bit data-paths would slow the system. Hence techniques like pipelining and parallel processing can be used. At the outset, this paper makes a strong argument to use an 8 bit processor size for high end VLSI Low Power media applications.

V. CONCLUSIONS

The paper brings to light a novel argument of the use of a 8 bit processor in place of 32 bit or 64 bit processors, for low power chip design. The main point of consideration is that the designer has to carefully extract the net list information so that his circuit level interpretation is correct and as per the designed HDL Code. But it is advisable to implement this method for small codes of small experimental applications, since as the size of the code increases, the schematic size increases enormously. This method, even though is complex, is reliable, simple and cheap. The results have proved that an 8 bit processor chip can do all the functions at good speed, but has the least power consumption. Hence it can be concluded that 8 bit processor can still be used for high edge media applications.

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REFERENCES

- [1] Jer Min Jou, Yun Lung Lee, Chen Yen Lin and Chien Ming Sun, "A Novel Reconfigurable computation unit for DSP applications", IEEE comp. society annual symp. on VLSI, pp 439-444, ISVLSI'07.
- [2] Navid Lashkarian, Ed Hemphi, Helen Tarn, Hemang Parekh and Chris Dick, "Reconfigurable Digital Front End Hardware for wire less base-station transmitters: Analysis, Design and FPGA implementation", IEEE transactions on circuits and systems, vol 54, No. 8, pp 1666-1677, Aug 2007.
- [3] Huijuan Yang and Alex.C.Kot, "Pattern based data hiding for Binary Image Authentication by Connectivity-Preserving", IEEE Transactions on multimedia, vol 9, no. 3, pp 475-486, APRIL 2007.
- [4] Giorgos Dimitrakopoulos, Christos Mavrokefalidis, Kostas Galanopoulos and Dimitris Niolos, "Sortor based permutation units for Media-Enhanced Processors" IEEE Transactions on VLSI systems, vol 15, no. 6, pp 711-715, June 2007.
- [5] Florin Balasa, Hongwei Zhu and Ilie.I.Lucian, "Computation of storage requirements for Multi dimensional signal processing applications", IEEE transactions on VLSI systems, vol 13, no 5, pp 447-460, April 2007.
- [6] Ismail Kadayif, Partho Nath, Mahmut Kandemir and Anand Sivasubramaniam, "Reducing data TLB power via compiler directed Address Generation", IEEE transactions on Comp. Aided design of IC's and systems, vol 26, no 2, pp 312-324, Feb 2007.
- [7] Alexandru Andrei, Petru Elas, Zebo Peng, Marcus.Y.Schmitz and Bashir M Al Hashni, "Energy optimization of multiprocessor systems on chip by voltage selection", IEEE transactions on VLSI systems, vol 15, no 3, pp 262-275, Mar 2007.
- [8] Frank Zhigang Wang, Sining Wu, Na Helian, Michael Andrew Parker, Yike Guo and Yuhui Deng and Vineet.R.Khare, "Grain Oriented Storage: A single-image cross domain. High bandwidth architecture", IEEE transactions on computers, vol 56, no 4, pp 474-487, April 2007.