Detailed Router for 3D FPGA using Sequential and Simultaneous Approach

Ashokkumar A, Dr. Niranjan N Chiplunkar, Vinay S

***Abstract*—The Auction Based methodology for routing of 3D FPGA (Field Programmable Gate Arrays) has been implemented using two approaches. One is the Simultaneous approach, where the Nets bid for the Pins they need, and all the bids are processed simultaneously. In the sequential approach, the bidding process is finalized sequentially. It has been observed that in large circuit designs, the simultaneous approach gives better results over sequential approach.**

Index Terms—Field programmable gate arrays, Routing, Nets, Wire, Algorithms.

I. Introduction

The term VLSI (Very Large Scale Integrated Circuit) refers to the ability to pack large number of transistors of given circuit in a small silicon area during the manufacturing of Integrated Circuits. Full custom, Semi Custom and PLD (Programmable Logic Design) approach are the three well known approaches for designing the VLSI ASICs (Application Specific Integrated Circuits). FPGA (Field Programmable Gate Array) is a User Programmable Integrated Circuit , using which a relatively large digital circuit can be implemented. FPGA technology is normally used to implement Prototype designs with a very low turn around time. Two Dimensional FPGA (2D FPGA) is a programmable IC structure, where in the Configurable Logic blocks, Routing resources and the I/O blocks are spread in multiple rows and columns in a 2 dimensional space(Fig. 1). The 3D FPGA provides increased number of logic blocks in the FPGA by using several number of layers of 2D FPGAs, interconnected by vertical vias[1]. These vias are single segmented or multi segmented[2]. If the design to be implemented is large, then 3D FPGA architecture is suitable(Fig. 2), as the increased number of logic blocks provide required logic. The layered architecture also provides routing infrastructure, thus improving the routability of the FPGA[3]. The routing problem of 3D FPGA is a problem of finding path between the pins of different logic blocks.

While routing source Pin of a logic block to the destination Pin of a different logic block, the path may have to go through different tracks. This path is called a Net. Each Net is made of

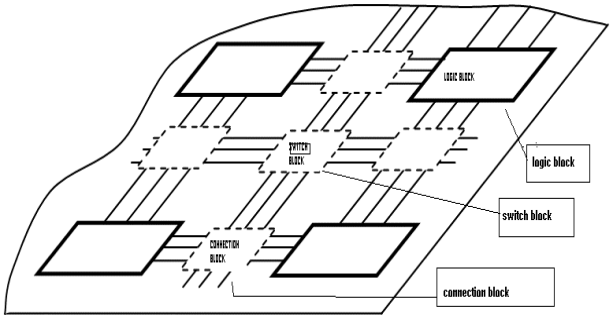

Fig 1. 2D FPGA

two terminal connections. Each Net requires a separate track. These tracks originate at different Pins of Logic blocks, Connection blocks and Switch blocks[8]. So the problem is to reserve Pins to each Net connection.

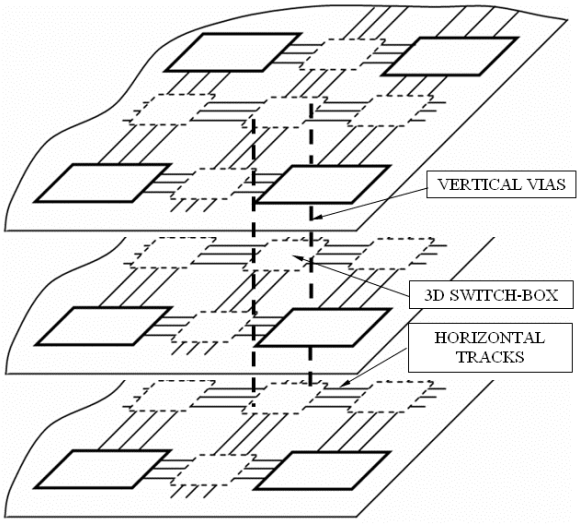

Fig. 2 3 D FPGA

The auction based methodology is used here to route the Net. The method involves a bidding process. Here Nets bid for the Pins of Blocks. The Nets use Points for the bidding. There is an Overseer, which oversee the Bidding Process. The Overseer allocates initial Points to every Net. The number of Points may be based on the number of Pins, the Net wants or it may be constant number.

The Bidding process may be conducted either in sequential or in simultaneous fashion[5]. In the sequential approach, the Pin auctions are held in sequential fashion. In the

This work was supported by the Computer Society of India under Grant for Minor Research Project Scheme(No. 1-14/2006-03).

Ashokkumar A, Research Scholar, N M A M Institute of Technology , Nitte 574 110. Karnataka, India. (e-mail: ashok567@gmail.com).

Niranjan N Chiplunkar, Vice Principal and HOD CSE, N M A M Institute of Technology, Nitte. Karnataka, India. (e-mail: nchiplunkar@nitte.ac.in).

Vinay S, Senior Lecturer, N M A M Institute of Technology, Nitte and Research Scholar at MIT, Manipal, India (email: vinaymanyan@gmail.com).

simultaneous approach, the Bidding is conducted in a simultaneous fashion. The Nets get a chance to revise the Bids. They use Points for bidding. The Pins keep track of the Bids, they have received. The Pins allow the winning Nets to use them for complete the Paths. The process is explained in the methodology section in detail.

The router requires placement information as inputs[6]. This placement is done such that the inter layer connection is minimum. Hence for any Net, the Pins required is available in the same layer. The router makes use of a single source shortest path algorithm to decide about the global route[7]. The Global route is the channel through which the Path passes through. Here the decision on exact segment is not taken (fig. 3). In the next phase, detailed route is decided. The detailed route specifies the exact segment used for the Path(Fig. 4) .

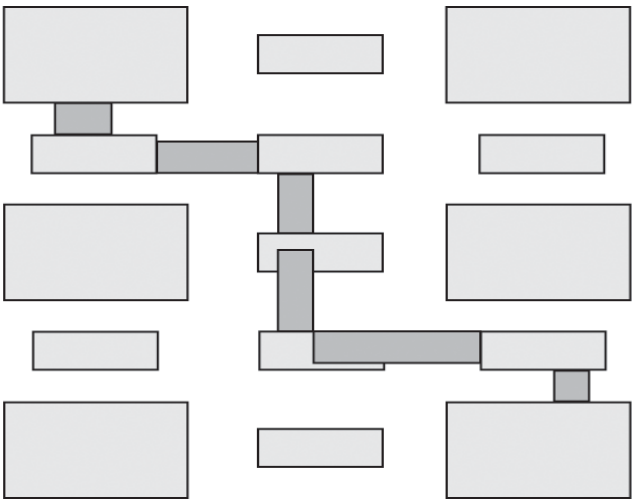

Fig. 3 Global Routing

The Auction process for finding the detailed route is not a single step process. The process is carried out in number of iterations. In every iteration, the Nets get a chance to modify their Bids on the Pins of a Block. If the Net wants a particular Pin, it can increase the Bid on the Pin. On the other hand, if the Net is winning the Bid without competition, it can decrease the Bid, so that the Points it saved may be used in other Bids.

II. RELATED WORK

Researchers at the University of Virginia have implemented Auction Based Detailed Router for 2D FPGA [11]. "TPR: Three Dimensional Place and Route tool" is a placement and detailed routing package developed by researchers of University of Minnesota. But this tool is inspired by a 2D placement and detailed routing tool of University of Toronto "VPR: Versatile Placement and Routing tool" [5]. Ours is the first effort to make use of auction based methodology for 3D FPGA routing .

III. AUCTION BASED METHODOLOGY

The Auction Based Methodology for the routing problem in 3D FPGA uses several Data structures.

Overseer oversees the Auction Process. Initially it allocates Points to all the Nets, for participating in the Pin Auction. The number of Points may be based on the number of Pins Net needs. It may be a constant value, irrespective of the number of Pins, the Net needs. We have used the second strategy. The Overseer also keeps track of the Bidding and signals the end of the Process. After all the Nets place their Bid, for the Pins they require, one iteration is said to be over. The Overseer gives each Net to modify the Bid, by changing the Bid Value. The Value may be increased or decreased, depending on whether the Net is winning or losing the Pin Auction. The Overseer stops the Bidding Process after certain number of iterations. If all the Nets get the Pins they need successfully, then the Routing is successful, else it fails.

Net is responsible for Bidding for the Pins, it needs for establishing the connections. Once the Bidding process starts, Net places Bid with the certain Value of Points. The Value may be high or low. The value depends on the criticality of the Pin and also on the number of the Pins, the Net needs to complete the connection. When Overseer allows, the Nets modify the Bid Point Value. There may be increase or decrease in the value. If the Net is winning the Pin comfortably with a large margin from its competitor, then the Net may lower the bid. On the other hand if the Net is losing the Bid, then it may try to increase the Bid Points using the unused Points available.

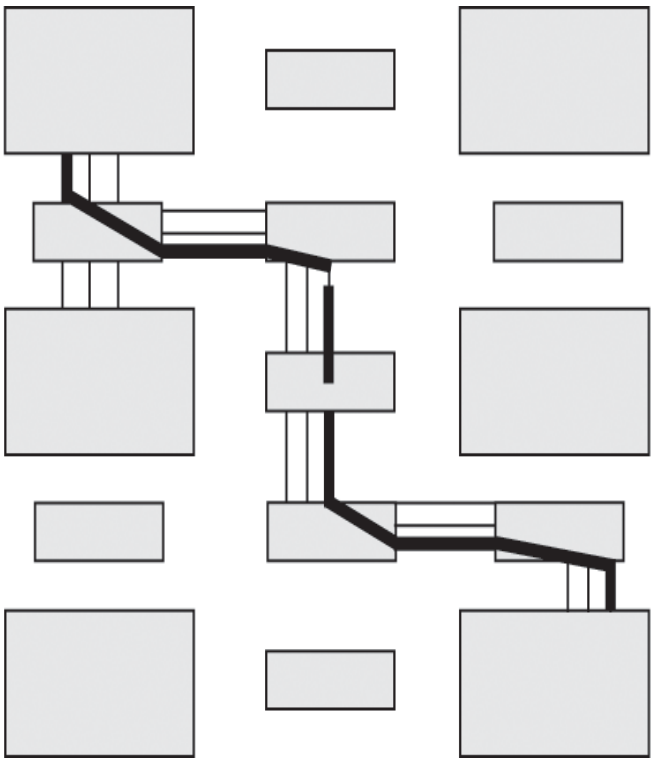

Fig. 4 Detailed Routing

The Pin is the third data structure in this router. The Bidding takes place for the Pins and it is the responsibility of the Pin to keep track of the Bids placed by various Nets on it. When the Oveseer notifies the end of the Bidding Process, the Pin should allow the winning Net to use it.

A. Simultaneousl Approach

In this approach, the Bidding process is held in number of iteration and the Pins are allocated at the end of the Auction. In every Iteration, the Nets get a chance to change their Bids. The Nets which have no Points or insufficient Points to increase their Bids on the Pins, find new Path and Bid for new Pins. The Net ordering may affect Routing. Simultaneous router makes sure that problems of Net ordering do not affect routing.

B. Sequential Approach

Sequential router on the other hand is affected by Net ordering. Here, the decision on Bidding is taken after each iteration. In every Iteration, all the Nets are given a chance to place their Bids on the Pins they want. At the end of each Iteration, the Nets are given a chance to modify their Bids, once modification is done, then the Pin Auction is finalised. The Nets which have won all Pin Auction are successful and others have to continue in Auction Process. After every round, the number of Nets participating in the Auction go on decreasing. At the end of each round, the Nets regain the Points and hence it may be used up for the next round of Bidding.

C. Implementation Details

The Simultaneous and Sequential Auction based router algorithms are given below.

1). Auction Based Algorithm(Simultaneous approach):

```
Input: Two terminal Netlist,
       Placement_details,
       Global_routes
Output: Detailed_routes
Start
Give each net an initial allocation of funds
done = false
while (not done ){
  for each losing Nets with insufficient  funds
        find new global route;
    Allow each net to place bids or modify bids in any desired
pin-auctions;
     if( all nets have a complete detailed route)
       done = true // successful completion
   elseif (any net cannot realize a complete detailed route)
      done = false // unsuccessful }
End
```

2). Auction Based Algorithm(Sequential approach):

```
Input: Two terminal Nettlist,
       Placement_details,
       Global_routes
Output: detailed_routes
Start
Give each net an initial allocation of funds
done = false
while (not done ){
  for each losing Nets with insufficient  funds
        find new global route;
    Allow each net to place bids or modify bids in any desired
pin-auctions;
     freeze the winning Pins positions ;
     if( all nets have a complete detailed route)
        done = true // successful completion
     elseif (any net cannot realize a complete detailed route)
        done = false // unsuccessful }
End
```

We have developed a package to carry out detailed routing in 3D FPGAs. Our implementation is on Linux platform using gcc compiler. We have used Object Oriented approach for our implementation.

D. Data Structures

Some of the important data structures used in our implementation are:

3.2.1 Block

To represents various types of blocks in the 3D FPGA like Logic blocks, connection block and switch block.

3.2.2 Net

Nets are the active agents in our implementation. The Nets should know which pins they want to realize their connection. They should decide the bid amount also. They should revise their bids such that they have winning chance and also when they win Pin auction it is only by small difference. By doing so Nets can save the amount they have for some other pins. In case they cannot win certain pins, Nets should find out alternative pins, to realize their connections.

3.2.3 Pin

Pin data structure is responsible for holding information on the bids it receives from Nets. Pin ultimately decides who the winner is. It should allow Nets to revise their bids. It has the responsibility to take care to see that only winning Nets use it.

3.2.4 Overseer

Overseer's role is to oversee the auctioning process. It can interfere in the auction process by allocating additional funds to the needy Nets to help them win some pin auctions.

IV. RESULTS

The sequential and simultaneous Auction Based algorithms for solving the detailed routing problem in 3D FPGA, implemented using object oriented approach using gcc compiler in Linux platform using Intel® Pentium® 4 Processor 3.0Ghz HT 800Mhz, 2MB L2 cache, 1 GB RAM machine were run on various Benchmark circuits[5].

The Benchmark circuits are of different sizes ranging from 1064 Logic blocks for Ex5p to 8383 Logic blocks for clma Benchmark circuits.

The sequential approach gives results faster than the simultaneous approach for smaller Benchmark circuits , since the competition for the Pins is less, in these circuits.

TABLE. I: RUN TIME FOR SIMULTANEOUS AND SEQUENTIAL ROUTERS
(INTEL® PENTIUM® 4 PROCESSOR 3.0GHZ HT 800MHZ, 2MB L2 CACHE, 1 GB RAM)

Sl. No	Circuit	No. of CLB	No of IO Block	CPU time in secs for simultaneous router	CPU time in secs for seq router
1	Ex5p	1064	71	80	59
2	Apex4	1262	28	77	70
3	Misex3	1397	28	82	75
4	Alu4	1522	22	61	55
5	Des	1591	501	70	70
6	Seq	1750	76	111	131
7	Apex2	1878	402	145	165
8	Spla	3690	62	522	542
9	Pdc	4575	56	1050	1070
10	Ex1010	4598	20	276	296
11	Dsip	1370	426	35	55
12	Tseng	1407	174	16	29
13	Diffeq	1497	103	46	56
14	Bigkey	1707	426	45	57
15	S298	1931	10	51	71
16	Frisc	3556	136	225	240
17	Elliptic	3604	245	140	159
18	S38417	6406	135	213	249
19	S38584.1	6447	342	267	279
20	Clma	8383	144	940	1040

In larger circuits where there is clash between Nets for the Pins, the Simultaneous method performs better. This may be because in the Simultaneous approach, the winning Nets do not get the possession of the Pins till last round. Here Pins are not allocated till all the Nets find suitable Paths to connect their Nets. Whereas in the sequential approach, winning Nets get the Pins they have won, after every round. Since Net ordering affects the Routing Process, it may force the remaining Nets to find round about routes. This affects the performance of the Detailed Router. However all the 20 Benchmark circuits are routed successfully by our Detailed Router.

The delay, routing area and Horizontal Channel Width(HCW) are estimated as in [3] and are plotted against number of layers in the 3D FPGA , as shown in Fig 5. The average values of these three parameters for different Benchmark circuits using both approaches (sequential and simultaneous) have been taken while plotting the graph. Fig 6. shows the plot of Routing wire length versus number of layers in 3D FPGA (again based on the average value). It can be seen that with the increase in number of layers, the Delay, routing wire length and Channel width decrease, whereas the routing area does not see much change with increase in number of layers.

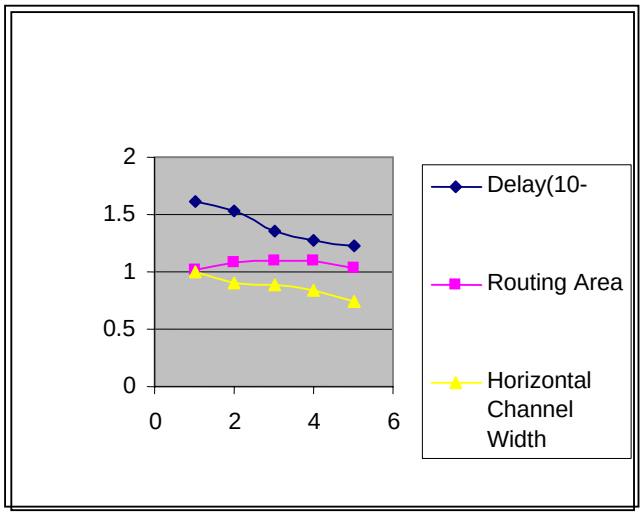

Fig. 5 Effect of number of layers on average values of delay, Routing Area, Horizontal Channel Width for all circuits.

V. Conclusion

We have developed two types of detailed routers for 3D FPGA based on Auction based methodology. In Auction methodology, We consider Pins as routing resources and Nets as active agents. Nets bid for the Pins. The first method works on simultaneous approach and the second one using sequential approach. Simultaneous approach solves routing problem faster in case of bigger circuits. The sequential method works faster for smaller circuits.

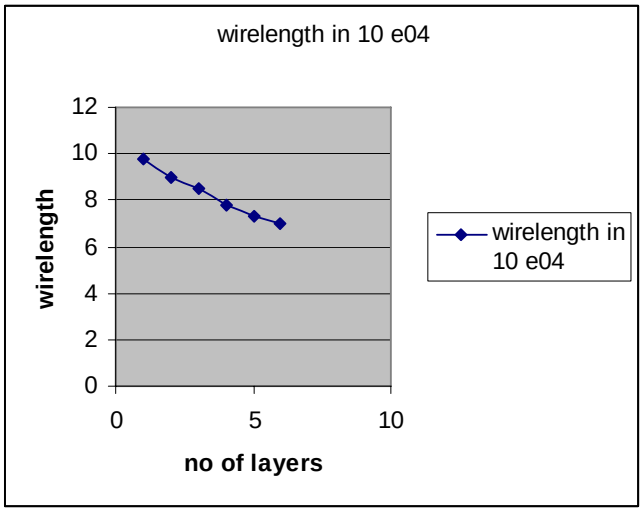

Fig. 6 Effect of number of layers on wirelength

REFERENCES

[1] M. Alexander, J. Cohoon, J. Colflesh, J. Karro, and G. Robins,, "Three-dimensional field programmable gate arrays," *Proc. IEEE International ASIC Conf.*, Austin TX, September 1995,pp. 253-256.
[2] C. Ababei, H. Mogal, and K. Bazargan, "Three-dimensional Place and Route for FPGAs," Proc. IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC), 2005.
[3] C. Ababei, H. Mogal, and K..K. Bazargan, " Exploring potential benefits for 3D FPGA Integration," Proc. Field Programmable Logic and its Applications(FPL), 2004.
[4] A.J. Alexander,J.P. Cohoon, Jared L. Colflesh, J. Karro," Three-Dimensional-Field Programmable Gate Array", Proc. Intl. ASIC, Conf., 1995, pp.253-256.
[5] V. Betz and J. Rose, "VPR: A new Packing Placement and Routing Tool for FPGA Research", Field Programmable Logic App., 1 997, pp.213-222.
[6] G. Borriello, C. Ebeling, S.Hauck, and S. Burns "The Triptych FPGA Architecture," *IEEE Transl.on VLSI Systems*, vol. 3, No. 4, 1995, pp. 491-501.
[7] C. Ebeling, L. McMurchie, S.A. Hauck, and S. Burns, "Placement and Routing Tools for Triptych FPGA," IEEE Tans. VLSI Systems , Vol.3, No. 4, Dec. 1995, pp.472-483.
[8] Cristinel ababei, "Design Automation for Physical Synthesis of VLSI circuits and FPGAs,."A Dissertation submitted to University of Minnesota, December 2004.
[9] M.J. Alexander , "High Performance routing for FPGAs", A Doctoral Thesis , University of Virginia, 1996.
[10] N. Sherwani, "Algorithms for VLSI Physical Design Automation" Second edition, Kluwer Academic Publishers , 1995.
[11] Sean T McCulloch, "Quark: An Auction Based Router for FPGAs", May 2000.