Reliability and Fault Tolerance of Ultra Low Voltage High Speed Differential CMOS

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Abstract

The reliability and fault tolerance of the differential ultra low voltage gate is elaborated in this paper. The gates optimal yield and defect tolerance compared to ULV gate and standard CMOS is given. The results are obtained through Monte-Carlo simulations. Keywords are: Ultra low voltage (ULV), Floating-Gate (FG), high speed and differential design.

1 Introduction and background

The transistor is one of the key components that has made possible the plethora of portable electronic gadgets that enriches our everyday life. Unfortunately, many multi-million transistor chips fabricated in modern processes suffer from very low yields ($< 50\%$) [1]. On the other hand the consumer market has dramatically increased demands for sophisticated portable electronics such as laptop computers and cellular phones. Portable electronics drive the need for low power and low voltage due to a limited budget set by a fixed maximum battery mass, while on the other hand demand for high-performance electronics regarding speed. Thus, in the last decade major developments have made low power designs a key objective in addition to speed and silicon area. In order to lower the energy consumption several approaches exists. One of the most fundamental and effective approach is to lower the supply-voltage [2,3]. Furthermore, it is called ultra low voltage ULV when the supply voltage is reduced to hundreds of millivolts [4, 5]. However, the scaling of the supply-voltage has the adverse effect of the performance of the design concerning speed. The main challenge is to obtain high speed at as low as possible supply-voltages. To maintain good evaluation response time at ultra low supply-voltages, the threshold voltages of the transistors must also be reduced. Unfortunately, this requires a change in the CMOS fabrication process. Multiple-V_{dd} technique has been proposed for low voltage high performance circuits designs [6] without changing the fabrication process. Floating-gates (FG) have also been proposed for ultra low voltage and low power (LP) logic [7]. Unfortunately, modern process face significant gate leakage due to the thin oxide. A ULV floating-gate inverter employing a frequent recharge technique has shown good properties in achieving high speed at ultra low voltages [8]. Even though the ULV gate has shown good performance it also has limitations due the leakage at the semi-floating-gates (SFG). A differential ULV gate has been proposed by including a keeper function [9] which is argued to have the speed of an ULV but the stability as a standard CMOS.

In this paper the reliability, yield and the defect tolerance of the differential ULV inverter compared to both standards CMOS and to ULV floating-gate inverter is examined. The main goal is to find the designs behaviour and pinpoint the adjustment parameter giving the best yield and fault tolerance.

The outline of this paper is as follows: in section 2 the differential ULV gate is thorough presented and the key advantages are pointed out. Section 3 presents the aspects of reliability such as speed, stability and noise-margin of the differential ULV both compared to CMOS and to ULV floating-gate inverter. While in section 4 a discussion on the achieved results are given. Finally, the paper concludes by pointing out the optimal design parameters. The simulation results demonstrated throughout this paper were obtained by simulation produced in a STM 90nm process environment provided by Cadence.

2 Differential ULV Inverter

The real appreciation of the differential ULV gate is obtained by understanding the design which its has its inheritance from. A floating-gate inverter were introduced and proposed to operate at ultra low voltage with high speed in [8]. The gate is called ULV and is shown in Fig. 1. The gate has been demonstrated to have a EDP higher than 20 times a standard CMOS gate. Furthermore, the gate has been used in the context of power analysis and has shown good capabilities to camouflage the current dissipation dependent of the input pattern [10]. Unfortunately, the ULV inverter and ULV gates in general using floating-gate design, has faced challenges due to their stability properties. With stability we refer to the deviation from the rails at the evaluation. The ULV gates challenge is closely linked to the well-known problem with floating-gates in modern process. As the technology makes possible to develop smaller and smaller transistors, as a conse-

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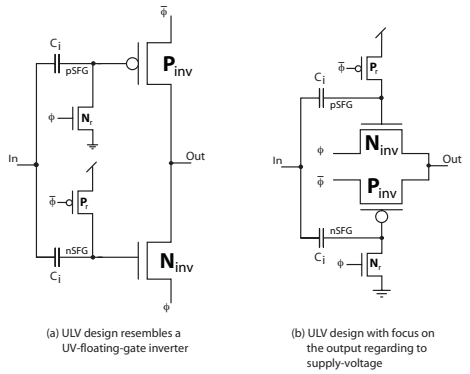

Figure 1: *The figure illustrates the ultra low voltage gate. Both designs are logically and electrically equivalent. In (a) the design clearly shows the inverter and the biasing/recharging of the floating-gate, while (b) is designed to emphasise that the output is not directly connected to the supply voltage.*

quence the gate oxide becomes thinner, resulting in a increased leakage from the floating-gates. This leakage sets boundaries for the operating frequency, both concerning the high and low cut-off. As a countermeasure for the leakage, the differential ULV gate were introduced. The differential ULV gates real asset is the keeper function included in the design, as demonstrated in Fig. 2. The keeper function is in first degree turning "more" off the transistor which should be off. In [11] the potential of the differential ULV gate, relative to standard CMOS, is discussed and it is found to be more than a decade better than ULV.

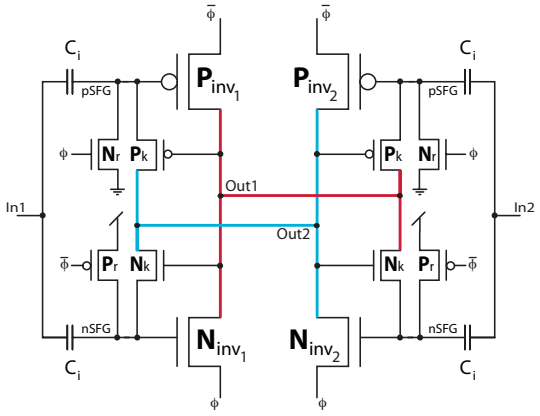

Figure 2: *The ultra low voltage differential semi floating-gate inverter including a keeper function, P_k and N_k, is illustrated. Transistor sizes are kept minimum and matched, the input capacitances are scaled relative to obtain the same voltage attenuation for both nSFG and pSFG.*

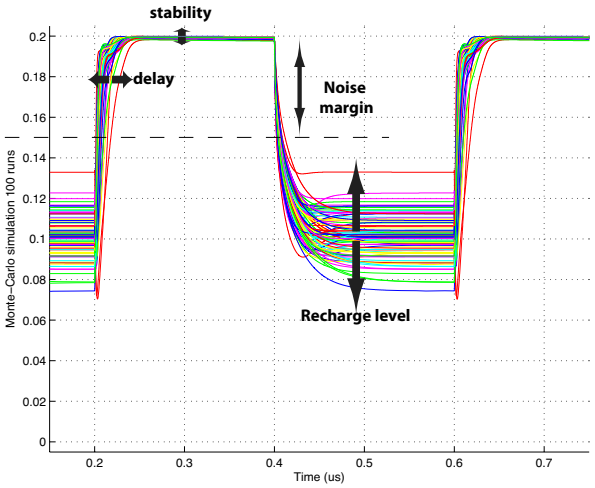

Figure 3: *Simulation results for a Monte-Carlo corner simulation for 100 runs of the differential ULV gate shown in Fig 2. The environment is set to both process and mismatch variation. On the plot there are four commented areas to emphasise the discussion topics.*

3 Reliability and Defect Tolerance

The basis of the results presented in the following are obtained through Monte-Carlo simulations including both process and mismatch variations. The data is collected through 100 runs and a parametric simulation of the supply-voltage $V_{\rm dd}$. The supply-voltage is swept from 0.15V - 0.5V with common conditions and has shown a 100% yield for all three gates. There are three aspects which are of interest that comply after the 100% yield, namely (i) *delay variation*, (ii) *stability* and (iii) *noise margin*. In Fig. 3 the simulation results of a 100 run Monte-Carlo is presented and the fields of interest are commented. Contrary to the standard CMOS both ULV gates have a recharge period and the recharge level represents the gates equilibrium state. With the results in Fig. 3 the mismatch variations of the transistors are evident and imply a direct consequence, which is altering the recharge level. Accordingly, the offset at the recharge level from $V_{\rm dd}/2$ plays an important role for the succeeding gates. The fundamental behaviour of the floating-gate structures are based upon a input voltage transition from a specified level, in this case $V_{\rm dd}/2$. An offset at the recharge level would decrease the voltage transition seen at the succeeding gates, and may at worst-case not be enough to represent an correct output. In other words, floating-gate structures which employ frequent recharge mechanism with a equilibrium state, $V_{\rm dd}/2$, would complicate and may weaken the fault tolerance. In the light of Monte-Carlo simulation it is interesting to find out what the lowest voltage transition a differential ULV gate needs in order to be reliable also under such corner conditions. Data collected during the 100 runs have showed a maximum voltage deviation from the $V_{\rm dd}/2$ at a $V_{\rm dd}$ =

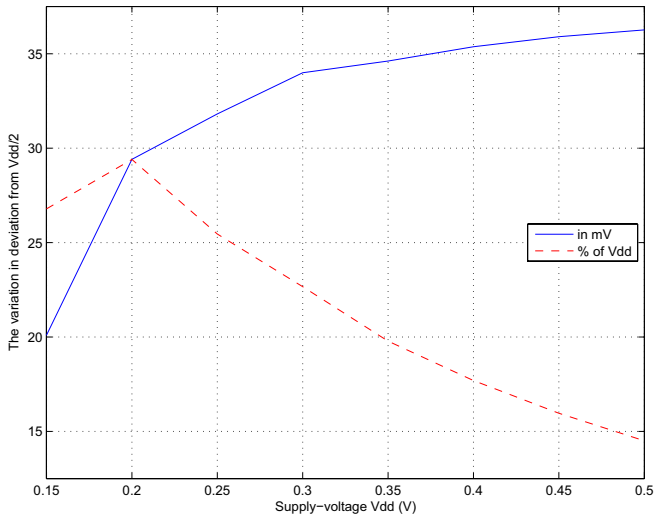

Figure 4: *Simulation results has shown variation due to mismatch at the recharge level. The plot represents both the deviation from the optimal equilibrium state,* $V_{\mathrm{dd}}/2$*, and the percentage within the supply-voltage* V_{dd}*.*

0.2 V with a variation of $b \approx 30$ mV, which impose a 30% attenuation. Figure 4 shows how the recharge level changes, using corner simulation, at worst case for different supply-voltages. The higher supply-voltage the more, in terms of mV, the equilibrium state is shifted, but the lower percentage relative to V_{dd}. The plot in Fig. 4 shows an intersect at $V_{\mathrm{dd}} = 200$ mV and an attenuation of 30%. Although, an attenuation of 30% is quite much, the differential ULV gate has not shown any signs of malfunction. The differential ULV gate has, as Fig. 5 illustrates, been simulated with an input voltage transition which is attenuated 80% and still are able to output correctly and also to a very good stability. The main affect an attenuation would imply is the increase in delay, i.e. the more an input signal is attenuated the higher the evaluation delay would become. Furthermore, the attenuation is also a function of the relation to the capacitive ratio seen at the semi-floating-gates. The robustness to a large attenuation for the differential ULV gate should be credited to the keeper function. The keeper transistor would help to turn off the right transistor as long as there is a small change in the output. Actually, as long as the two differentiated output are shifting in the opposite direction from each other from the equilibrium state, the representative keeper transistors would help the output drivers to symmetrically pull their representative outputs to the rails. Therefore, the ULV gate which does not have the keeper function is not expected to sustain a corner situation where the recharge level is shifted and thus generating an attenuation of more than 30%. Furthermore, it is important to stress that the keeper function also provides high stability under any circumstances in terms of deviation from the rails.

The situation where worst case recharge level offset and the worst case mismatch of the transistors regarding delay arise on the same chip and for two succeeding gates is highly unlikely. In a simulation environment, such as Monte-Carlo, only one given aspects is examined. Referring back to Fig. 3 the worst case of mismatch and process variation gives an change in the delay. The delay are measured based on a 50% to 50% input and output transition. The same conditions apply for all three designs. The maximum delay variation for a Monte-Carlo simulation with 100 runs are displayed in Fig. 6. The delay variation would increase if the simulation environment has included a sweeping parameter to represent the offset at the recharge level. The need to easier evaluate and visualise the collected data and to lay a foundation for discussing the values relative to CMOS, the data is plotted in Fig. 7. There is a minimum delay variation found at $V_{\mathrm{dd}} = 300$ mV both for the ULV and the differential ULV.

Once the delay is considered, the next topic is the stability of the gates. The stability represents the deviation from the rails and can also be used to indicate the yield during corner simulation. Bear in mind that the data set used are for a V_{dd} ranging from 150 mV to 500 mV and that all gates have showed 100% yield. Previously, the ULV were implied to have a lower yield due to the leakage at the semi-floating-gates. Although this statement has not been proved, the indications showed by Fig. 8 further strengthen the statement. The figure represents the stability variation relative to CMOS for different supply voltages. The stability variation is calculated as the difference between the best and worst stability during 100

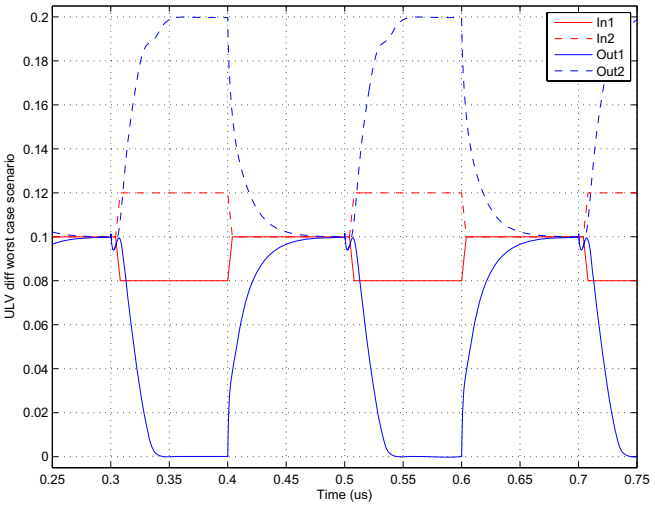

Figure 5: *Simulation results for the differential ULV gate verifying the gates ability to operate on very high attenuation for the input signal. The simulated environment are reflecting an input transition which is attenuated 80% and the outputs are for a succeeding gate.*

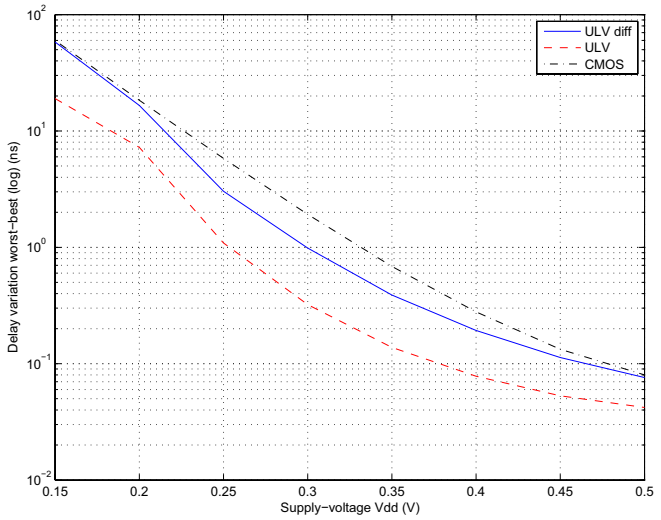

Figure 6: *Corner simulations show a delay variation as a mismatch at the input capacitors and transistors. The delay variation is calculated from a 50% to 50% input and output transition.*

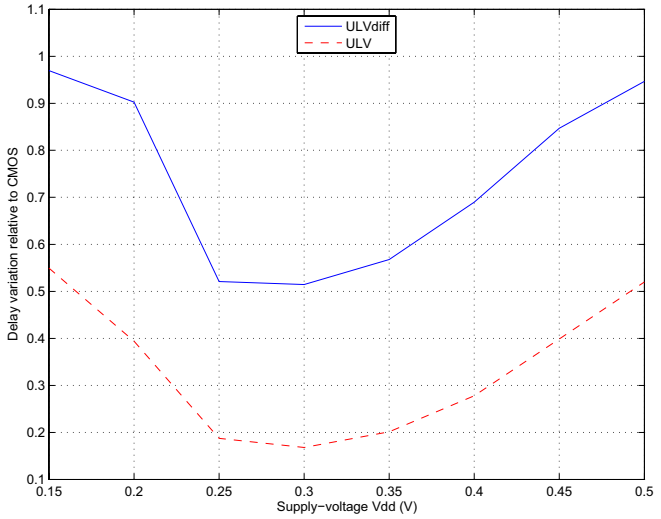

Figure 7: *The delay variation obtained during Monte-Carlo simulation is plotted relative to CMOS. The main goal is to bring out the difference and the potential of the ULV gates. Both gates show a minima at* V_{dd} *= 300 mV.*

runs.

Finally, the last aspects is the noise margin for the gates. The noise margin is actually closely linked to the yield. The data collected through corner simulation representing noise margin follows the formula below:

$$\frac{\mathrm{stability}_{WC} - (V_{dd} \cdot 0.75)}{V_{dd} \cdot 0.25} \qquad (1)$$

where $\mathrm{stability}_{\mathrm{WC}}$ is the lowest evaluation value through the 100 runs. The result would give a value which represents the worst case stability is within the percentage of the noise-margin. The lower the result is the closer the output is to the limits of the noise margin. In the context of yield it can be used to denote that a result above 0 has a 100% yield. The result for corner simulation is given in Fig. 9. As stated earlier for the ULV gate, the predictions for a 100% yield is diminishing. The result for a standard CMOS is very close to the differential ULV, as can be implied by Fig. 8, and thus not been included in the plot of Fig. 9.

4 Discussion

All the simulation results speak in the favour of the differential ULV gate. Firstly, the reliability the keeper function gives even though the recharge levels is shifted. Secondly, the delay variations show a optimal point at V_{dd} = 300 mV. Considering the threshold voltage, V_{th}, which for a 90nm process is approximately 270 mV, a general optimal point is expected to be around the V_{th}. Previous work on differential ULV gate has showed a optimal point for EDP to be at V_{dd} = 350 mV [11]. Referring to Fig. 7 there is not much of a difference between 300 mV and 350 mV. Thirdly, the stability of the gates has demonstrated quite large difference. The leakage at the semi floating-gate for the ULV gate really rules out its candidate. Fortunately, the keeper function at the differential ULV gate ensures that its candidate is present alongside standard CMOS. It can actually be found that the stability for the differential ULV gate is actually better than CMOS for V_{dd} between 230mV to 430mV, with a local minima at 300 mV. Referring to Fig. 8 the plot clearly demon-

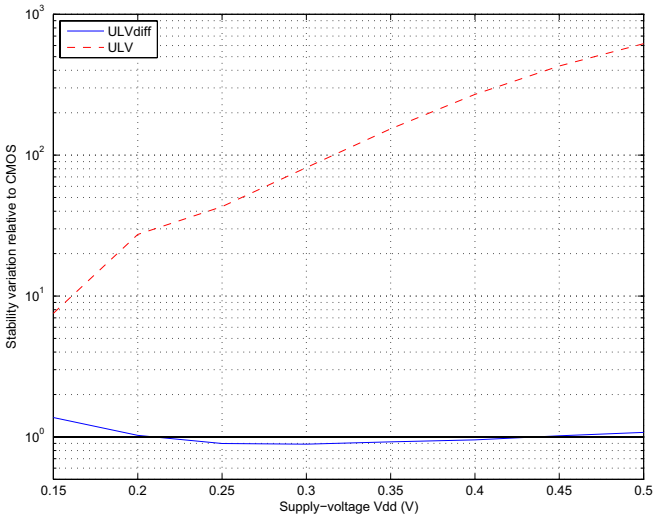

Figure 8: *The stability variations during a Monte-Carlo simulation relative to CMOS are plotted. The ULV gates stability decreases as the stability variation increases as a function of* V_{dd}*. The differential ULV gate shows an improvement of stability relative to CMOS for* V_{dd} *at the range 150 mV to 500 mV.*

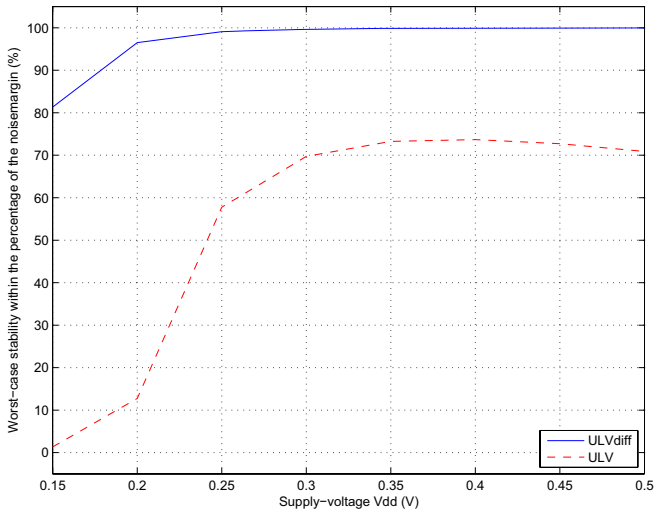

Figure 9: *Simulation results for the lowest evaluation stability as percentage within the noise margin is presented. This plot can also be directly used to elaborate on the yield of the gates. In the V_{dd} range given all gates have 100% yield, but the ULV is barely surviving corners as the V_{dd} decreases.*

strates the difference of the stability relative to CMOS. Ones again the results from corner simulations show a optimal V_{dd} at 300 mV. Last but not least, the discussion about the yield of the gates are presented in Fig. 9. The plot shows that the ULV gate is barely surviving the lowest supply-voltage, while the differential ULV gate at worst case is within 80% of the noise margin. An interesting discussion of the results are that the differential ULV gate becomes more and more stable and closer to obtaining 100% within the noise-margin, while the same cannot be seen for the ULV gate. The data show that the ULV gate has a top peak at $V_{dd} = 350$ mV. From all these results there is reason to believe that the optimal V_{dd} should be around 325 mV, in order to achieve the best EDP, reliability and fault tolerance. Furthermore, the main credit should be given to the keeper function. The keeper function, as obtained from the results, can be regarded to protect the benefit, i.e. speed, of the ULV gate and to strengthen its weakness, i.e. stability. Hence, giving the differential ULV gates the best from both designs, ULV and standard CMOS.

5 Conclusion

In this paper we have throughly analysed the differential ultra low voltage gate. The corner simulations, from a Monte-Carlo simulation, represents both process and mismatch variations. The data collected are based on 100 runs. Optimal supply-voltage which gives the lowest delay variation, most stability and best noise margin is $V_{dd} = 300$ mV. Overall reliability and fault tolerance for the differential ULV inverter has been demonstrated to be better than standard CMOS inverter and ULV floating-gate inverter.

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