Proceedings of the International MultiConference of Engineers and Computer Scientists 2009 Vol II
IMECS 2009, March 18 - 20, 2009, Hong Kong

Design of A 1.9GHz CMOS Downmixer Based on TSMC 0.18um Technology

Lin Wei, Huang Shizhen , Wangzhen , Chen Zhi

Abstract—**A Design of A 1.9GHz downmixer based on TSMC 0.18um is presented, using Gilbert configuration. The conversion gain is about 12.8dB, the noise figure is about 13.6dB and IIP3 is about 0.068dBm with -25dBm LO input signal. The power supply is 3V and the design is based on TSMC 0.18um technology.**

Key Word: CMOS , Downmixer Based

I. Introduction

Mixer is one of the most important parts in the transceiver. In the receiver, a downmixer is followed by the Low-Noise amplifier. It changes the RF signal to low frequency signal, achieving the conversion of frequency. Its performances have great effect on the whole system. It requires good linearity, low signal leakage, low noise and proper conversion gain.

II. PRINCIPLE

Figure 1 is the typical configuration of Gilbert. The differential pair M1 and M2 are the radio frequency port trans- conductance. M3,M4,M5 and M6 work like the switch.The radio frequency signal inputs thought M1,M2 and the LO signal inputs thought M3,M4,M5 and M6.

If the Lo signal is big enough, the output current of the double-balanced mixer is

$$I_o = g_m \times V_{rf} \times \cos\omega_{rf} t \times \mathrm{sgn}[\cos\omega_{LO} t]$$
(1)

In this formula g_m is the transconductance of M1 and M2, $\mathrm{sgn}[\cos\omega_{LO} t]$ is a square wave signal with the amplitude of 1 and frequency of ω_{LO} . Transform the $\mathrm{sgn}[\cos\omega_{LO} t]$ by Fourierism transformation, we take

$$\mathrm{sgn}[\cos\omega_{LO} t] = \sum A_k \times \cos k\omega_{LO} t$$
(2)

In this formula, k equals to 1，2，3 and so on. The current we need is when k equals to 1,we get output current as follows:

$$I_o = g_m \times 2 \times [\cos(k\omega_{LO} + \omega_{rf})t + \cos(k\omega_{LO} - \omega_{rf})t] \div \pi \quad (3)$$

The project was supported by the Natural Science Foundation of China (Grant No. 60572016).

The authors are with Fujian key Laboratory of Microelectronics & Integrated Circuits , Fuzhou University, Fujian Province, 350002, China (Email:hs501@fzu.edu.cn)

III. Design and component choice

The design Circuit is shown in Figure 2 as follows:

A. The design of tail current

The tail current is achieved by a current-mirror configuration. M7 and M8 have the same width to length ratio. We can change the drain current of M7 by changing the ratio of width to length. In this design, the drain current of M7 is about 3.5mA.

B. The design of transconductance M5 and M6

Through the saturation state of FET formula we get

$$g_m = \mu_n c_{ox} \times \frac{W}{L} \times (V_{gs} - V_{th}) \quad (4)$$

It means that when we increase W/L, the current of transconductance will increase, which can improve the gain of mixer. But

$$g_m = 2I_d \div (V_{gs} - V_{th})$$

when the current of drain keeps the same, $V_{gs} - V_{th}$ will decrease, and the non-linearity of the device will increase, so we must

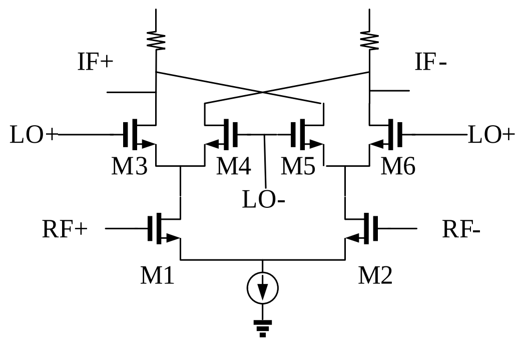

Figure 1. Typical Configuration of Gilbert

choose a proper width to length ratio and a proper voltage which can keep M5 and M6 in the saturation state. In this design, W/L equals to 100n/0.18n, the voltage is 1V. In order to improve the linearity of the current, we use a inductance in the source of M5 and M6. But we must consider that the use of this inductance will decrease the linearity of the mixer and big inductance is not fit for integration.

C. The Design of switch M3,M4,M5 and M6

M3,M4,M5 and M6 must choose the proper voltage to fit the formula $V_{gs} = V_{th}$ ，making the MOSFET operate in the switch-mode in the proper LO voltage. When designing these MOSFET, we must consider the optimization of noise and linearity. Because the 1/f noise is the main noise in the mixer, we can decrease the noise by increasing the width to length ratio. But if the width of the gate is too large, the parasitical capacitance will be large enough to slow the speed of the MOSFET. So we must choose a proper width. In this design W/L equals to 42n/0.18n.

D. *The Match of port*

All the ports are match to 50 ohm. By using Cadance software we can get the impedance conveniently.

E. *Other Recommendations*

In order to get larger gain we used source-follow configuration. It is composed of M9,M10,M11 and M12. But the use of source-follow configuration will decrease the linearity greatly, so we must choose the proper width to length ratio. In this design, the value is 500n/0.5u.

IV. Design and Component Choice

A. Conversion gain

The simulation of conversion gain is as Figure 4. We can see the conversion gain achieve 13dB when the frequency equals to 1.9GHz. We can improve the gain by increasing the transconductance or the load R_L. We can increase g_m by increasing the width to length ratio, but it also increase the non-linear of the circuit, so we must choose it properly.

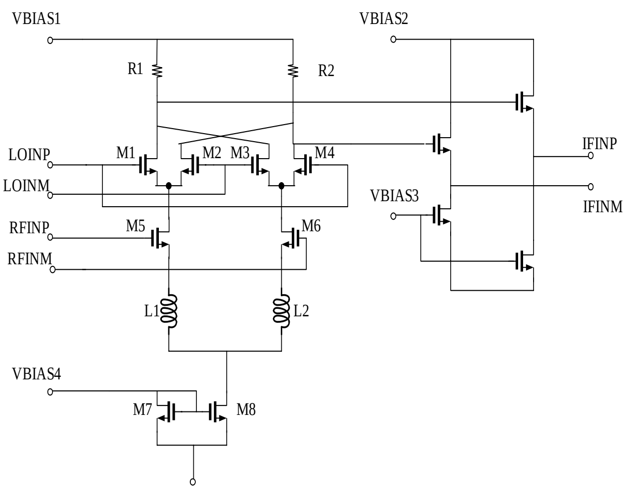

Figure 2 .the circuit of mixer

B. *Noise Figure*

The simulation of Noise Figure is as Figure 5.The noise figure is about 13.6dB at 100MHz. The main noise of the mixer is 1/f noise, thermal noise of the switch MOSFET, the thermal noise and load noise of drive port. Increase of the tail current will increase the 1/f noise and thermal noise of the switch MOSFET, but it can decrease thermal noise of the switch MOSFET and the conversion gain. By increasing the strength of LO signal will decrease 1/f noise and thermal noise of the switch MOSFET, but it can increase the thermal noise of drive port.

C. *Third-Order Intercept Point (IIP3)*

The simulation of Third-Order Intercept Point is as Figure 6. Under the -25dBm input LO signal, the Third-Order Intercept Point is 0.068dBm. The poor linearity dues to the usage of source-follow configuration and inductance.

D. *The Match of port*

Figure 7 is the match of RF port. Through Smith Chart we can see the match of RF port is good enough. Figure 8 is the LO leakage@RF input. LO leakage@RF input achieves -71.3dB at 1.9GHz, it achieves good isolation.

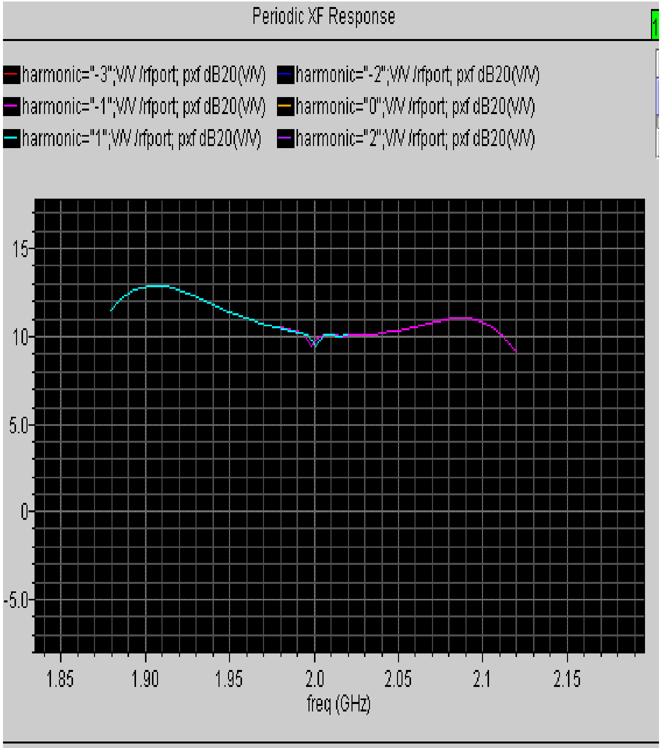

Figure 3. Conversion Gain

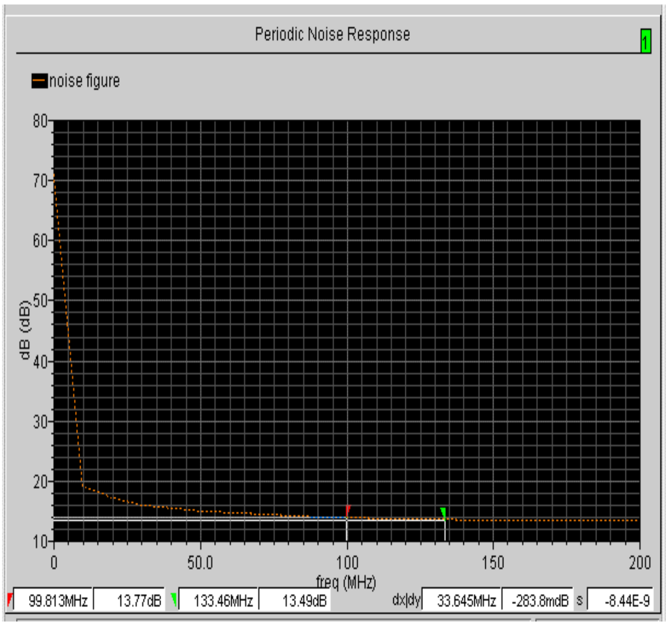

Figure 4. Noise Figure

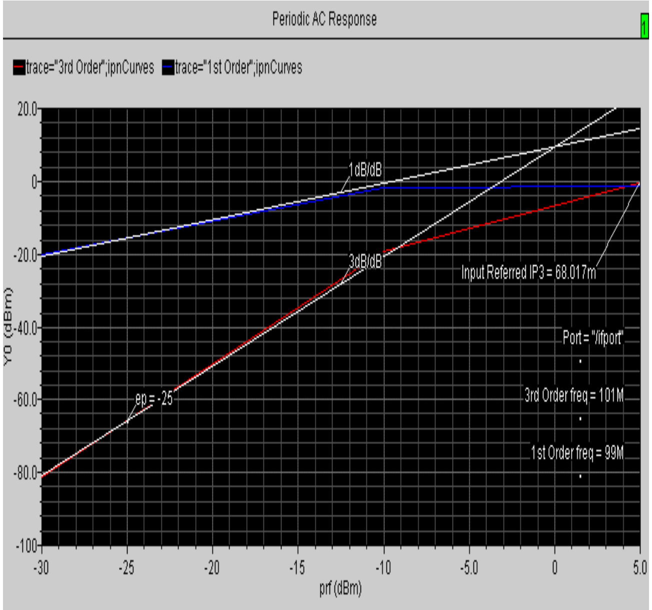

Figure 5. Third-Order Intercept Poin

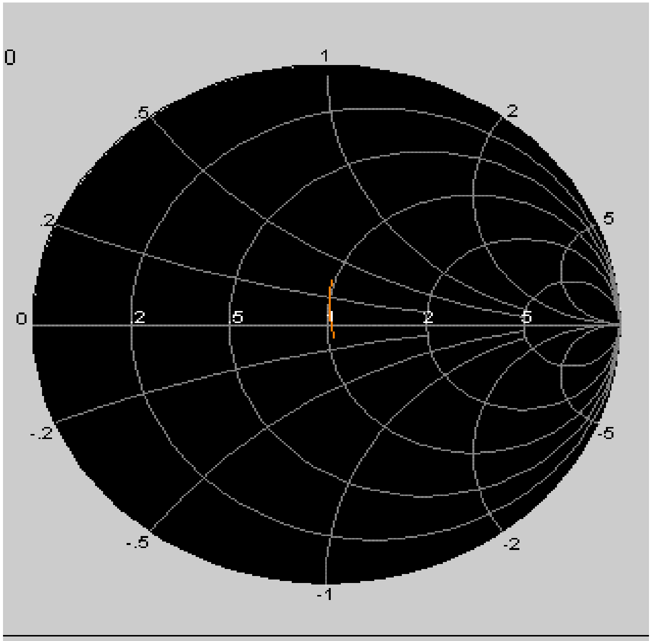

Figure 6. The Match of Radio Frequency Port

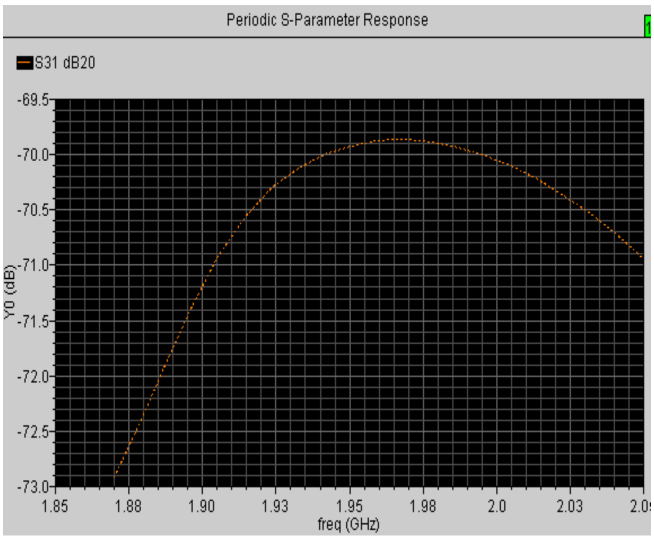

Figure 7. LO leakage@RF Input

V. Conclusion

A Design of a mixer with Gilbert configuration based on TSMC CMOS 0.18um technology is presented. The conversion gain is 13dB, Noise Figure is 13.6dB, Third Input Intermodule Point is 0.068dBm, LO leakage@RF input is -71.3dBm. This design achieves anticipate effect.

Acknowledgment

The project was supported by the Natural Science Foundation of of China (Grant No. 10871221).

References

[1] Thomas H. lee , The Design of CMOS Radio Frequency Integrated Circuits Second Edition

[2] P.J. Sullivan, B.A.Xavier, W.H.Ku," Low Voltage Performance os a Microwave CMOS Gilbirt Cell Mixer" IEEE Journal of Solid-State Circuits, vol.32, no.7, July 1997.

[3] A.Rofougaran,J.Chang, M. Rofougaran, S. Hhorram, A.Abidi., "A 1 GHz CMOS RF Front - End IC with wide Dynamic Range", IEEE Journal of Solid-Stale Circuits, vol. 31, no. 7, July 1996.

[4] S.Li, J.Zohios, J.Choi, M.Ismail,"RF CMOS Mixer Design and Optimization for Wideband CDMA Application", in Proc. of Southwest Symposium on Mixed-Signal Design SSMSD, USA, 2000.

[5] Behzad Razavi, Design of Analog CMOS And Integrated Circuits

[6] Q.Huang, F.Piazza, P.Orsmi, T. Ohgiuo, "The Impact of Scaling Down to Deep Submicron on CMOS RF Circuits", IEEE Journal of Solid-State Circuits, vol.33, no.7, July 1998.

[7I F. Stubbe, S. Kishore, C. Hull, V. Della Tom, "A CMOS RF-Receiver Front-End for lMHz Applications", in Proc. Of Symposium on VLSI Circuits, 1998.

[8] T.H. Lee, The Design of CMOS Radio-Frequency Integrated Circuits, Cambridge University Press, 1998.

[9] C. Hung, M. Ismail, K. Halonen, V. Porn, "Low-voltage Rail-to-rail CMOS V-I Converter", in IEEE Transactions on Circuits and Systems-Il: Analog and Digital Signal Processing. vol. 46. No. 6. June 1999.