Design Of A Voltage-controlled Ring Oscillator Based On MOS Capacitance

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Abstract—**The traditional ring voltage-controlled oscillator (VCO) generally uses the method of controlling resistance to change the oscillation frequency. This paper describes a 2GHz fully differential ring voltage-controlled oscillator based on 0.18μm CMOS technology. The oscillation frequency is controlled through MOS capacitance in the output of each delay cell. This method has stabile output waveform and linear tuning characteristic.**

Key Word: **CMOS, Voltage-controlled Ring Oscillator**

I. INTRODUCTION

With the wireless communication industry developing rapidly, CMOS circuits which are low-cost, low-power, high stability become the best wireless communication system solutions. In the communication system, the voltage controlled oscillator (VCO) is the important component, especially in the PLL circuit, clock recovery circuit and frequency integrated circuit, so it is the top priorities. According to oscillator principle, oscillator can be divided into two categories: One is the LC oscillation which is composed of the active devices, coupled with LC resonant circuit. Another one is the loop ring oscillator which is composed of delayed cascade units with a positive feedback. In this paper the design using TSMC 0.18μm CMOS process, completed in the Cadence design environment

II. FRAME OF CIRCUIT

A. Core of Circuit

The VCO using three chains structure, because reducing the number of chains can increase frequency, at the same time can reduce current consumption, lower power dissipation of circuit. Circuit module is shown in Fig.1. Current amplifier circuit module is used as a delay unit oscillator circuit, M1, M2 is a pair of differential input tubes, M3, M4 are the loads which are PMOS tubes in the form of diode connected. The diodes connected loads consume a voltage space, thereby there increase the PMOS tubes M5, M6 in the circuit, which are controlled directly by the input signal, this structure enable the voltage of output node to achieve the biggest value VDD, even if the current of tail current source changes largely it also has the relative constant output swing. NMOS tubes M0 and M7 make up of current mirror. NMOS tube M8

and M9 respectively equates to a capacitor CL, which value is controlled by VCON. Traditional oscillator adjusts the frequency by changing the value of load resistors, but this design is by changing control voltage V_{CON} to change the value of capacitor M8, M9 which work in the saturated state, then change the value of total output node capacitor of oscillator $(C_L'\|C_L)$, C_L is equivalent to the value of series-parallel connection of C_{GD}, C_{GB}, C_{GS}, C_{SB} and C_{DB}, C_L' is the node parasitic capacitance. According to this equation:

$$f_{osc} = \frac{1}{2NT_D} = \frac{1}{2\times3\times R_{ON}\times(C_L'\|C_L)} \tag{1}$$

The node parasitic capacitance C_L' has fixed value, then the oscillation frequency can be changed when changing the value of C_L. The output resistance is

$$R_{ON} = r_{o1}\,\|\,[\frac{1}{g_{m3}}\,\|\,r_{o3}]\,\|\,r_{05} \approx r_{o1}\,\|\,\frac{1}{g_{m3}}\,\|\,r_{05} \tag{2}$$

This method has little impact on the static working state, and almost has no impact on the output swing, and can use the larger scope of linear control voltage to change frequency.
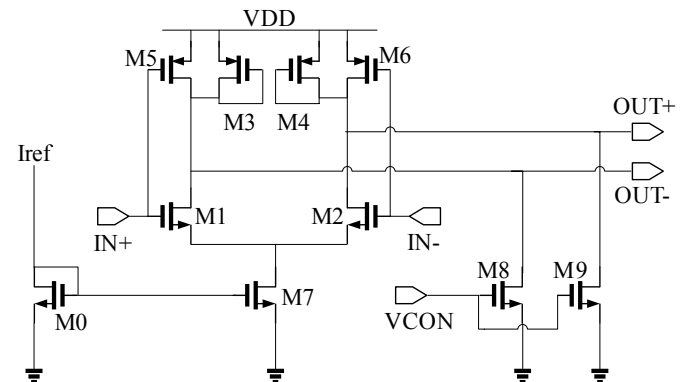

Fig.1 Implementation of each stage

B. Output Buffer

Output buffer circuit magnifies and regulates the output signal of front circuit, at the same time it provides large enough current and voltage to drive follow-up circuit. Even more important it can provide the better ability of isolation, then avoid the oscillation frequency of VCO to arouse the impact of frequency traction effect when there has the external effect of loads. The circuit is shown in Fig.2.

C. Figures

Output matching circuit follows after the output buffer circuit, which provides the 50Ω transmission line impedance matching, then eliminates the power loss of the signal reflection, and increases the efficiency of transmission. The circuit is shown in Fig.3.
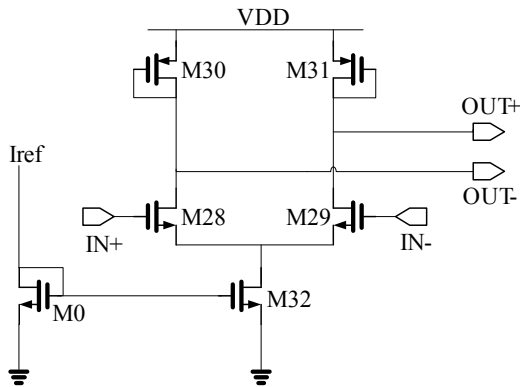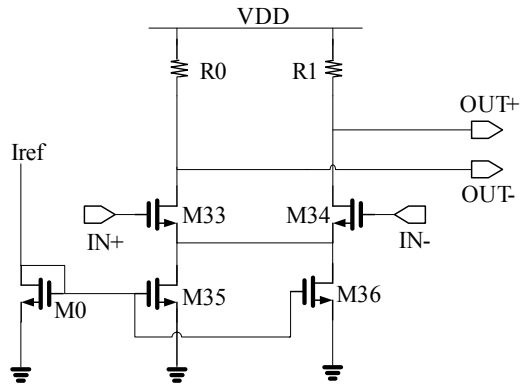
Fig.2 Output buffer

Fig.3 Output matching

III. CHOOSING DEVICE PARAMETERS

If you are using *Word,* use either the Microsoft Equation Editor or the *MathType* add-on (http://www.mathtype.com) for equations in your paper (Insert | Object | Create New | Microsoft Equation *or* MathType Equation). "Float over text" should *not* be selected.

channel length is much larger than the smallest feature size allows.

The choice of input NMOS transistors of the delay cells is based on three-tier structure, and it should consider that every level need to provide the enough value of Gain (Gain≥2), meanwhile it should consider the output node capacitance, resistance contribution.

As to the load transistors, the values of W/L are based on the output nodes resistance, capacitance and output signal frequency. These values of PMOS which next to the loads should be considered together.

As to the choice of MOS capacitor. First, the linearity of voltage-frequency tuning curve is necessary to be considered. Second, the tuning voltage range is to be considered. So the width of MOS capacitor can be smaller, and the length can be larger than the width, thus the tubes could achieve the aforementioned requirements.

A. Output Buffer

Output buffer must be able to isolate and amplify the signal which come from front circuit, so output buffer circuit should has certain gain. At the same time the width and length of the input NMOS transistors can not be too long, to avoid the effects on the output node of VCO with too large parasitic capacitance.

B. Output Matching

Output matching circuit has to be considered that the balance between the output voltage swing and impedance matching. In order to achieve impedance matching, it needs to choose the large working current, which can be produced by two same size NMOS transistors. Considering the output voltage swing and the impedance matching, the value of load resistance should be 100Ω, then the range of differential output voltage can be 400mV. The reason of that do not choose diode connected form of PMOS transistors is that such load will introduce larger parasitic capacitance, and will give greater impact on the imaginary part of output impedance.

IV. SIMULATION RESULT

The simulation of circuit is completed in the Cadence design environment.

A. Center Frequency

Center frequency is 2GHz, it can achieve through changing the value of MOS capacitor. The waveform is shown in Fig.4.

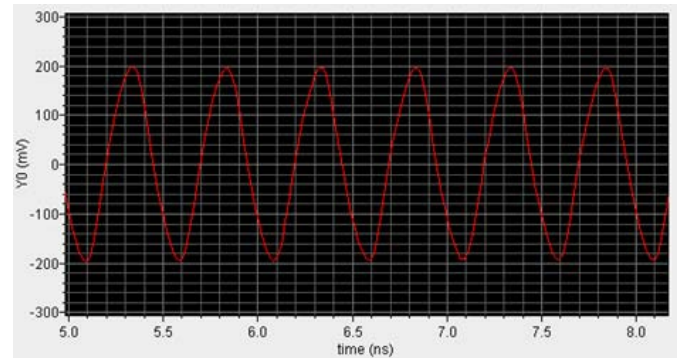Fig.4 Center frequency

B. Tuning Range

Frequency tuning is controlled by regulating voltage V_{CON}, this request the range is $0V \leq V_{CON} \leq 3V$. In his paper $1V \leq V_{CON} \leq 2.5V$ can achieve 2.05GHz~1.95GHz frequency changes, as shown in Fig.5. The differential output voltage swing can achieve 400mV when tuning different frequency, as shown in Fig.6.
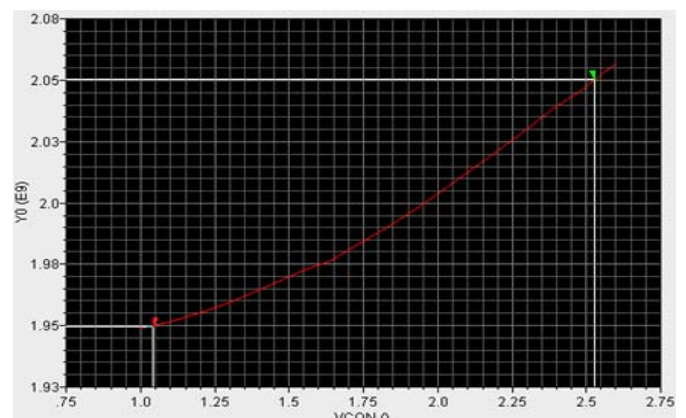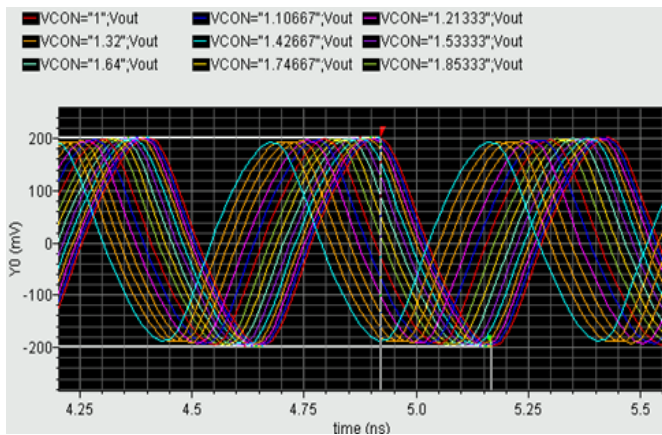

Fig.5 Control voltage-frequency curve

Fig.6 Output swing with different value of V_{CON}

C. Phase Noise

Because the tuning MOS capacitor almost has no effect on whole circuit, when changing the working frequency, the phase noise almost has no change. The phase noise is shown in Fig.7.
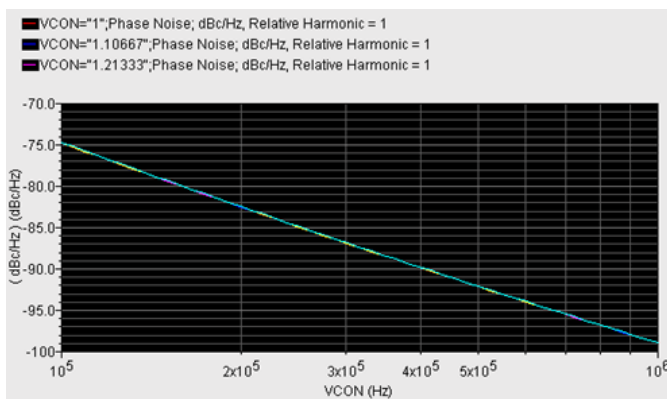

Fig.7 Phase noise with different value of V_{CON}

V. GENERAL

The paper describes a 2GHz fully differential ring voltage controlled oscillator based on 0.18μm CMOS technology. The tuning range is 100MHz, the supply voltage is 3V, and the power consumption of VCO core is 21mW. After further improvement it could be wider tuning range. The design has positive effect on the study and application of the voltage controlled oscillation in the wireless communication systems.

REFERENCES

[1] Razavi B. Design of analog CMOS integrated circuits, New Yorks, McGraw-Hill, 2001.

[2] Chi Baoyong, Yu Zhiping, Shi Bingxue. Analysis and design of CMOS RF integrated circuits, Beijing, Tsinghua University Press, 2006.

[3] Dou Jianhua, Liu Heting. Design of 1.56GHz ring VCO using 0.6μm CMOS technology. Instrumentation Technology, 2006, 6.

[4] Dou Jianhua, Zhan Feng, Wu Xi. Design of a voltage-controlled oscillator based on MOS capacitance. Journal of Hefei University of Technology, 2006, 6.

[5] Wu Chunhong, Zhu En,Wang Xueyan, Yu Weijia, Cheng Shudong, Wang Zhigong. 6GHz ring VCO design using 0.18μm CMOS technology. Chinese Journal of Electron Device, 2003, 12.

[6] Razvan Ionta, Mihai Sanduleanu, Andrei Vladimirescu, Dan Steriu. Ring oscillator based on R-NMOS logic with Back-Gate control. 2006 IEEE International Conference on Volume 1, Issue, May 2006 Page(s): 255 - 258.