# Design of A 2GHz Low Phase Noise LC VCO

Lu Peiming, Huang Shizhen , Song Lianyi , Chen Run

***Abstract*—A design of a integrated LC-VCO which is used in the phase-locked loop frequency synthesizer is presented. We reduce the phase noise effectively presupposes the tuning range. The VCO is realized by using the technology of tsmc CMOS 0.18um. The whole circuit is completed under the environment of CANDENCE, the result shows that the phase noise is -108dbc/Hz @100KHz and -131.9dbc/Hz@1MHz. The working voltage is 3V, and the working current is 5mA.**

**Key Word: Low Phase Noise, LC, VCO, Design**

## I. INTRODUCTION

Voltage controlled oscillator is widely used to generate the local oscillator carrier signals for both up-conversion and down-conversion mixing of the input baseband and RF signal. The challenges in implementing a fully integrated VCO with on-chip LC resonator for portable application constitute of achieving low phase noise, high tuning range and low power consumption.

The phase noise times power consumption product depends primarily on the quality factor of the tank. The best phase noise, for a given power consumption, in CMOS VCO has been obtained by using bondwire inductors. [1] But the large spread of bondwire inductors make practically impossible due to its limited tuning range. Spiral inductors feature less spreads making the tuning of the tank variations more feasible. But the Q values in standard digital CMOS processes is much lower, this brings bad phase noise to the VCO. In this paper, the VCO is completed with a symmetric inductor instead of two standard symmetric inductors. Compared to the standard inductors, a symmetric inductor can save much more area, what is the most important is that, a symmetric inductor has higher Q values compared to two standard inductors. In order to reduce the consumption of the inductor, the values of the inductor used in the circuit should be as small as possible.

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This paper is organized as follows. The circuit design is presented in section 2, the discussion of the measured results is carried on in Section 3, the conclusion is presented in Section 4.

## II. CIRCUIT DESIGN

### *A. LC-VCO Basic*

A general LC-VCO can be symbolized as in Fig.1. The oscillator consists of an inductor and a capacitor, building a parallel resonance tank and an active element –R, compensating the losses of the inductor and the losses of the capacitor. As the capacitance is proportional to a tuning input voltage, the circuit results in a VCO with angular center frequency.

We can change the resonance frequency by changing the value of C, and the tuning range is also determined. In a circuit the capacitance C includes either the tuning capacitance to the parasitical capacitance of the inductor, the nod capacitance of MOSFET, and the exteral load capacitance etc.

From Fig.1, we can conclude that the phase noise is mainly determined by the quality value of the tank. As far as present IC technics, the quality value of an inductor determines the Q value of the tank. There are two kinds of indutors in IC technics, the spiral inductor and the bondwire inductor. The bondwire inductor has high Q values, but the large spread of bondwire inductors make it practically impossible to tune out the components variations with a standard p-n varactor, due to its limited tuning range. Spiral inductors, instead, feature less spreads making the tuning of the tank variations more feasible. On the other hand, spiral inductors in standard digital CMOS processes feature much lower Q values. This mandates higher power consumption, for the same phase noise. In this design, we use a symmetrical inductor instead of two serial inductors to save the area. Besides, the Q value of the tank is much higher.

*B. The Phase Noise Model*

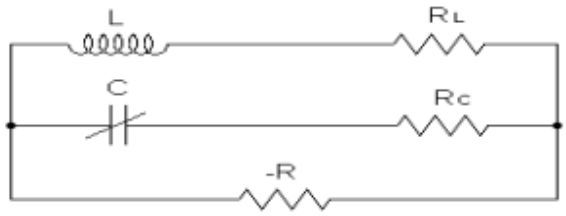


Figure 1. Basic LC resonator tank.

Commonly, the tuning voltage of the oscillator is high, which makes the MOSFET on and off periodically. So the oscillator is a nonlinear time- mutative system., we can not analyse the phase noise using the linear time-inmutative model. Analysing the phase noise is a much difficult work.. The most famous phase noise model[2] is expressed by Leeson, we can expressed it as in :

$$L(\Delta\omega) = 10\log\{\frac{1}{2}\frac{FKT}{Pc}[1+(\frac{\omega 0}{2Q_L})^2](1+\frac{\omega c}{\Delta\omega})\} \quad (1)$$

This formula can not be used to forecast the phase noise of a circuit, Real changed the parameter F to improve the utilization of the formula just as (2):

$$F = 1+\frac{4\gamma RI}{\pi Vo}+\gamma\frac{4}{9}g_{mbiasR} \quad (2)$$

The first item shows the contribution of the LC tank to the phase noise, the second one shows the contribution of the negative resistance crosscoupled pairs, the third one shows the contribution of the current source.

## III. Design and Analysis of the Circuit

The main circuit is expressed as figure 2. The differentially tuned LC-VCO can reduce the effect of the common-noise on the control input signal and extend the tuning range of the VCO which is important for low voltage operation. The differentially tuned LC-VCO is adopted reduce the power consumption of the VCO, the current in VCO is limited to about 7mA in the design, so the VCO works in the current-limited region [3]. The structure of complementary NMOS and PMOS crosscoupled pairs which can provide more excellent phase noise performance in current-limited region [4] is chosen as shown in figure 2. The current of the VCO is provided by the on-chip bandgap circuit, and the fully-integrated VCO can be realized.

The varactor is realized by using accumulation MOS varactor. The PMOS transistors and the NMOS transistors constitute the cross-coupled pairs respectively. They generate the negative resistance to cancel the loss in the LC tank. The inductor L is a symmetrical inductor. The quality factor of the symmetrical inductor gets to about 10 at 2 GHz. The bias current is provided by the NMOS transistor.

The Q value of the tank is mainly determined by the inductor, so we can make the Q of the tank as follows:

$$Q \approx Rp/\omega L \quad (3)$$

The frequency of the LC tank and the tuning voltage of the oscillator are calculated as follows.

$$\omega_o = 1/\sqrt{LC} \quad (4)$$

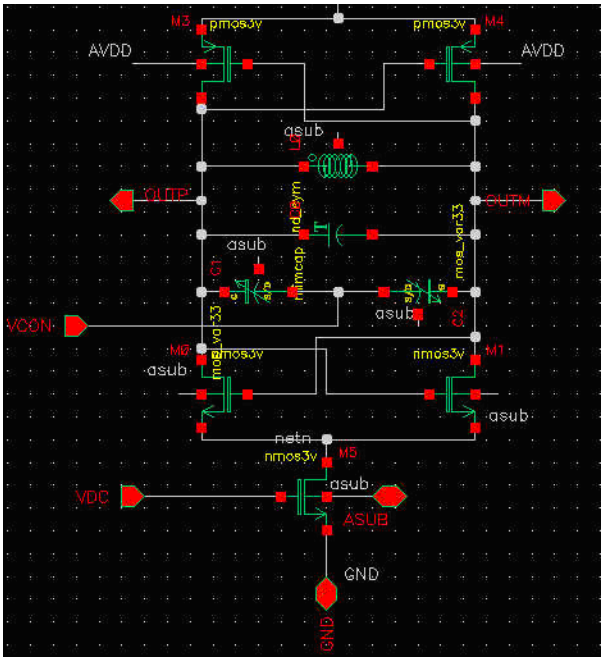


Figure 2. The schematic of the VCO.

$$Vo = 4IRp/\pi \quad (5)$$

So we can bring [3],[4],[5] to [1][2]and receive the phase noise model of the circuit just as follows:

$$L(\Delta\omega) = 10\log\frac{2FKT}{(4I/\pi)^2}\frac{1}{LQ^3}\frac{\omega_o}{\Delta\omega^2} \quad (6)$$

$$F = 1+\gamma+\gamma\frac{4}{9}g_{mbiasR} \quad (7)$$

From (6)(7), we can include that if the phase of the current source is eliminated, the phase noise of the oscillator will be the best.

## IV. Simulation and Result

This work is realized under the technical of TSMC0.18um, the simulation instrument is Candence SpectreRF. The voltage is 3V, and the current is 7mA, The layout of the circuit is expressed in figure 3. The tuning voltage is expressed in figure 4. We can see that the wave shape is absolutely different, and has no common module. The rising wave and the falling wave are almost symmetrical. The waveform of the phase noise

simulation is expressed as in figure 5. and the tuning range is 200M just as expressed in figure 6.

Table 1 summarizes the circuit measuring result of the work and other LC-VCO of recent literatures. From the table, we can see that the noise performance is comparatively better than the others.

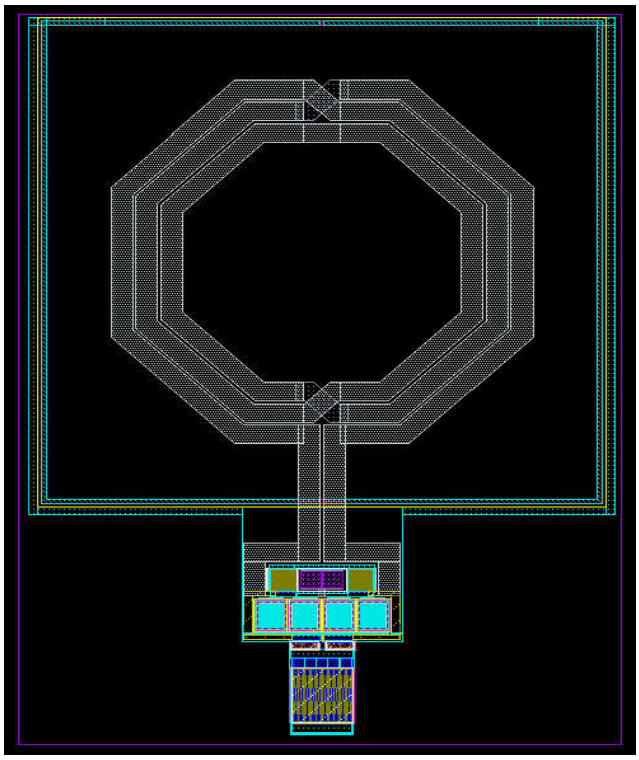

Figure 3. The layout of the VCO.

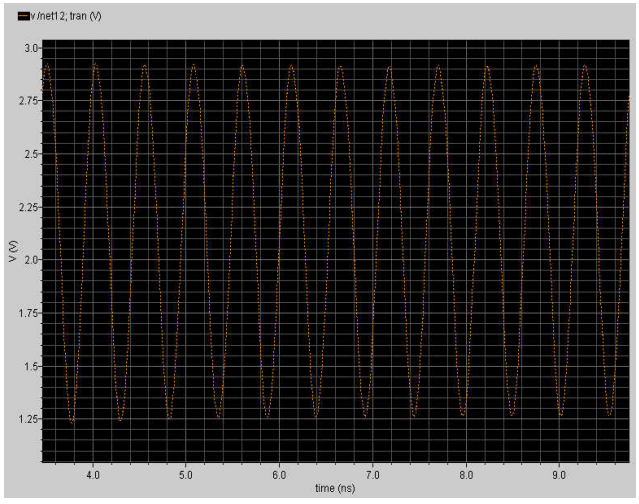


Figure 4. Simulation of the output voltage

## V. CONCLUSION

A differentially tuned low phase noise CMOS monolithic LC-VCO with a tuning range of 10% is presented in this paper. We put the phase noise to the first place. The symmetrical inductor is used to minimize the phase noise and the area. Simulation results have shown that the phase noise of the VCO is excellent.

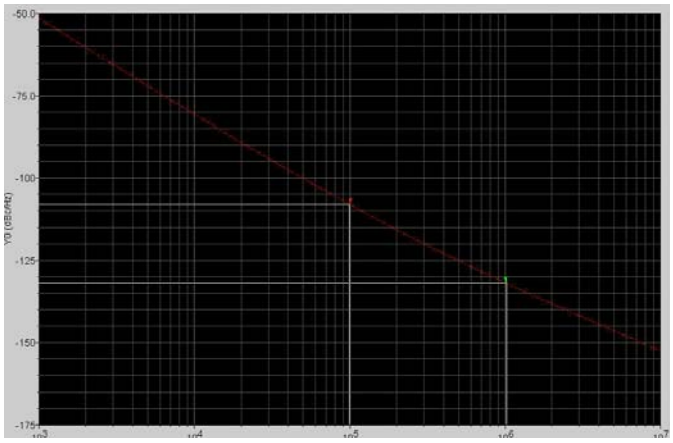

Figure 5. Waveform of the phase noise

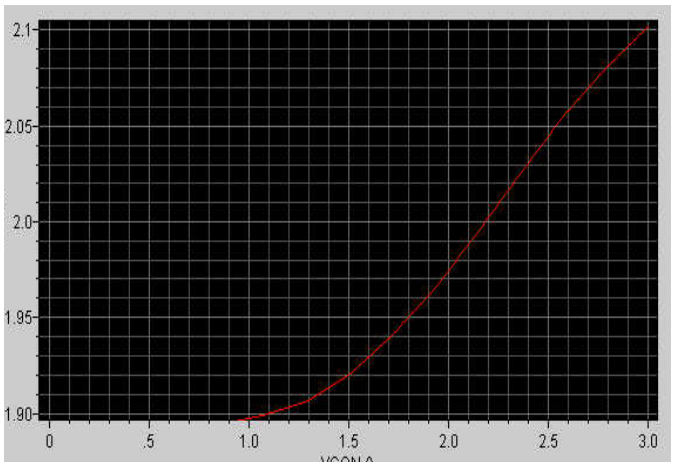

Figure 6. Waveform of the tuning range

TABLE I. COMPRARITION OF THIS WORK WIHE OTHER WORKS

| Ref | Tech (CMOS) | Center freq (GHz) | Power (mW) | Tuning Range | PN@ 1MHz offset (dBc/Hz) |
|---|---|---|---|---|---|
| [5] | 0.18um | 4.4 | 4.9 | 41% | -110 |
| [6] | 0.18um | 2.4 | 1.8 | 5% | -100.2 |
| [7] | 0.35um | 6 | 18 | 17% | -94 |
| This | 0.18um | 2 | 15 | 10% | -131.9 |

## ACKNOWLEDGMENT

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## REFERENCES

[1] J.Craninckx and M.Steyeart, "A 1.8GHz CMOS low-phase noise voltage-controlled oscillator with prescaler," IEEE J. Solid-State Circuits, vol.30,pp.1474-1482,Dec.1995.

[2] Lee T H, "The Design of CMOS Radio-Frequency Integrated Circuits(Second Edition)," U.S.A. :Cambridge University Press,2004.

[3] A. Hajimiri and T. H. Lee, "A general theory of phase noise in electrical oscillators," IEEE J. Solid-State Circuits, vol. 33, no. 2, pp. 179C194, Feb. 1998

[4] B. De Muer, "CMOS monolithic fractional-N frequency synthesizers, " Ph.D. dissertation, KU Leuven, 2002.

[5] A. Fard, T. Johnson, and D.Aberg, "A low power wide band COMS VCOfor multi-standard radios," IEEE R Adio and Wireless Conf., Sept. 2004, pp.79-82.

[6] Jie Long,Jo Yi Foo and Robert J. Weber, "A 2.4GHz Low-Power Low-phase-Noise CMOS LC VCO," IEEE omputer Society Annual Symposium on VLSI Emerging Trends in VLSI Systems Design, 0-7695-2097-9/04,2004.

[7] B.Razavi, "A study of phase noise in CMOS oscillators," IEEE Journal of Solid-state Circuits,vol. 31,no.3,pp.331-343,Mar.1996.