Design and Implementation of 8K-bits Low Power SRAM in 180nm Technology

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*Abstract-***This paper explores the tradeoffs that are involved in the design of SRAM. The major components of an SRAM such as the row decoders, the memory cells and the sense amplifiers have been studied in detail. The circuit techniques used to reduce the power dissipation and delay of these components has been explored and the tradeoffs have been explained. The key to low power operation in the SRAM data path is to reduce the signal swings on the high capacitance nodes like the bitlines and the data lines. Clocked voltage sense amplifiers are essential for obtaining low sensing power, and accurate generation of their sense clock is required for high speed operation. The tracking circuits essentially use a replica memory cell and a replica bitline to track the delay of the memory cell over a wide range of process and operating conditions. We present experimental results from two different prototypes. Finally an 8Kb prototype SRAM has been designed and verified. This design incorporates some of the circuit techniques used to reduce power dissipation and delay. Experimental data has been provided which shows the effectiveness of using the resetting scheme for the row decoders. While designing the SRAM, techniques such as circuit partitioning, gate oxide thickness variations and low power layout techniques are made use of to minimize the power dissipation. The mask design of the constituent memory blocks is done using virtuoso tool, the DRC & LVS verified through Hercules/Calibre. The design was simulated at a clock speed of 500 MHz. The read access time was found to be 0.85ns while the write access time was found to be 0.42ns at pre-layout simulations. The total power dissipation was 10.232mW at pre-layout simulations. The read access time was found to be 1.23ns while the write access time was found to be 0.85ns at post-layout simulations.The total power dissipation was 20.521mW at post-layout simulations.**

Index Terms- **6T Cell, 8Kb SRAM, Full Chip Memory, Low Power, Memory Banking**

I. INTRODUCTION

Static random-access memory (SRAM) continues to be a critical component across a wide range of microelectronics applications from consumer wireless to high-end workstation and microprocessor applications. For almost all fields of applications, semiconductor memory has been a key enabling technology. It is forecasted that embedded memory in SOC designs will cover up to 90% of the total chip area. A representative example is the use of cache memory in microprocessors. The operational speed could be significantly improved by the application of on-chip cache memory that temporarily stored a fraction of the data and instruction content of the main memory.

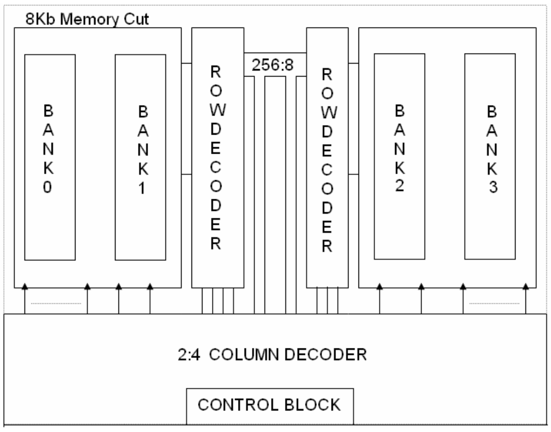

Fig. 1. Detailed View of 8Kb SRAM Memory

Semiconductor memory arrays capable of storing large quantities of digital information are essential to all digital systems. The ever-increasing demand for larger data storage capacity has driven the fabrication technology and memory development toward more compact design rules and, consequently, toward higher storage densities. This project deals with design of low power static random-access memory cells and peripheral circuits for standalone RAMs, in 180nm focusing on stable operation and reduced leakage current and power dissipation in standby and active modes.

The detailed view of the designed 8Kb SRAM memory block is as shown in Fig. 1, this total block is built up of two 4Kb memory cuts along with decoding sections and control logics for proper operation of the memory. In this project work, emphasis is laid on minimizing power consumption. The decoding logic is implemented as a tree (multi-stage path) to reduce power dissipation in active mode. To reduce the power in standby mode, adopting a multi-Vth technique reduces the leakage current [2].

As the technology shrinks (in Sub-micron technologies), the power issue becomes very prominent due to high transistor density, increased leakage currents and increase in interconnect parasitics. In spite of the cropping up of power issues, the power consumption can be reduced by adopting suitable techniques, such as circuit partitioning, increasing gate oxide thickness in non-critical paths, reducing Vth (dual Vth) etc. According to Benton H. Calhoun, Anantha Chandrakasan [2] an 180nm SRAM can be designed that functions into the sub-threshold region and examines the impact of process variation for low-voltage operation is described. He also depicts the impact of number of transistors and their structure on the leakage power of the memory bit cell. The circuit partitioning technique also improves the speed of our memory. The control block, the decoders and IO blocks are all in low Vth, whereas the memory cells, the dummy column and dummy row along with the sense amplifier are in high Vth [1]. Having this kind of configuration has helped in gaining in speed and also reducing the dynamic and static power consumption by a considerable amount

The concepts of variation of threshold voltages and increased gate-oxide thickness [4], for reduced leakage currents due to

Manuscript received December 29, 2008. This work was supported in part by the SV College of Engineering and Technology, Chittoor, Affiliated to JNTU, Hyderabad.

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subthreshold conduction and gate tunnel current are included, which assure the design of low-voltage random-access memory (RAM) cells and peripheral circuits for standalone SRAMs, focusing on stable operation and reduced subthreshold current in standby and active modes A number of researchers have studied the low power design of SRAM memories; they concluded that by circuit partitioning, variable Vth techniques and reducing capacitance along word lines, the power consumed in SRAM memories can be minimized.

A. Advantages and Uses of Low Power SRAM

1) 1.1.1 SRAMs are basically used as:

- Embedded memory, e.g.: First and second level caches in processors Data buffers in various DSP chips
- Standalone SRAMs: This can be integrated as an external memory during board design stage.
- Caches in computer systems Main memory in low power applications

2) 1.1.2 Advantages of SRAM memories:

- Faster Data Access speeds.
- Standby power of SRAM memories is very low inspite of high density of transistors.
- SRAM cells have high noise immunity due to larger noise margins, and have ability to operate at lower power supplies

II. MEMORY ARCHITECTURE

The preferred organization for Random access memories is shown in Figure. 2. This organization is random-access architecture which is an Asynchronous design. The name is derived from the fact that memory locations (addresses) can be accessed in random order at a fixed rate, independent of physical location, for reading or writing. The storage array, or core, is made up of simple cell circuits arranged to share connections in horizontal rows and vertical columns. The horizontal lines, which are driven only from outside the storage array, are called wordlines, while the vertical lines, along which data flow into and out of cells, are called bitlines. A cell is accessed for reading or writing by selecting its row and column. Each Cell can store 0 or 1. Memories may simultaneously select 4, 8, 16, 32, or 64 columns in one row depending on the application. The row and column (or groups of columns) to be selected are determined by decoding binary address information. For example, consider a row decoder that has 2 n out-put lines, a different one of which is enabled for each different n-bit input code. The column decoder takes m inputs and produces 2 m bit line access signals, of which any of them can be enabled at one time.

The bit selection is done using a multiplexer circuit to direct the corresponding cell outputs to data registers. In total, 2 n X 2 m cells are stored in the core array. In this design, the number of rows and columns are selected based on the control signals. Using two 4Kb memory cuts, an 8Kb SRAM memory is designed.

A. *SRAM Cell*

The basic static RAM cell is shown in Figure 3. It consists of two cross-coupled inverters and two access transistors. The access transistors are connected to the wordline at their respective gate terminals, and the bitlines at their source/drain terminals.

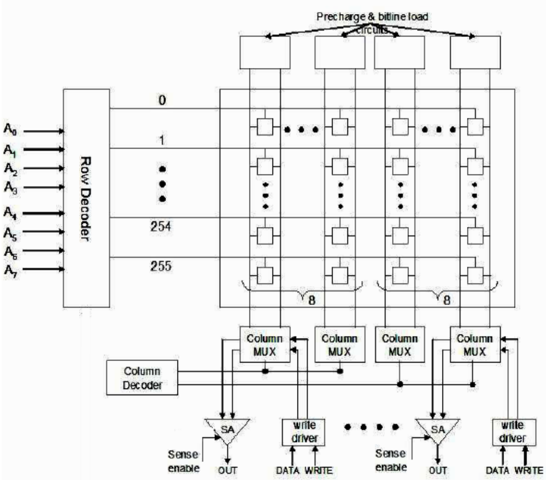

Fig. 2. SRAM Memory Architecture **[1]**

The wordline is used to select the cell while the bitlines are used to perform read or write operations on the cell. Internally, the cell holds the stored value on one side and its complement on the other side. For reference purposes, assume that node *q* holds the stored value while node holds its complement. The two complementary bitlines are used to improve speed and noise rejection properties. The VTC of cross-coupled inverters is shown in Figure 4. The VTC conveys the key cell design considerations for read and write operations. In the cross-coupled configuration, the stored values are represented by the two stable states in the VTC. The cell will retain its current state until one of the internal nodes crosses the switching threshold. When this occurs, the cell will flip its internal state. Therefore, during a read operation, we must not disturb its current state, while during the write operation we must force the internal voltage to swing past VS to change the state.

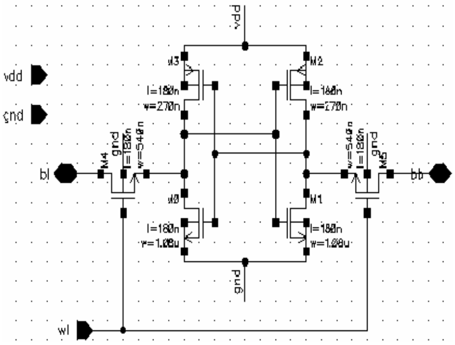

Fig. 3. SRAM Memory Cell

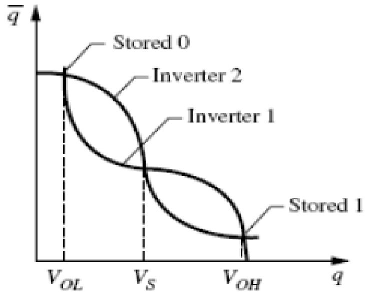

Fig. 4. VTC of 6T SRAM cell

The six transistor (6T) static memory cell in CMOS technology is illustrated schematically in Figure 3. The cross-coupled inverters, M1, M5 and M2, M6, act as the storage element. Major design effort is directed at minimizing the cell area and power consumption so that millions of cells can be placed on a chip. Subthreshold leakage currents control the steady state power consumption of the cell, so a larger threshold voltage is often used in memory circuits.

B. 2.2 Sense Amplifier Design

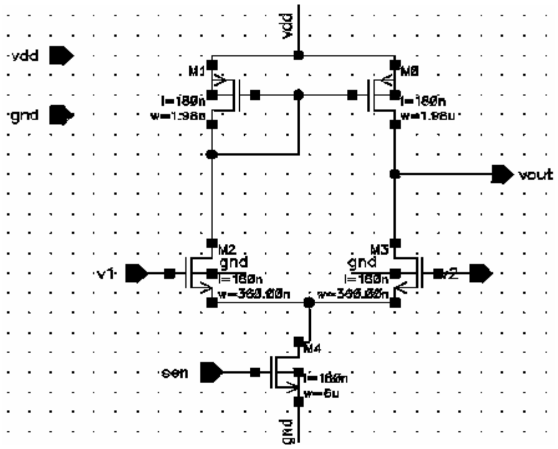

Fig 5. Differential Voltage Sense Amplifier

The most commonly used static voltage sense amplifier is shown in Figure 5. The main reason for using this type of sense amplifier is to improve the noise immunity and speed of the read circuit. Since the voltage swing on the bitlines is limited due to the large capacitances, any noise on these lines may cause an error in the reading process. In fact, any noise that is common to *b* and bbar should not be amplified. We are only interested in the differential signal changes between the two bitlines. The sense amplifier shown in Figure 5 attenuates *common-mode noise* and amplifies *differential-mode signals*. The circuit can be divided into three components: the current mirror, common source amplifier, and the biasing current source. All transistors are initially placed in the saturation region of operation so that the gain is large. They also use large values of channel length, L, to improve linearity. The two transistors, M3 and M4, act to provide the same current to the two branches of the circuit. That is, the current flowing through M3 is mirrored in M4: The main reason for using this type of sense amplifier is to improve the noise immunity and speed of the read circuit. Since the voltage swing on the bitlines is limited due to the large capacitances, any noise on these lines may cause an error in the reading process. In fact, any noise that is common to b and bbar should not be amplified. We are only interested in the differential signal changes between the two bitlines.

C. Precharge circuit

In both read and write operations, the bitlines are initially pulled up to a high voltage near VDD. The circuits used to precharge the bitlines depend on the type of sensing that is used in the read operation. A precharge signal, PC, is applied to the two pull-ups the two bitlines respected to their voltage levels. When the wordline (wl) signal goes high, one bitline remains high and the other falls at a linear rate until wl goes low. The difference between the bitlines is fed into a voltage-sensing latch-based amplifier that is triggered when the differential voltage exceeds a certain threshold.

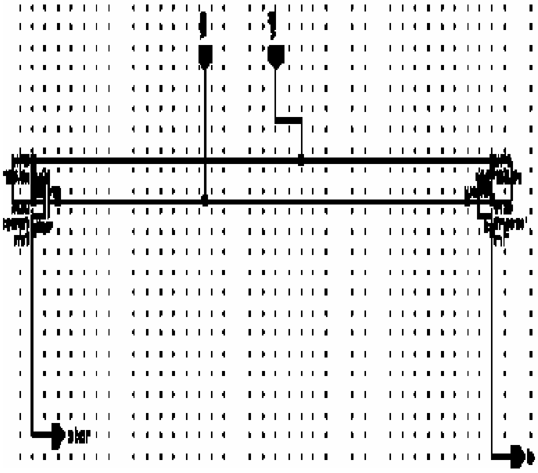

Fig 6. Precharge circuit

The precharge circuit shown in Figure 6 is reminiscent of the pseudo-NMOS circuits.

D. Memory Control unit

The control unit allows the data to either be written into the memory cell, or it passes the data from the bitlines onto the sense amplifier. The control unit was designed using pass gates. The sizes of the transistors were chosen, so that they are wide enough to offer less resistance while being small enough to fit within the pitch of the memory cell. We have used PMOS transistors for the circuits that allow data to be read from the bitlines to the sense amplifiers, while we have used NMOS transistors to write the data onto the bitlines. The read and write signals along with the data line are also given as inputs to each block of the control unit. Figure 7 shows the schematic of the control unit for one bitline column.

In the design of the memory cell we had seen that the PMOS transistor which connects the bitline to the sense amplifier should be sized as 810*nm*. This is done so that the layout of the control unit fits within the pitch of the memory cell. NMOS transistors are used to write the data onto the bitlines. The working of the design is very simple. If the column decoder output is asserted and the write signal is enabled, then the data and databar is driven on to the bitlines. If the column decoder output is asserted and the read signal is enabled, then the data on the bitlines is read out into the sense amplifier. SPICE simulations were used to verify this design.

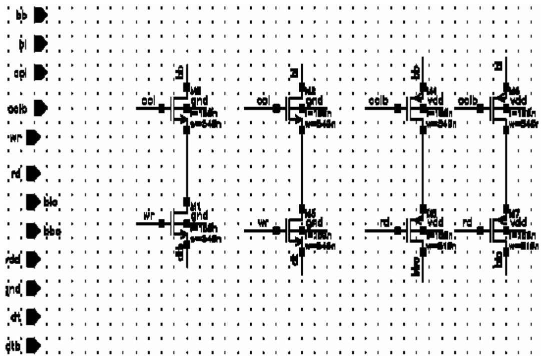

Fig 7. Memory Control unit

E. 2.5 Write Driver

Generally the bitline is discharged all the way to ground during a write operation. This huge bitline swing can cause large power consumption during writes. During a read operation, the bitline voltage swing is generally restricted to around 200mV, and thus the writes can on an average consume about 1/8th more power than a read operation. One method to reduce write power consumption has been proposed in [5] and involves partitioning the bitline into very small segments with very small capacitances.

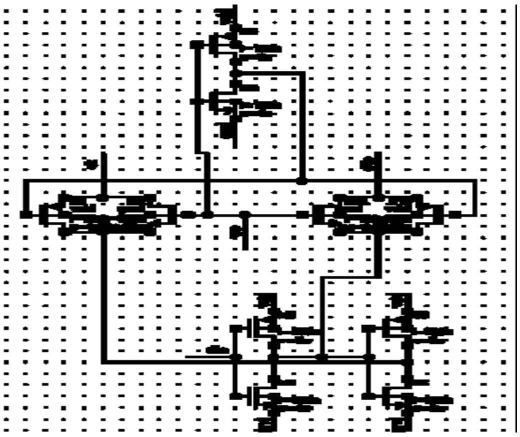

Fig 8. Write Driver Circuit

Another method proposes using small voltage swings in the bitlines to do the writes. However, the key problem in achieving writes using a small bitline voltage swing is to actually overpower the memory cell using such a small swing. The design also consumes quite a lot of area. We have gone for a very simple design, where the data and the databar are driven onto the bitlines mainly using inverters. Pass gate transistors which are enabled by the write signal allow these signals to be put on the bitlines. The major constraint on the size of the inverters is the area of the memory cells. We need to ensure that the write drivers fit within its pitch width.

F. *Dynamic NOR Decoders*

This NOR based decoders are used for both row and column decoders. The NOR decoder works like any other dynamic circuit. It requires a pre-charge cycle followed by the evaluation stage.

Pre-charge state: The 'Pre-charge' input is asserted which turns ON the PMOS devices and all the outputs of the decoder go to Vdd (Logic '1'). The decoder should not be read at this instant, since all the outputs will be at Vdd.

Evaluation Stage: Once the pre-charge is done, the PMOS device is turned OFF. The outputs will still be at Logic '1', because the charge will be stored on the capacitors. Now the inputs are applied on the three address lines. The corresponding NMOS devices will be turned ON and the charged capacitor on that line will be discharged to ground. Thus all, except one line will go to ground (Logic '0'). The line, which remains high, will be the decoded line and this line will drive all the NMOS transistors on that line. Thus the right data will be available on the data line. This data will be given to the output data block, which will return the correct data to the outside world when the OE (Output Enable) signal is asserted.

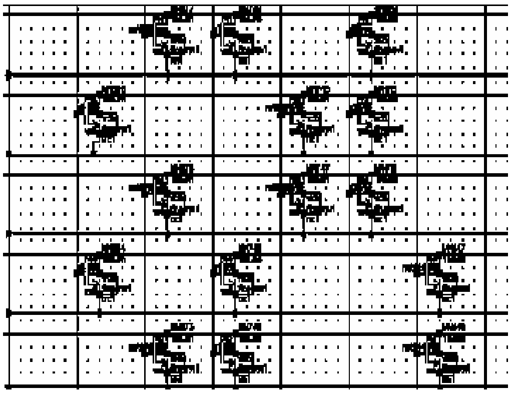

Fig 9. Dynamic NOR Decoder

III. LOW POWER DESIGN TECHNIQUES

In order to significantly reduce the power consumption in SRAMs all contributors to the total power must be targeted. The most efficient techniques used in memory are:

A. *SRAM Partitioning*

For large SRAMs, significant improvements in delay and power can be achieved by partitioning the cell array into smaller sub arrays, rather than having a single monolithic array. Typically, a large array is partitioned into a number of identically sized sub arrays (commonly referred to as macros), each of which stores a part of the accessed word, called the sub word, and all of which are activated simultaneously to access the complete word [1]. The macros can be thought of as independent RAMs, except that they might share parts of the decoder. This 4Kb SRAM divided into 4 banks and each bank having a capacity of 2Kb.when one bank is enabled remaining banks on in stand by mode. So power consumption is reduced into one by forth of original power consumption. Before partitioning power is 40.672mw after partitioning power is reduced to 20.423mw.

B. *DWL Architecture*

During an access to some row, the word line activates all the cells in that row and the desired sub word is accessed via the column multiplexers. This arrangement has two drawbacks for macros that have a very large number of columns: the word line RC delay grows as the square of the number of cells in the row, and bitline power grows linearly with the number of columns. Both these drawbacks can be overcome by further sub dividing the macros into smaller blocks of cells using the Divided Word Line (DWL) technique first proposed by Yoshimoto [1].

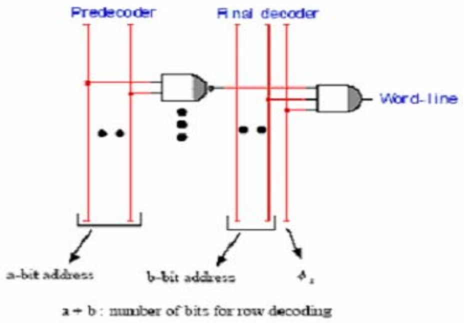

Fig 10. Basic Row Decoder

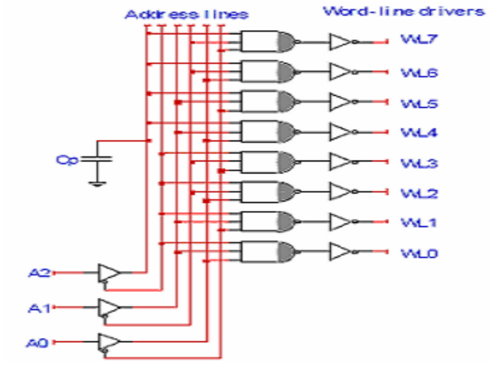

Fig 11. Two Stage Decoder Architecture

In the DWL technique the long word line of a conventional array is broken up into k sections, with each section activated independently thus reducing the word line length by k and hence reducing its RC delay by K2. Figure 2.1 shows the DWL architecture where a macro of 64 columns is partitioned into 4 blocks each having only 8 columns. The row selection is now done in two stages, first a global word line is activated which is then transmitted into the desired block by a block select signal to activate the desired local word line. Since the local word line is shorter, it has a lower RC delay. Before Divided Word Line (DWL) technique power is 20.423mw after Divided Word Line (DWL) technique power is reduced to 15.267mw.

C. *Low Power Decoders*

However, the normal decoder built using logic gates has the following drawbacks. The main problem is that the decoder will require a very large number of transistors. The capacitance associated with the long runs of wires and high gate input count will add to long delays. The address inputs will also have to be buffered to drive this huge capacitance load. The layout will become unnecessarily complex and so more time-consuming. Another problem is that the power consumption of such a decoder will be very high due to the large number of gates. SRAM chips are important components of embedded mobile systems, which generally run on batteries. It is very important to minimize the power consumption so as to maximize the life of the battery. To overcome these problems, we have used a dynamic NOR decoder. This structure reduces the number of transistors by half. It also increases the speed of the decoder and makes the layout simple and less time-consuming. Before low power decoders power is 15.267mw after using of low power decoder's power is reduced to 12.373mw.

D. *AC current reduction*

One of the circuit techniques that reduce AC current in memories is a multi-stage decoding. It is common that fast static CMOS decoders are based on decode architecture; the number of transistors, fan-in and the loading on the address input buffers is reduced. As a result, both speed and power are optimized. The signal generated by the pulse generator, enables the decoder and secures pulse activated word-line. This AC current reduction technique is implemented on OR/NOR and AND/NAND decoder architectures. The input buffers drive the interconnect capacitance of the address line and also the input capacitance of the NAND gates. By using a two-stage decode architecture, the number of transistors, fan-in and the loading on the address input buffers is reduced (see Figure 11.) when compared to the structure in Figure 10. As a result, both speed and power are optimized. The signal, generated by the pulse generator, enables the decoder and secures pulse activated word-line.

Before using decoder architecture power is 12.373mw after using of decoder architecture power is reduced to 11.530mw

E. *Process corners*

Notice how the SNSP corner is more extreme than the FNFP and TNTP corners. This is because some parameters like oxide thickness track for both flavors of transistors and therefore cannot improve one flavor while making the other flavor worse. Environmental variations, particularly of voltage and temperature, can make as much difference as processing. Therefore High and Low voltage and temperature corners are generally defined. For example, a chip normally operating at VDD=2.5 volts may use a high VDD of 2.75 and low VDD of 2.25. A high temperature may be 120 degrees C and a low temperature may be 0 degrees C for a part operating in the commercial temperature environment, since the actual transistor temperature on a hot die may far exceed the ambient temperature. Finally, an additional letter is sometimes added representing metal performance. Process tilt is becoming increasingly important, but is not yet well characterized for most processes. It comes from systematic and random variations of parameters across a die. Power dissipation of 8Kb SRAM with SNSP is 10.373mw, for FNFP and for TNTP 53.722mw and 70.245mw respectively.

F. *Low Power Layout Guidelines[11]-[12]*

- When beginning a cell layout, identify critical speed paths. These paths should be prioritized when designing the layout. Critical paths should follow these rules:
- Use poly only when necessary (as poly adds on lot of resistance).
- Do not jump signals in diffusion.
- Analog circuits, such as sense amplifiers, need to have matched layout in critical areas.
- Generally, any metal line adjacent to a wide bus should have greater than minimum spacing to avoid lithography problems. Also, signal lines running a long distance should have greater than minimum width to reduce series resistance.
- Do not place contacts across the width of power bus metal line. Doing so reduces the effective width on the bus. Calculate the effective metal line width by subtracting the width of contacts placed in the paths.
- All cells should be DRC and LVS clean (except for recommended rules) before they are called complete.
- To reduce edge capacitance on the output node, divide wide gates into an even number of legs with the output node to the inside and power to the outside. Each leg should be kept short in order to minimize series gate resistance.

IV. RESULTS AND DISCUSSIONS

A. *SNM of SRAM Cell*

The SNM value is determined most easily from simulation by forcing the voltage on one of the internal nodes of the cell (q) from ground to the power supply and recording the response of the other node (qbar). The setup of the simulation should be constructed with the worst-case contact resistances, including the cell's ground path. This diagram is referred to as "Butterfly" curve for the memory cell as shown in the below figure 12. The **SNM** is defined as the smallest diagonal of the two maximum squares that can he fit into the cross section of the VTC diagrams of the cross-coupled inverters. The SNM of the SRAM cell is calculated and it is 0.6v.

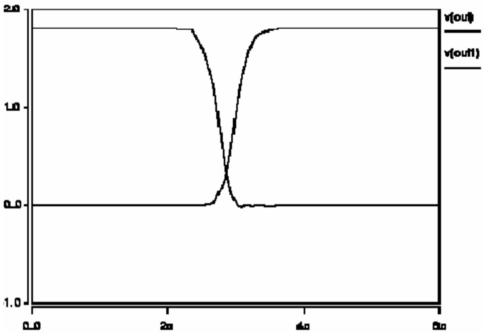

Fig 12. Butterfly Diagrams for 6T SRAM

B. *Simulations of Sense Amplifier*

The sense amplifier is enabled by using the replica bitline scheme based on capacitance ratioing. We have designed the replica bitline so that it enables the sense amplifier when the bitline voltage is 30mV. The sense amplifier was tested by varying the bitline voltage. Two voltage sources were used to vary the bitline voltage. The capacitance of the memory cells for a column was extracted from the layout and was found to be around 400fF. The parasitics of the bitlines have already been calculated in section 2.2 and these were used for this test as well. The simulations were run by varying the differential bitline voltages from 10mV to 200mV. In the below figure 13, BL is having a voltage of 1.14v and BLB having a voltage of 1.11v. So the difference voltage is 30mv, sense amplifier sense the difference voltage and produces the proper logic voltage.

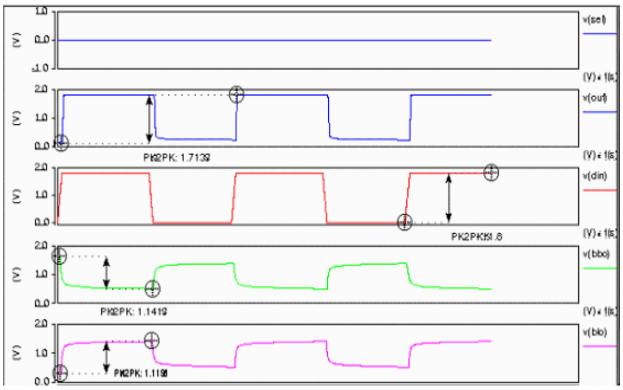

Fig 13. Waveform of Sense Amplifier

C. *Simulations of Precharge circuit*

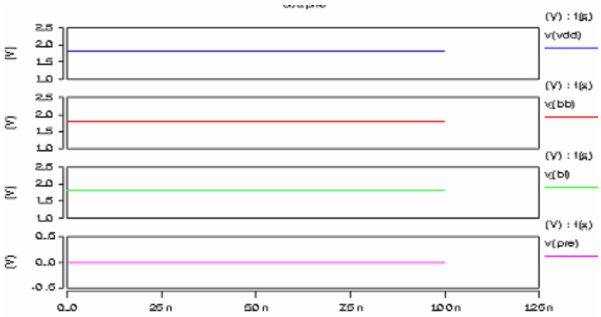

Fig 14. Waveform of Precharge Device.

The function of the precharge circuit is to charge the bit-line and inverse bit-lines (bit-line bar) to 1.8 V. The precharge enables the bit-lines to be charged high at all times except during write and read cycle.

D. *Simulations of Control Unit*

The control unit allows the data to either be written into the memory cell, or it passes the data from the bitlines onto the sense amplifier. The control unit was designed using pass gates. The sizes of the transistors were chosen, so that they are wide enough to offer less resistance while being small enough to fit within the pitch of the memory cell We have used PMOS transistors for the circuits that allow data to be read from the bitlines to the sense amplifiers, while we have used NMOS transistors to write the data onto the bitlines.

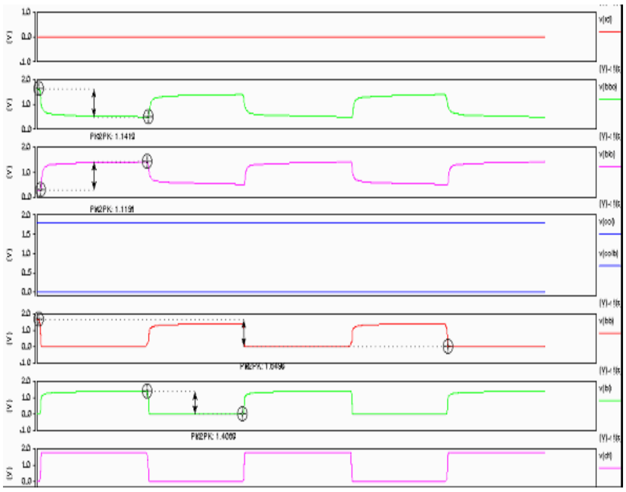

Fig 15. Waveform of Control Unit

The read and write signals along with the data line are also given as inputs to each block of the control unit. From the above figure 15 we can see that based on the control signals data written into memory and reading from the memory is happening.BL1 and BLB1 are the outputs which are given to the sense amplifier.BL2 and BLB2 are the outputs which are data going to written into the SRAM cell.

E. *Simulations of Write Driver*

Generally the bitline is discharged all the way to ground during a write operation. This huge bitline swing can cause large power consumption during writes. During a read operation, the bitline voltage swing is generally restricted to around 200mV, and thus the writes can on an average consume about 1/8th more power than a read operation. One method to reduce write power consumption has been proposed in [5] and involves partitioning the bitline into very small segments with very small capacitances.

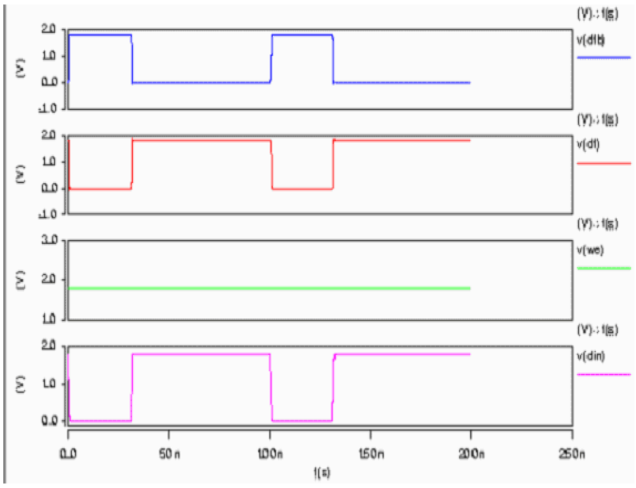

Fig 16. Waveform of Write Driver

F. *4.6 Simulation of Decoder Circuit*

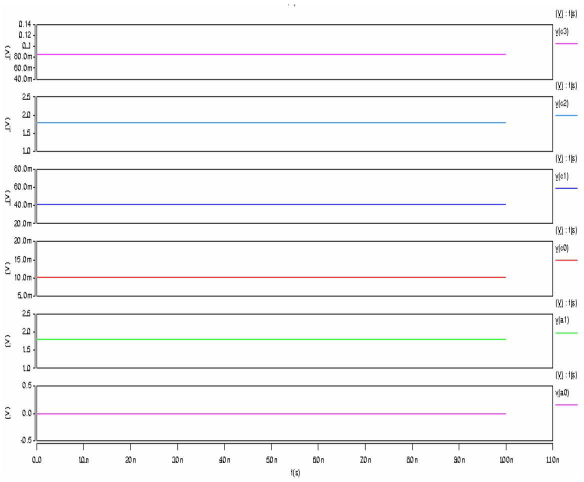

Fig 17. Waveform of 2:4 Column Decoders

In the above figure 17 S0, S1 are the control signals and C0, C1, C2, C3 are the outputs from the column decoder.S1S0=”10” is given so C2 column is enabled. The output which is shown below related to column decoder. Like column decoder row decoder also simulated with different inputs. For both row and column decoder NOR based decoders are used. Decoders which are built with logic of dynamic circuits reduce the power. Because, logic which has to be implemented are arranged by the NMOS transistors. PMOS transistors are used for precharge purpose only. So PMOS count is reduced in dynamic logic when compared to the CMOS logic.

G. *Writing Data into the 8Kb SRAM*

Different sequences of 1's and 0's were written into the memory array to make sure that the write circuitry works. Figure 18 shows the waveforms that were obtained when writing a ‘1’ and ‘0’ into the memory cell. As seen the when data ‘1’ is writing, once the write signal is asserted and the word line is pulled high, the Q node starts to rise to Vdd while the *Q* node starts dropping down to Gnd. The write access time is the time elapsed between a write request and the final writing of the input data into the memory. From simulations this was found to be 0.82ns.

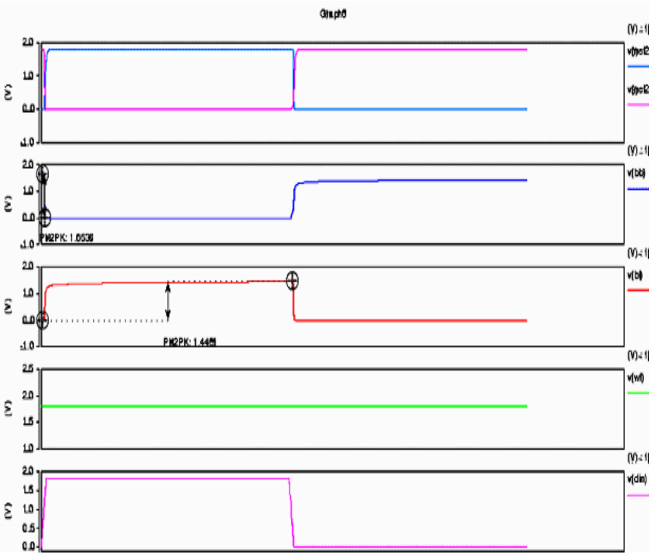

Fig 18. Simulation of 8Kb SRAM Write Operation

The write cycle is the minimum time required between write cycles. From the simulations this was found to be 1.2ns. The post-layout simulation of 8Kb SRAM write accesses time is shown in Figure 18.

Write Access Time = 53.928ns - 53.108ns

= 0.82ns

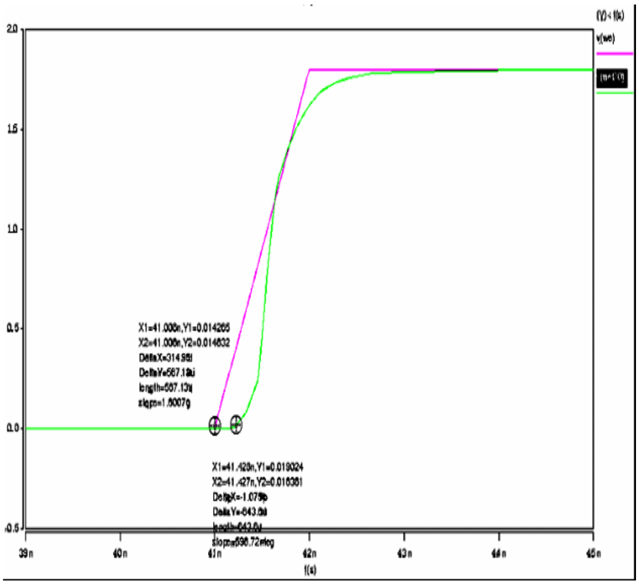

Fig 19. Waveform of 8Kb SRAM Write Access Time

H. Reading Data from the 8Kb SRAM

The data which is present in the memory array needs to be read out by the sense amplifier circuits which have to be enabled by the replica bitline circuit. During the read operation there are chances of the data getting destroyed.

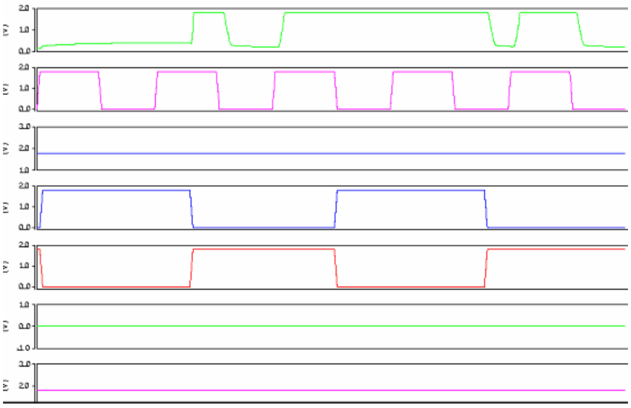

Fig 20. Waveform of 8Kb SRAM Read Operation

Figure 20 shows the waveforms that were obtained from the simulations. As seen when reading data logic ‘0’ or logic ‘1’ from the memory array, the voltage at node Q rises up to 30mV. This is however not sufficient to flip the contents of the memory cell.

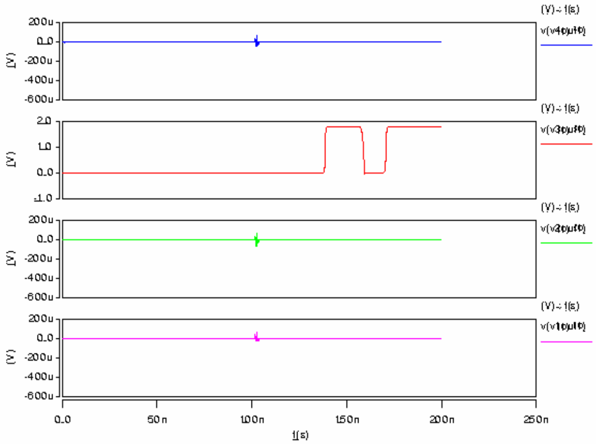

Fig 21. Waveform of Multiple Bank

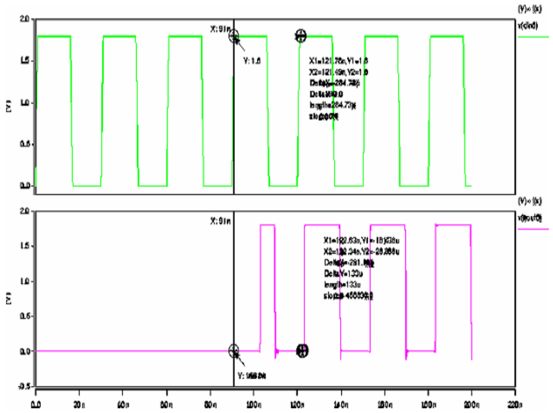

Fig 22. Waveform of Read Accesses Time

In the above Figure 21 we can see that bank-2 is in active mode and remaining banks are in stand by mode.

The read access time is the time taken to retrieve data from the memory cell. For our design the read access time was found to be 1.13ns. The read cycle is the minimum time required between successive reads. For our design this was found to be 1.4ns. The read cycle time is greater than the read access time since the bitlines need to be precharged before a read operation can be performed.

From the above figure 22 we can calculate the write access time that is given below.

Read Access Time = 251.78ns -250.55ns

= 1.23ns

I. Layout Drawn for the Design

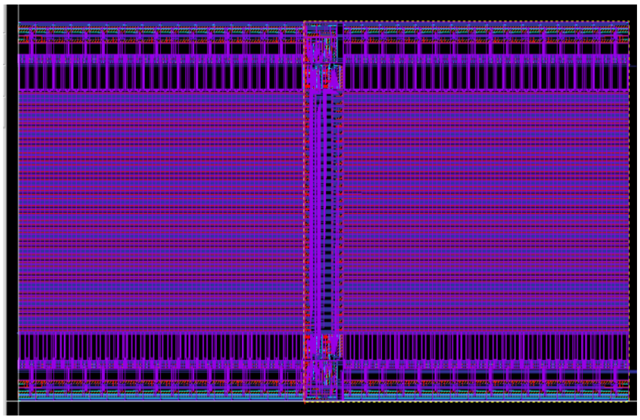

Fig 23. Layout of 8Kb SRAM

The layout was drawn for the design in .18 micron technology using Virtuoso®.

The layout was drawn for the design keeping in mind the usage of the block in other designs like ASIC or FPGA. The layout used up to 3 metal layers. So when this memory used at any ASIC designs blockage metal layers up to metal3.

V. SUMMARY OF RESULTS

The design described and it was tested to make sure that the designs worked as expected. Each block of the 8Kb SRAM was independently tested and the results verified. The designs were simulated across the process corners to make sure that they can withstand the process variations. Finally the entire design as a whole was simulated. For each design the RC delay of the interconnect wires was calculated using specific tools and these values were incorporated in the simulations. For 8Kb SRAM pre and post-layout simulations is completed and its comparison is given in below table 1. In the above table 1given results are worst case conditions. Different results are obtained when temperature is varied from -45^{0}C to 125^{0}C among them worst case conditions are shown in the above Table I.

Table I. Comparison of Pre and Post-layout simulation

Features	Pre-layout Simulation	Post-layout Simulation
Clock Speed	500MHz	500MHz
Power Dissipation	10.373mW	20.521mW
Read Accesses Time	0.85ns	1.23ns
Read Cycle Time	1.4ns	1.4ns
Write Accesses Time	0.42ns	0.85ns
Write Cycle Time	1.2ns	1.2ns
Area	1000umX1000 um	1000umX1000 um
Supply	1.8V	1.8V
Standby Current	13.2uA	14.7uA
Temperature	Military	Military

VI. CONCLUSION

This paper presents a 6T-based SRAM, which addresses the critical issues in designing a low power static RAM in deep sub micron technologies along with the design techniques used to overcome them. In this work the existing SRAM architectures are investigated, and then a basic 6T SRAM structure was chosen. The decoder, excluding the predecoder, is implemented as a binary structure by implementing a multi-stage path. For fast lower power solutions, the heuristic of reducing the sizes of the input stage in the higher levels of the decode tree allows for good trade-offs between delay and power. The SRAM access path is split into two portions: from address input to word line rise (the row decoder) and from word line rise to data output (the read data path). Techniques to optimize both of these paths are investigated and implemented. While designing the SRAM, techniques such as circuit partitioning, DWL architecture and low power layout techniques are made use of to minimize the power dissipation.

REFERENCES

[1] Bharadwaj S. Amrutur and Mark A. Horowitz , "*Speed and Power Scaling of SRAM's*", IEEE Transactions on Solid-State Circuits, vol. 35,pp. 175-185, no. 2, February 2000.

[2] Kenneth W. Mai, Toshihiko Mori, Bharadwaj S. Amrutur, Ron Ho, Bennett Wilburn, Mark A. Horowitz, Isao Fukushi, Tetsuo Izawa, and Shin Mitarai, "*Low-Power SRAM Design Using Half-Swing Pulse-Mode Techniques* ", IEEE Journal Of Solid-State Circuits, vol. 33, pp. 1659-1671, no. 11, November 1998.

[3] Bharadwaj S. Amrutur and Mark A. Horowitz, "Fast Low-Power Decoders for RAMs", IEEE Journal of Solid-State Circuits, vol. 36, pp. 1506-1515, no. 10, October 2001.

[4] Craig Lage, James D. Hayden and Chitra Subramanian, "Advanced SRAM Technology - The Race Between 4T and 6T Cells", Electron Devices Meeting, pp. 271-274, no.10, December 1996.

[5] Scott Doyle, Shankamarayanan Ramdswamy, Tri Hoang, Leonard Rockett, Tim Grembowski, and Adam Bumgamer, "*High Performance Radiation Hardened Static Random Access Memory (SRAM) Design for Space Applications*", IEEE Aerospace Conference Proceedings, vol. 4, pp. 2284 – 2293, no. 10, March 2004.

[6] O. Minato, "*2Kx8 bit Hi-CMOS static RAMs*", IEEE Journal of Solid State Circuits, vol. SC-15, no. 4, pp. 656-660, August 1980.

[7] Y. Kohno, "*A 14-ns 1-Mbit CMOS SRAM with variable bit organization*", IEEE Journal of Solid State Circuits, vol. 29, pp. 1060-1065, no. 9, October 1988.

[8] T. Chappell, "*A 2-ns Cycle, 3.8-ns Access 512-Kb CMOS ECL SRAM with a Fully Pipelined Architecture*", IEEE Journal of Solid State Circuits, vol. 26, pp. 1577-1585, no.11, November 1991.

[9] K. Sasaki, "*A 7-ns 140-mW 1-Mb CMOS SRAM with current sense amplifier*", IEEE Journal of Solid State Circuits, vol. 27, pp. 1511-1517, no. 11, November 1992.

[10] K.W. Mai, "*Low-power SRAM design using half-swing pulse-mode techniques*", IEEE Journal of Solid State Circuits, vol. 33, pp. 1659-1671, no. 11, November 1998.

[11] Sreerama Reddy G M and Dr. P. Chandrashekara Reddy, "*Negative Word Line Scheme Based Low Power 8Kb SRAM for Stand Alone Devices*", European Journal of Scientific Research, Vol. 26, No.2, Feb 2009

[12] Sreerama Reddy G M and Dr. P. Chandrashekara Reddy, "*Design and VLSI Implementation of 8Mb Low Power SRAM in 90nm*", European Journal of Scientific Research, Vol. 26, No.2, Feb 2009