Digitally Programmable Current Follower and Its Application

Tattaya Pukkalanun, Worapong Tangsrirat and Masahiro Yoshida

***Abstract*— A realization of the CMOS digitally programmable current follower (DP-CF) suitable for low-voltage high-frequency application is presented. To achieve very low input resistance, it is realized using a modification of a low-input resistance stage as an input stage. To achieve the precise digital control of the current gain, the current division technique is used. The proposed DP-CF can operate with low voltage supplies of ±1.5 V, and is designed with 0.5-μm CMOS SCN05H process. As an application, the digitally programmable current-mode rectifier using the proposed DP-CF is given. Simulation results are also included.**

***Index Terms*—Current Follower (CF), Current-Mode Circuits, Recytifier, Digitally Programmable.**

I. Introduction

The current follower (CF) is one of the most important and versatile current-mode building blocks for realizing many analog signal-processing applications. This is a well-known fact that it offers inherent wider bandwidth, wider dynamic range, simpler circuitry, and lower power consumption due to the current-mode nature of the performed signal processing [1]. In addition, the employment of CFs as active elements increases design simplicity as it offers the ability of virtually grounding admittance when they are connected to the CF input terminal. Another significant advantage of using CFs is that the voltage tracking error related active sensitivity problems are not taken into consideration because of virtual ground at the input terminal. Therefore, a carefully selected configuration can lead to reduction of active sensitivity problems caused by the sole exiting current-tracking error. Considering this fact, the CF has attracted considerable attention as alternative to other more complex building blocks in the implementation of filtering, immittance simulating and oscillator circuits [2]-[9].

The aim of this paper is, therefore, to present a novel CMOS current follower which provides the ability of digital trimming current gain. The proposed digitally programmable current follower (DP-CF) is realized through the modification of the low-input resistance input stage [10] and the current divider cell. It is shown that the circuit utilizes the current division technique to achieve precise digital trimming with no component spreading, and uses the current-mode approach to obtain low-voltage operation and high bandwidth. An application of the proposed DP-CF in realizing digitally programmable current-mode rectifier has been described. PSPICE simulation results based on the MOSIS 0.5-μm CMOS SCN05H parameters are in agreement with the presented theory.

Manuscript received January 7, 2009.

Tattaya Pukkalanun is with the Department of Control Engineering, Faculty of Engineering, King Mongkut's Institute of Technology Ladkrabang (KMITL), Chalongkrung road, Ladkrabang, Bangkok 10520, Thailand (e-mail: kptattay@kmitl.ac.th).

Worapong Tangsrirat is with the Department of Control Engineering, Faculty of Engineering, King Mongkut's Institute of Technology Ladkrabang (KMITL), Chalongkrung road, Ladkrabang, Bangkok 10520, Thailand (phone: +662-326-4205; fax: +662-326-4225, e-mail: ktworapo@kmitl.ac.th).

Masahiro Yoshida is with the Department of Embedded Technology, School of Information Science and Technology, Tokai University, Hiratsuka, Kanagawa 259-1292, Japan (e-mail: yoshida@tokai.ac.jp).

II. Proposed Digitally Programmable Current Follower

As shown in Fig.1(a), the CMOS realization of the proposed current division cell (CDC) is based on the use of the unity-gain current amplifier (M_1-M_6) with a very low-input resistance terminal [10] and a current divider circuit (M_7-M_{10}). The input terminal of this cell is held at virtual ground which results in a low-input resistance input stage (M_1-M_6). Based on the current division technique, the output currents (i_i, i_{oi} and $\overline{i_{oi}}$) of the proposed CDC related to the input current (i_{i+1}) can respectively be given by :

$$i_i = \frac{i_{i+1}}{2} \quad , \quad i_{oi} = a_i\left(\frac{i_{i+1}}{2}\right) \quad \text{and} \quad \overline{i_{oi}} = \overline{a_i}\left(\frac{i_{i+1}}{2}\right) \tag{1}$$

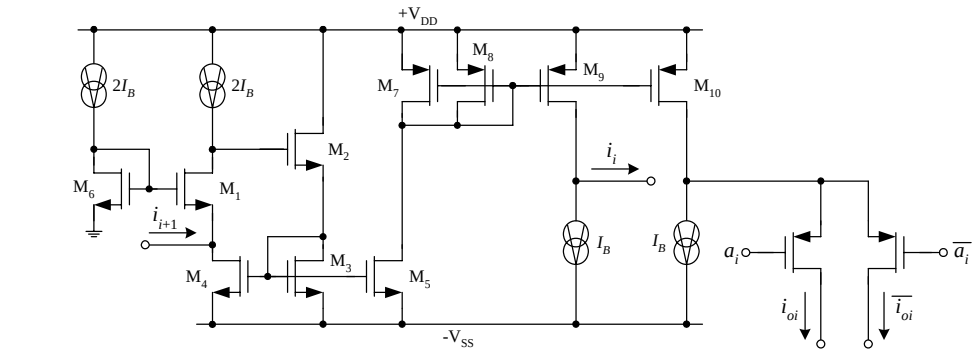
where a_i is the digital control bit of this cell. The circuit symbol of the CDC is represented in Fig.1(b).

Fig.2(a) shows the proposed DP-CF. It is realized through the cascading connection of n CDCs of Fig.1, where the output current i_j of the CDC_j (j = 1, 2, …, n) is used as an input current of the next stage. The output current (i_{out}) of the n-stage CDCs is then applied to the low-input resistance unity-gain current amplifier (M_{11}-M_{19}) to provide two output currents i_{out+} and i_{out-}. Therefore, by the action of the CDC network, two output currents of the proposed DP-CF can be expressed as :

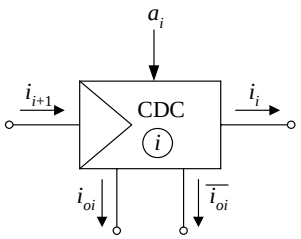
$$i_{out+} \cong i_{out-} = \alpha i_{in} \tag{2}$$

where

$$\alpha = \left(\frac{1}{2^{n+1}}\right)\left[1 + \sum_{i=0}^{n} a_i 2^i\right] \tag{3}$$

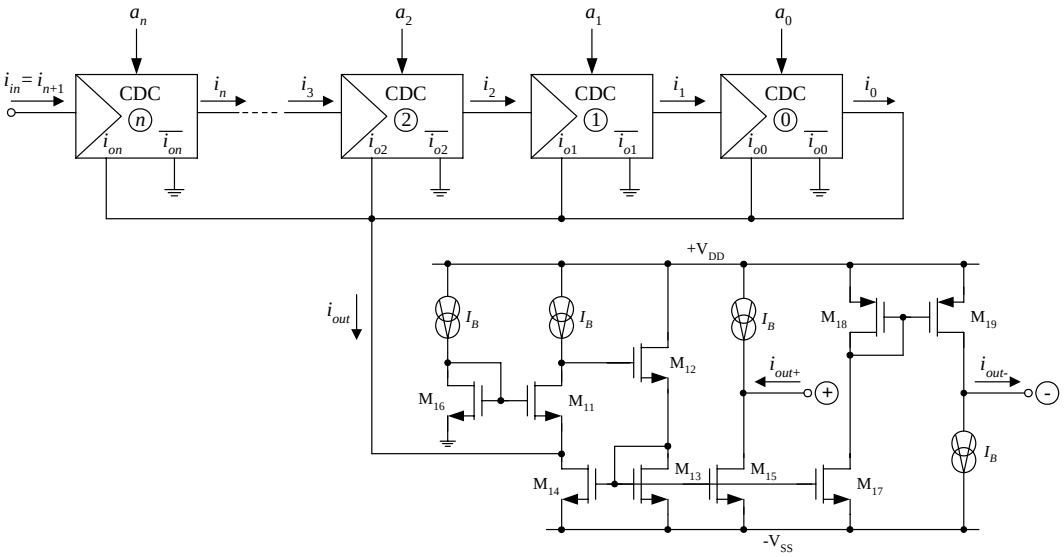


(a)

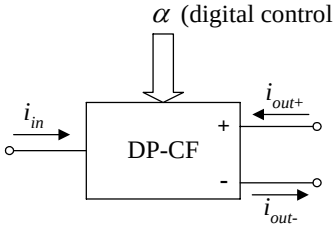


(b)

Fig.1 : Proposed CDC
(a) circuit diagram (b) its symbol



(a)



(b)

Fig.2 : Proposed DP-CF
(a) circuit diagram (b) its symbol

From equation (3), it is seen that the current gain (α) of the proposed DP-CF can be controlled digitally. The circuit symbol of the proposed DP-CF is also represented in Fig.2(b).

From Fig.2, it can be considered from the positive to the negative supply voltages that the proposed circuit uses only two MOS transistors and one bias current source. Therefore, the circuit can operate at a low power supply voltage of ($2V_{DSi} + V_{IB}$), where V_{DSi} and V_{IB} are the drain-to-source voltage of the MOS transistor and the voltage drop at the bias current source I_B, respectively. As an example, for the standard 0.5-μm CMOS process parameters, the threshold voltages V_{TN} and $-V_{TP}$ of the NMOS and PMOS transistors are about 0.64V and 0.91V, respectively. If the bias current sources I_B are realized by the basic current mirrors, as a result, the minimum supply voltage of about [2(0.64V)+(0.91V)] = 2.19V or ±1.095V can be used.

III. Simulation Results

The correct operation of the proposed DP-CF of Fig.2 has been evaluated through PSPICE simulation using the 0.5-μm CMOS SCN05H technology provided by MOSIS. The aspect ratios of the transistors used are W/L = 20μm/1μm for NMOS devices and W/L = 40μm/1μm for PMOS devices, respectively. The DC power supply voltages are chosen as $+V_{DD} = -V_{SS} = 1.5$V, and all bias currents I_B are set to be 100μA. The digital control input is $n = 3$ (4 bits).

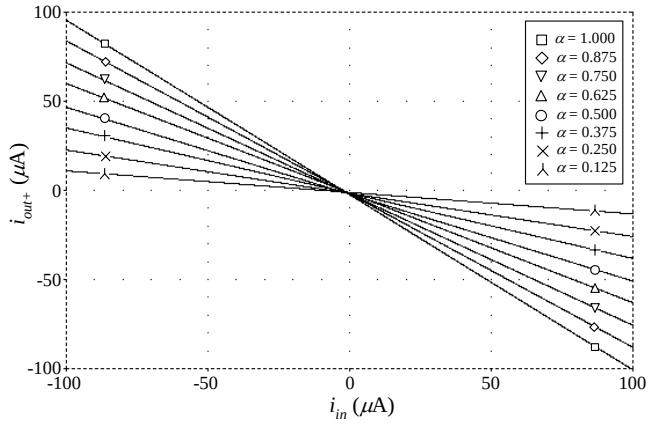


Fig.3 : DC current transfer characteristic.

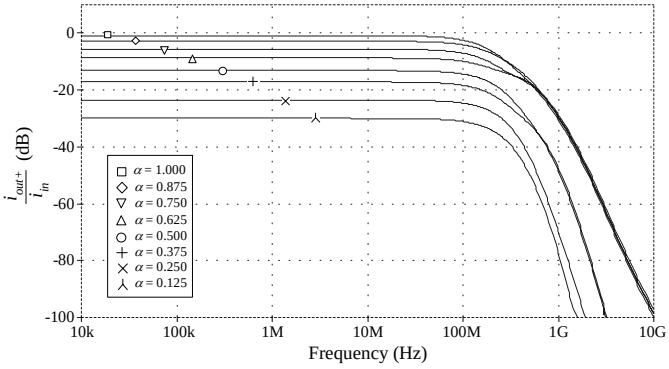


Fig.4 : AC current transfer characteristic (i_{out+}/i_{in}).

Fig.3 shows the DC current transfer characteristic of the proposed DP-CF given in Fig.2 when the input current i_{in} is varied from -100 μA to 100 μA for various values of the digitally-controlled current gain α scanning from 0.125 to 1.000 with a 0.125 step. It can be measured from simulations that the maximum offset currents are less than 5 μA. These offsets regarding theory values are mainly due to the effect of the current transfer error exhibited by the current mirror. With the same α scanning, the simulated AC current transfer characteristic of the proposed DP-CF is shown in Fig.4, from which its bandwidth of about 100 MHz is observed. All gain values are approximately changed from -30 dB to 0 dB.

IV. DP-CF Based Application

A digitally programmable current-mode full-wave rectifier can easily be configured using a single DP-CF as shown in Fig.5(a). This circuit is based on the well-known principle of precise current conveyor-based rectification reported in [11]. For the circuit realization, it is possible to use a MOS transistor connected as a diode as shown in Fig.5(b) [12]. Therefore, from the basic circuit operation, the expressions for the output voltages v_{o1} and v_{o2} can be given by :

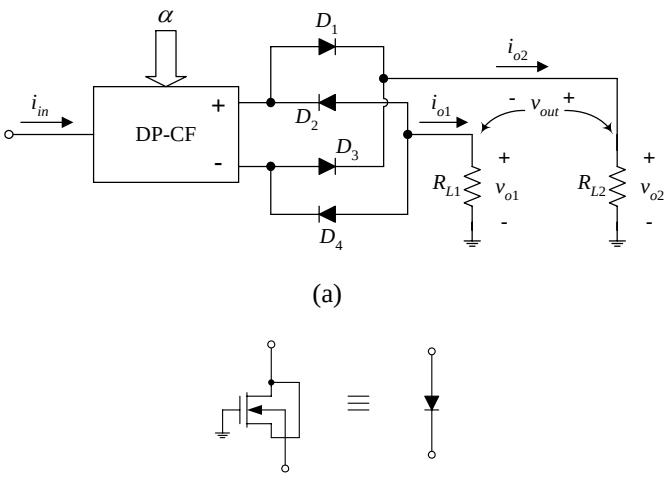
$$v_{o1} = -\alpha R_{L1}|i_{in}| \tag{4}$$

and

$$v_{o2} = \alpha R_{L2}|i_{in}| \quad . \tag{5}$$

As seen from equations (4) and (5), the amplitude of v_{o1} and v_{o2} can be adjusted digitally by the parameter α. Moreover, if $R_{L1} = R_{L2} = R_L$, the differential output voltage (v_{out}) of this circuit is equal to

$$v_{out} = v_{o2} - v_{o1} = \alpha 2R_L|i_{in}| \quad . \tag{6}$$



(a)

(b)

Fig.5 : Digitally programmable current-mode full-wave rectifier.
(a) circuit diagram (b) MOS connected as a diode.

Fig.6 displays the time domain responses of the rectified output waveforms obtained from the circuit of Fig.5(a) when the sinusoidal input current signal has 100-μA peak amplitude and 1 MHz. In Fig.6, the digitally controlled current gain parameter α is ranged from 0.250 to 1.000 in steps of 0.250 and $R_{L1} = R_{L2} = 10\ \Omega$. As seen from the figure, the circuit exhibits little imperfection up to frequencies close to 1 MHz. The amplitude error between the input and output signals is mainly caused by the offset current of the DP-CF element, which is mentioned previously.

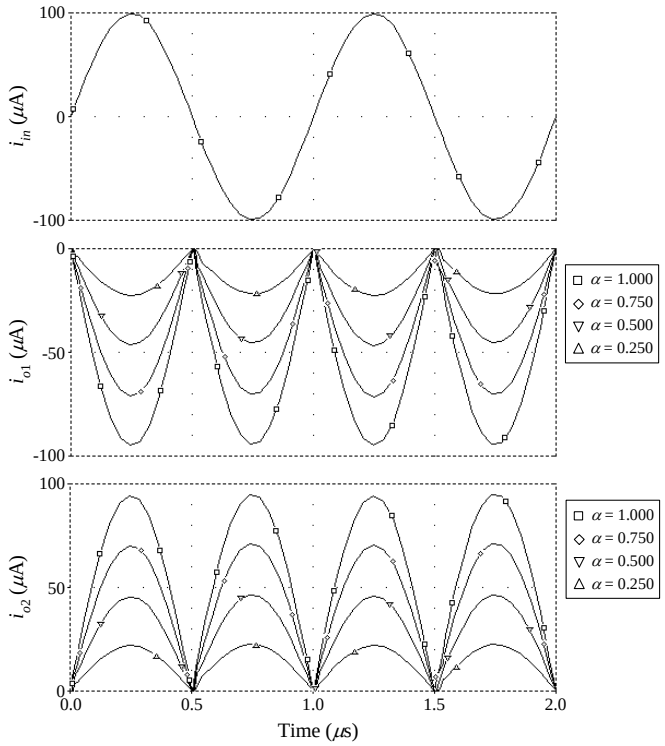


Fig.6 : Time domain responses of the digitally programmable current-mode full-wave rectifier of Fig.5(a) for different values of α.

V. Conclusion

In this work, the low-voltage DP-CF is proposed and simulation results are presented. The proposed DP-CF is based on a low-input resistance stage and a current division technique. The low-input resistance stage based on a negative feedback technique is employed as an input stage to provide very low input resistance. The current division cell is also proposed and used to provide the digital control of the current gain between input and output terminals of the proposed DP-CF. To demonstrate the versatility of the proposed device, a digitally programmable application is also included.

References

[1] C. Toumazou, F. J. Lidgey, D. G. Haigh, *Analogue IC design : the current-mode approach*, Stevenage, U.K. : Peter Peregrinus, 1990.

[2] S.I. Liu, J.J. Chen, and J.H. Tsay, "New insensitive notch and all-pass filters with single current follower", *Electron. Lett.*, vol.27, pp.1712-1713, 1991.

[3] S. I. Liu, J. J. Chen, H. W. Taso and J. H. Tsay, "Design of biquad filters with a single current follower", *IEEE Proc. G*, vol.14, pp.165-170, 1993.

[4] S. I. Liu, J. J. Chen, and Y. S. Hwang, "New current-mode biquad filters using current followers", *IEEE Trans. Circuits Syst. I : Fundamental Theory and Applications*, vol.42, pp.380-383, 1995.

[5] E. M. Drakakis, and C. A. Karybakas, "A multiple output active filter based on current followers", *Int. J. Electron*., vol.86, no.2, pp.141-151, 1999.

[6] R. Senani and S. S. Gupta, "New universal filter using only current followers as active elements", *Int. J. Electron. Commun. (AEU)*, vol.60, pp.251-256, 2006.

[7] A. U. Keskin, and A. Toker, "A NIC with impedance scaling properties using unity gain cells", *Analog Integr. Circ. Sig. Process.*, vol.41, pp.85-87, 2004.

[8] C. Psychalinos, and A. Spanidou, "Current amplifier based grounded and floating inductance simulators", *Int. J. Electron. Commun. (AEU)*, vol.60, pp.168-171, 2006.

[9] M. T. Abuelma'atti, "Grounded capacitor current-mode oscillator using single current follower", *IEEE Trans. Circuits Syst. I : Fundamental Theory and Applications*, vol.39, no.12, pp.1018-1020, 1992.

[10] W. Tangsrirat, K. Klahan, T. Dumawipata and W. Surakampontorn, "Low-voltage NMOS-based current differencing buffered amplifier and its application to current-mode ladder filter design", *Int. J. Electron.*, vol.93, no.11, pp.777-791, 2006.

[11] CCII01 current conveyor amplifier, Data sheet, LTP Electronics Ltd., Oxford, UK, 1993.

[12] A. Monpapassorn, K. Dejhan and F. Cheevasuvit, "CMOS dual output current mode haft-wave rectifier", *Int. J. Electron.*, vol.88, no.10, pp.1073-1084, 2001.