Optimal Scheduling Algorithm Using Hopfield Neural Network

Sun-Ho Jee, Yong-Chul Cho, Liang Zhang, Hyun-Chan Cho and Hee-Sun Kang

Abstract—**Multi-spinner is used in Photoresist process of semiconductor manufacturing. Photoresist process is the process of wafer deposal including wafer cleaning, surface treatment, Photoresist spread and Soft Baking. Though each successful process of this Multi-spinner equipment works by moving wafer, if optical scheduling applied to improve transfer path, it increases the volume of produced semiconductors. The main concern of paper is to optimize scheduling method using artificial neural network to solve scheduling problem of each processes of Multi-spinner. The effectiveness of optical scheduling is proved by computer simulation.**

Index Terms—— **Multi-Spinner, Neural Network, Optical Scheduling**

I. Introduction

In the semi-conductor manufacturing process, Photolithography is the process that determines integrations by forming very integrated pattern on wafers. In order to accomplish PR-forming process and Development in the Photolithography without Exposure process, it uses Multi-spinner equipments which use a spin method and Transfer Robot make the wafer movements.

Photolithography is composed by surface preparation which is improved adhesion with the wafer and PR and PR spread and Soft Baking which is removed solvent in PR. In this manufacturing process, transfer robot in multi-spinner moves wafers and as reducing process waiting time and scheduling the shortest distance, it can help to improve semiconductor product. Consequently, in PR forming process, it will be able to improve the productivity as transfer robot's wafer transfer course is optimized by scheduling.

CS unit in Multi-spinner is the equipment which supplies mass wafers. The transfer robot transfers wafers in CS unit in sequence when the transfer robot transfers each manufacturing process. At that time, the transfer robot stops due to difference of each process time. If the transfer robot transfers the nearest wafer in next process step instead of sequence, PR forming process completes in minimum process time. Therefore it is needed to optimize scheduling in CS for reducing process waiting time.

Manuscript received December 29, 2008.

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We know that the transfer robot's speed of multi-spinner is fixed with many examples. So, we can think that minimizing process time is similar to minimizing movement time.

In this paper, we suggest an artificial neural network to solve scheduling problem. The artificial neural network can calculate complex problem because it has advantage of arranging in a row structure that has difference type of existing method [2], [3].

We prove the efficiency of optimization scheduling of the artificial neural network by computer simulation.

II. Multi-Spinner's Constitution and System

Fig.1 shows a plane figure of Multi-spinner equipment system and Fig. 2 shows action steps of Multi-spinner.

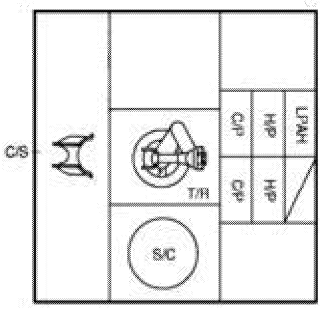

Fig. 1 System of Multi-Spinner[1]

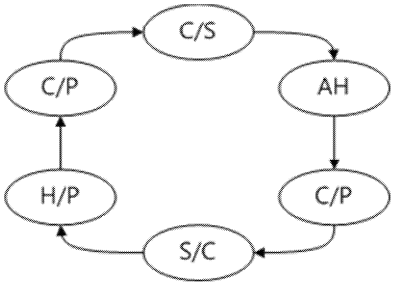

Fig. 2 Action step of Multi-spinner (PR-forming process)

The definition of every process is shown as follows:

CS: Cassette. A unit that has a lot of wafers in 1set.

AH: Low Pressure Adhesion Heater. A unit that injects HMDS(Hexa Methyl Di Silazane) gas to strengthen

CP: Cool Plate Baker. A unit that cools the heated unit processed by HP unit.

SC: Spin Coater. A unit that forms layer(film) on wafers.

HP: Hot Plate Baker. A unit that bakes wafers at high temperatures.

TR: Transfer Robot. A unit that conveys wafers.

Multi-spinner system does NOT arrange process flow as shown Fig. 2. Because that needs repeated process flow and efficient managements, the process structure of Multi-spinner is formed(shown as Fig. 1).

Because the robot inserts the second wafer after the whole process of the first one is finished, between the first unit processes the robot has to wait for the final end of the first process. So, in this case process time is longer and produce is reduced.

Existent system uses Shift way as shown Table I.

After 1st wafer of CS has done AH process, 1st wafer moves process of CP and 2nd wafer of CS moves process of AH, and if CP's process completes and 1st wafer moves Coater process, 2nd wafer moves process of CP, 3rd wafer moves process of AH. But, if process performs as above, halt happens after any process is completed. Because the process time of CS and HP are different. Under the influence, the whole processing time is prolonged.

Generally, by Shift method waiting time of each unit is decided by the longest unit process time. So according to each unit process time, transferring wafers that is filled to CS by AH process to near position of transfer robot, indeed, reduce total process time and help greatly to increase output.

Start	---------->					End
C/S	AH	C/P	S/C	H/P	C/P	C/S
1						
2	1					
3	2	1				
4	3	2	1			
5	4	3	2	1		
6	5	4	3	2	1	
7	6	5	4	3	2	1

Table I. Multi-Spinner's processing by shift method

Process	Ex)Time(sec)
AH	55s
C/P	55s
Coater	54.5s
H/P	90s
C/P	55s

Table II. ex) Processing time

III. Optimal Scheduling Algorism Using Hopfield Neural Network

In Multi-spinner equipment transfer robot can solve the problem of optimizing the path from the start slot S to the end slot D which has N wafers and L links by the graph method. Each link (*i, j*) has expense that correspond to what, when this sets path from node *i* to *j* node cost expense by matrix expression possibility do[4].

Define that series Multi-spinner's processes that connect *d*(end) and *s*(start) are P_{sd} route and if express this with (1), W_T which is total path process time in path P_{sd} are same with sums of times of each processes with (2).

$$P_{sd}: s \rightarrow i \rightarrow j \rightarrow k \cdots \rightarrow r \rightarrow d \quad (1)$$

$$W_T = W_{si} + W_{ij} + W_{jk} + \cdots + W_{rd} \quad (2)$$

Therefore, the target is optimal scheduling that can minimize the whole process time about path. General Multi-spinner's equipment makes transfer robot transfer wafers depending on order of each process by Shift method.

Table III. expresses Multi-spinner's process order and wafer transfer course of transfer robot. The horizontal axis means that wafer from the first to *Nth* is filled into CS slot and vertical axis means CS_i (process start) - > AH -> CS_i > CP1 - > SC -> CP2 - > HP – CS_i (process end) process order. Till the transfer process of wafers of *N* are completed, path of transfer robot passes through following process.

$$P_{11} \rightarrow P_{21} \rightarrow P_{31} \rightarrow P_{12} \rightarrow P_{22} \rightarrow P_{31} \rightarrow P_{41} \rightarrow P_{22} \rightarrow P_{32} \rightarrow P_{13} \rightarrow P_{23} \rightarrow P_{41} \rightarrow P_{51} \rightarrow P_{32} \rightarrow P_{42} \rightarrow P_{23} \rightarrow P_{33} \rightarrow P_{14} \rightarrow P_{24} \rightarrow P_{51} \rightarrow P_{61} \rightarrow P_{42} \rightarrow P_{52} \rightarrow P_{33} \rightarrow P_{43} \rightarrow P_{24} \rightarrow P_{34} \rightarrow P_{15} \rightarrow P_{25} \rightarrow P_{61} \rightarrow P_{71}$$

Until finishing one wafer in process, the transfer robot transport wafer by the process step. The transfer robot return previous process in order to transfer next *kth* wafer and have to get wafer.

Until finishing one wafer, the transfer robot doesn't finish each process once a time but does several unit process at the same time. Also transfer course of AH, CP1, SC, HP, and CP2 continually keep same course from one to *N* wafer. Occurrence of delay is occurred by CS slots' distance after getting CS slots' wafer and completing process. Also because each unit process time is different, delay time is occurred.

wafer number / process	1	2	3	4	5	…	N
CS_i	P11	P12	P13	P14	P15	…	P1N
AH	P21	P22	P23	P24	P25	…	P2N
CP1	P31	P32	P33	P34	P35	…	P3N
SC	P41	P42	P43	P44	P45	…	P4N
HP	P51	P52	P53	P54	P55	…	P5N
CP2	P61	P62	P63	P64	P65	…	P6N
CS_i	P71	P72	P73	P74	P75	…	P7N

Table III. Multi-spinner's process step

In order to calculate the shortest movement of transfer robot, the *kth* wafer and the *ith* wafer' transfer path are put to one process. So between every step the transfer time and distance are compared and calculated. If very step's time can be the smallest one, the move sequence of robot is achieved. Because the transfer robot move the arms to transfer wafers according to this sequence which is just like a M× N matrix. We can use hopfield neural network to find out the optimal process

A. Decision of each step optimal path in distance

Fig. 3 is example of transfer path until the process of one wafer is completed. And the number in figure is transfer path of transfer robot.

As referred before, transfer robot repeats same process. At that time, time lag is same with Table II.

1) Distance difference of wafers that is filled on CS slot : In Fig. 3, transfer distance of orders of 2 , 5, 11, 19, 29 at AH, transfer distance of orders of 4, 10, 18, 28 at CP1, transfer distance of orders of 31 at CP2

2) As you show Table II, waiting time of transfer robot by a process time difference of each processes

That is, wafers of *N* to fill on CS slot each distance and process waiting time of transfer robot by one step and calculate each step's minimum distance.

Have *kth* wafer and route of *ith* wafer two wafers on CS slot with Fig. 4 and in *kth* wafer of CS slot and AH distance, CP1 while respect age until wafer of *kth* is completed *ith* distance of CS slot, and Step of but wish to include waiting time of transfer robot by difference during time between distance and each process that *kth* wafer is filled on CS slot again in distance of *ith* wafer and AH, CP2 being completed, get into process waiting time by wafer *ith* if unite time of Steps of these each *N*.

At this time, Multi-spinner's transfer robot regards that time taken in distance is fixed with the example that is many.

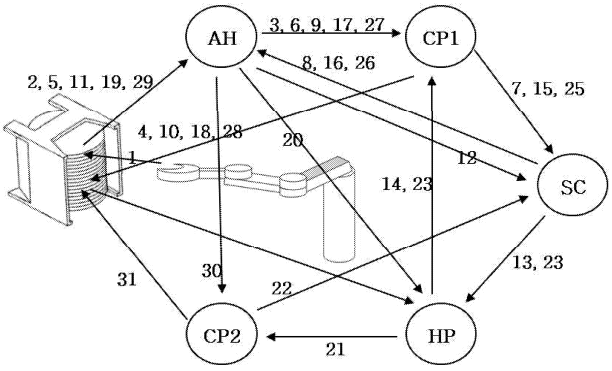

Fig. 3 One wafer process transfer path example of transfer robot until is completed
(Each number means transfer order of transfer robot.

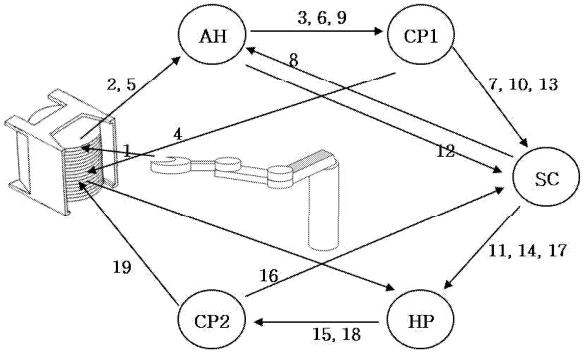

Fig. 4 Example of *kth* wafer and transfer path of wafer of *ith*.

That can be arranged as follows (3).

1) Difference during process time that is happened at each process : *L*
2) Time that bring *i* wafer in process: i_s
3) Time that have *i* wafer that complete process to CS: i_d
4) Time that take until *ith* that come back to process from CS *ith* to bring *kth* wafer: i_f
5) Time that bring k wafer by process in CS that process is begun: k_s

$$T_{ik} = L + i_s + i_d - i_f - k_s \qquad (3)$$

T_{ik} expresses time difference of when bring *ith* wafer and *kth* wafer and difference of process waiting time. This is, if reduces difference during time, waiting time decreases and last process time decreases.

B. Decision optimal path using Hopfield network

M × N steps of each *N* can appear by matrix, and *N* means quantities of wafer that is filled on CS slot, *M* means transfer robot is a process step. In the case of *M*, because transfer robot moves by order of each process, considers wafer of *Nth* of transfer time until process is completed and process waiting time.

If express this M × N to 2 dimensions determinant, W_{ij} can be expressed with Table IV.

If express Table IV. that is consisted of M × N relationship matrix by Hopfield neural networks energy function E, that is same with (4).

	1	2	3	4	5	…	N
Step1							
Step2							
Step3				①			
Step4							
Step5							
…							
Step N							

Table IV. Transfer Step of each *N* wafers
(The transfer route of *4th* wafer after Step 3 is shown as ①.)

$$E = \frac{A}{2}\sum_{i=1}^{N}\sum_{\substack{l=1\\ l\neq j}}^{N}\sum_{j=1}^{N} V_{ij}V_{il} + \frac{B}{2}\sum_{k=1}^{N}\sum_{\substack{i=1\\ i\neq k}}^{N}\sum_{j=1}^{N} V_{ij}V_{kj} + \frac{C}{2}\sum_{i=1}^{N}\left(\sum_{j=1}^{N} V_{ij} - N\right)^2 + \frac{D}{2}\sum_{\substack{i=1\\ i\neq k}}^{N}\sum_{\substack{j=1\\ j\neq l}}^{N}\sum_{k=1}^{N}\sum_{l=1}^{N} T_{il}\,V_{ij}\left((V_{il} - V_{kl}) + (V_{ij} - V_{kj})\right) \quad (4)$$

According to this equation, the resulting set of rules is as follows:

1st triple: Avert to depose other wafer's process in every same step.

2nd triple: Prevent that transfer robot to handle two steps at the same time.

3rd triple: Confirm transfer robot move following sets each all steps in process number of times.

4th triple: The meaning of the 4th triple is as follows.

1) The target function of the shortest waiting time

2) T: the transfer robot waiting time and movement time

3) The repeat of transfer robot

Also, A, B, C, D are constant.

Input U_{ij} of neuron and output V_{ij} that minimize energy function E of (4) are expressed with (5), (6)

$$\frac{dU_{ij}}{dt} = -\frac{\partial E}{\partial V_{ij}} = -\frac{A}{2}\sum_{\substack{j=1\\ j\neq i}}^{N} V_{il} - \frac{B}{2}\sum_{\substack{k=1\\ k\neq l}}^{N} V_{kj} - C\left(\sum_{k=1}^{N}\sum_{j=1}^{N} V_{ij} - N\right) - D\sum_{\substack{i=1\\ i\neq k}}^{N}\sum_{\substack{k=1\\ j\neq l}}^{N}\sum_{j=1}^{N}\sum_{l=1}^{N} T_{il}\left((V_{il} - V_{kl}) + (V_{ij} - V_{kj})\right) \quad (5)$$

$$V_{ij} = \frac{1}{2}\left(1 + \tanh\left(\frac{u_{ij}}{u_0}\right)\right) \quad (6)$$

Using Euler techniques[5] to solve differential equation (5), (6) at neural algorithm, is same with (7).

$$U_{ij}(t + \Delta t) = U_{ij}(t) + \Delta t\left\{-U_{ij}(t) - \frac{\partial E}{\partial V_{ij}}\right\} \quad (7)$$

Using (7) we can get U_{ij} which is substitute to (6) to get Vij. Therefore, the optimal path is found out.

IV. SIMULATION

Simulation order requires the step that follows:

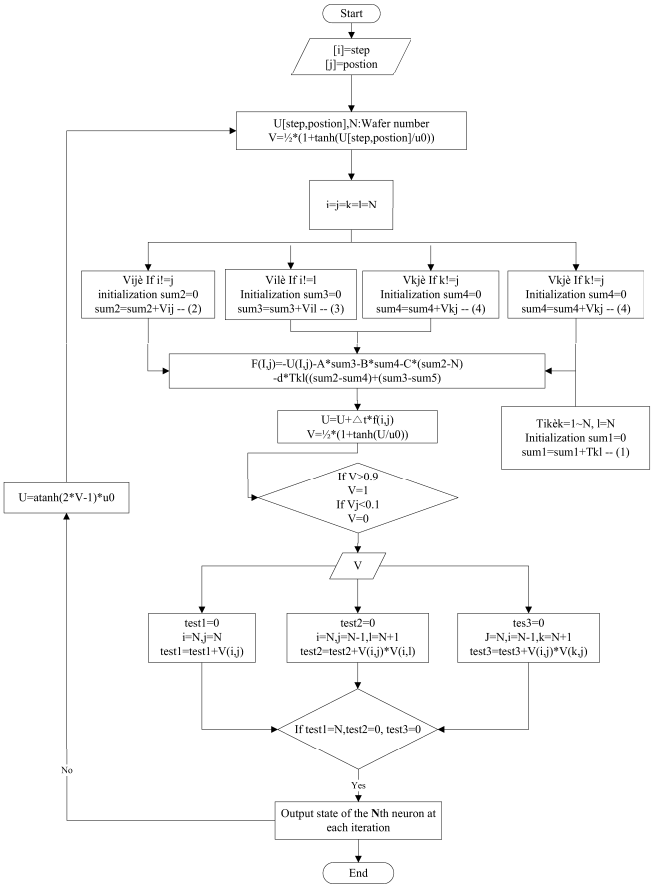

Fig. 5 Simulation Follow

If there is a set of wafer which are 10 wafers in total and the robot spend 3 sec to move to the first wafer and 0.5 sec between every slot as same as shown in Table II. We simulate the whole process using the optimal algorithm which sequence is gotten as Table V. The following figures from Fig. 6 to Fig. 15 demonstrate the output state of the neuron at each iteration. Comparing with the general shift method, we can see that the optimal scheduling method save 3 second using the data we have gotten. Table VI to VIII confirm the result.

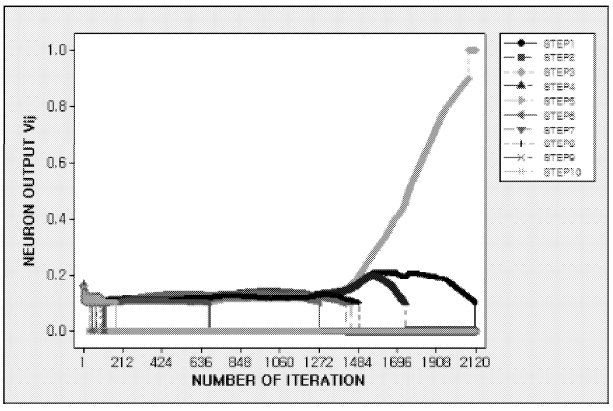

Fig. 6 Output state of the *1th* neuron at each iteration.

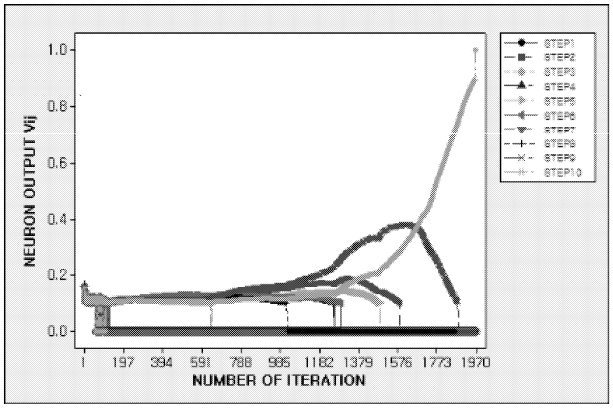

Fig. 7 Output state of the *2th* neuron at each iteration.

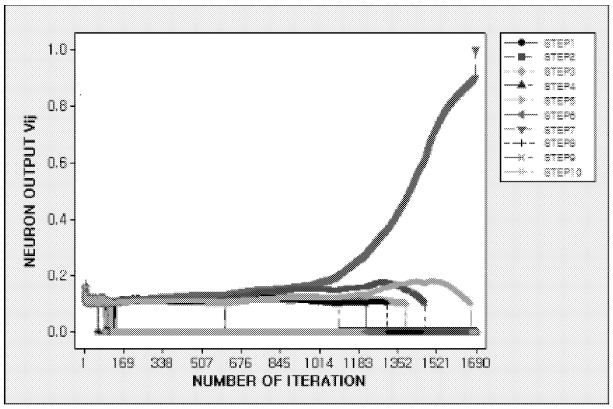

Fig. 8 Output state of the *3th* neuron at each iteration.

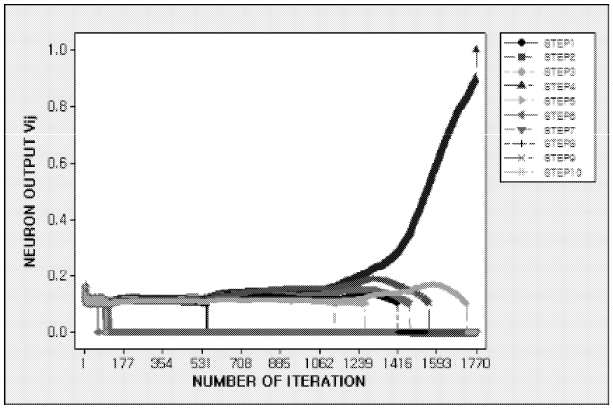

Fig. 9 Output state of the *4th* neuron at each iteration.

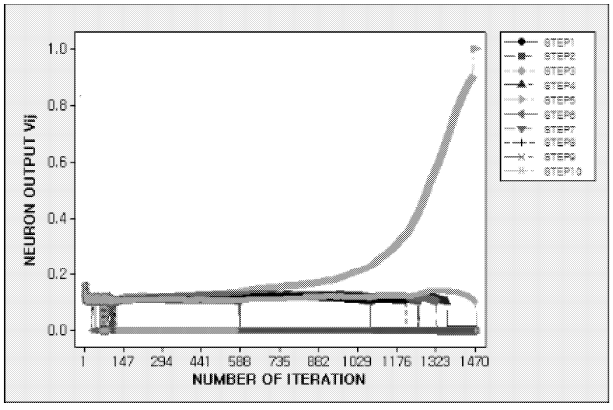

Fig 10. Output state of the *5th* neuron at each iteration.

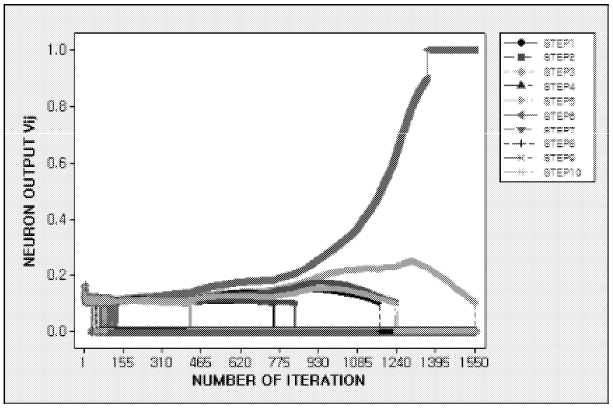

Fig. 11 Output state of the *6th* neuron at each iteration.

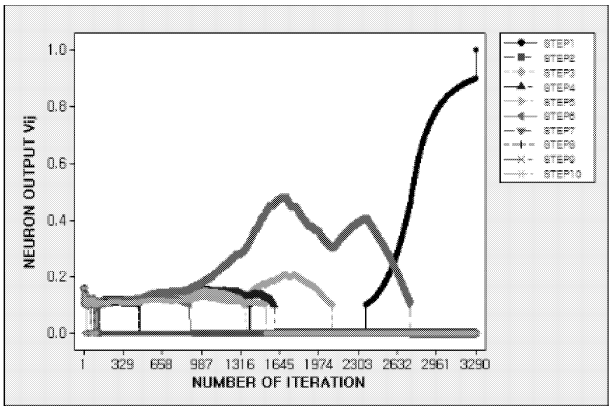

Fig. 12 Output state of the *7th* neuron at each iteration.

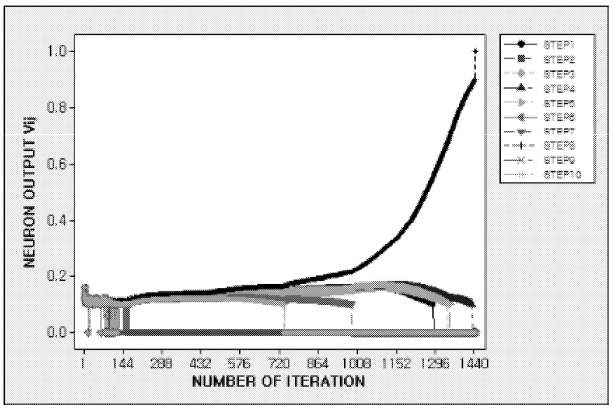

Fig. 13 Output state of the *8th* neuron at each iteration.

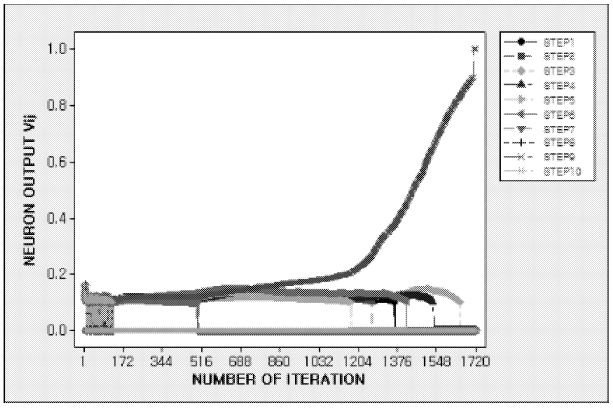

Fig. 14 Output state of the *9th* neuron at each iteration.

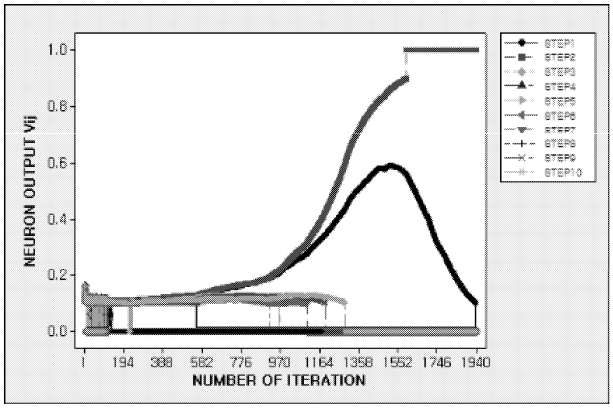

Fig. 15 Output state of the *10th* neuron at each iteration.

i \ j	1	2	3	4	5	6	7	8	9	10
step1	0	0	0	0	0	0	1	0	0	0
step2	0	0	0	0	0	0	0	0	0	1
step3	1	0	0	0	0	0	0	0	0	0
step4	0	0	0	1	0	0	0	0	0	0
step5	0	0	0	0	1	0	0	0	0	0
step6	0	0	0	0	0	1	0	0	0	0
step7	0	0	1	0	0	0	0	0	0	0
step8	0	0	0	0	0	0	0	1	0	0
step9	0	0	0	0	0	0	0	0	1	0
step10	0	1	0	0	0	0	0	0	0	0

Table V. Final output state of each neuron yielding minimum-time path and execution order of subtask.(*j*=position).
Wafer transfer path : 3-10-7-4-5-6-1-8-9-2

	55		55		55		90		55			
CS	AH도착	AH완료	CP도착	CP완료	SC도착	SC완료	HP도착	HP완료	CP도착	CP완료	CS	공정완료
3.0	3.0	58.0	58.0	113.0	113.0	168.0	168.0	258.0	258.0	313.0	3.0	316.0
3.5	61.5	116.5	116.5	171.5	171.5	226.5	258.0	348.0	348.0	403.0	3.5	406.5
4.0	120.5	175.5	175.5	230.5	258.0	313.0	348.0	438.0	438.0	493.0	4.0	497.0
4.5	180.0	235.0	258.0	313.0	348.0	403.0	438.0	528.0	528.0	583.0	4.5	587.5
5.0	263.0	318.0	348.0	403.0	438.0	493.0	528.0	618.0	618.0	673.0	5.0	679.0
5.5	353.5	408.5	438.0	493.0	528.0	583.0	618.0	708.0	708.0	763.0	5.5	769.5
6.0	444.0	499.0	528.0	583.0	618.0	673.0	708.0	798.0	798.0	853.0	6.0	859.0
6.5	534.5	589.5	618.0	673.0	708.0	763.0	798.0	888.0	888.0	943.0	6.5	949.5
7.0	625.0	680.0	708.0	763.0	798.0	853.0	888.0	978.0	978.0	1033.0	7.0	1040.0
7.5	715.5	770.5	798.0	853.0	888.0	943.0	978.0	1068.0	1068.0	1123.0	7.5	1130.5

Table VI. 10 wafers transfer order by empirical public decision is sequential case(1-2-3-4-5-6-7-8-9-10)
Last process completion time: 1130.5s

	55		55		55		90		55			
CS	AH도착	AH완료	CP도착	CP완료	SC도착	SC완료	HP도착	HP완료	CP도착	CP완료	CS	공정완료
6.0	6.0	61.0	61.0	116.0	116.0	171.0	171.0	261.0	261.0	316.0	6.0	322.0
6.5	67.5	122.5	122.5	177.5	177.5	232.5	261.0	351.0	351.0	406.0	6.5	412.5
7.0	129.5	184.5	184.5	239.5	261.0	316.0	351.0	441.0	441.0	496.0	7.0	503.0
7.5	192.0	247.0	261.0	316.0	351.0	406.0	441.0	531.0	531.0	586.0	7.5	593.5
3.0	264.0	319.0	351.0	406.0	441.0	496.0	531.0	621.0	621.0	676.0	3.0	679.0
3.5	354.5	409.5	441.0	496.0	531.0	586.0	621.0	711.0	711.0	766.0	3.5	769.5
4.0	445.0	500.0	531.0	586.0	621.0	676.0	711.0	801.0	801.0	856.0	4.0	860.0
4.5	535.5	590.5	621.0	676.0	711.0	766.0	801.0	891.0	891.0	946.0	4.5	950.5
5.0	626.0	681.0	711.0	766.0	801.0	856.0	891.0	981.0	981.0	1036.0	5.0	1041.0
5.5	716.5	771.5	801.0	856.0	891.0	946.0	981.0	1071.0	1071.0	1126.0	5.5	1131.5

Table VII. 10 wafers transfer order by empirical public decision is at random case (7-8-9-10-1-2-3-4-5-6)
Last process completion time: 1131.5s

	55		55		55		90		55			
CS	AH도착	AH완료	CP도착	CP완료	SC도착	SC완료	HP도착	HP완료	CP도착	CP완료	CS	공정완료
4.0	4.0	59.0	59.0	114.0	114.0	169.0	169.0	259.0	259.0	314.0	4.0	318.0
7.5	66.5	121.5	121.5	176.5	176.5	231.5	259.0	349.0	349.0	404.0	7.5	411.5
6.0	127.5	182.5	182.5	237.5	259.0	314.0	349.0	439.0	439.0	494.0	6.0	500.0
4.5	187.0	242.0	259.0	314.0	349.0	404.0	439.0	529.0	529.0	584.0	4.5	588.5
5.0	264.0	319.0	349.0	404.0	439.0	494.0	529.0	619.0	619.0	674.0	5.0	679.0
5.5	354.5	409.5	439.0	494.0	529.0	584.0	619.0	709.0	709.0	764.0	5.5	769.5
3.0	442.0	497.0	529.0	584.0	619.0	674.0	709.0	799.0	799.0	854.0	3.0	857.0
6.5	535.5	590.5	619.0	674.0	709.0	764.0	799.0	889.0	889.0	944.0	6.5	950.5
7.0	626.0	681.0	709.0	764.0	799.0	854.0	889.0	979.0	979.0	1034.0	7.0	1041.0
3.5	712.5	767.5	799.0	854.0	889.0	944.0	979.0	1069.0	1069.0	1124.0	3.5	1127.5

Table VIII. 10 wafers transfer order by empirical public decision is optimal path case(3-10-7-4-5-6-1-8-9-2)
Last process completion time: 1127.5s

Comparing with general shift method, for 10 wafers set the optimal scheduling method save 3 second and for 25 wafers set 11 seconds are saved.

Photo process of semi-conductor process repeats process in tens to hundreds seconds to form very integrated pattern on wafers. Among this, reduced only several seconds at PR process, but we can reduce end time from tens to hundreds seconds if quantity of wafers and repeated process are increased.

V. CONCLUSION

In this paper, we propose optimized scheduling of Multi-spinner equipment in Photo process that do the most repeat in process of semi-conductor manufacturing process and using unit of Hopfield neural networks to solve scheduling problem.

Existent sequential shift method does not consider distance of wafer in CS and process waiting time. While, did shortening of last process time considering process time and distance of wafer, and achievement path can solve the problem easily as by decrease of the is easy by decrease of the calculation amount if use neural networks that suggested in this paper that see because increase explosively according as number of wafer increases in case calculate by existing calculation method.

Efficiency of this paper proved through computer simulation and it may helps greatly increasing semi-conductor product when input in actuality process.

Considered wafer and AH process, last CP2 process interval and latency time that is filled to CS in this treatise, but research is thought that can shorten manufacturing process time still more if can consider transfer time by each process, and increase number of HP process that process difference becomes much also and increase number of transfer robot hereafter.

ACKNOWLEDGMENT

This research was financially supported by the Ministry of Education, Science Technology (MEST) and Korea Industrial Technology Foundation (KOTEF) through the Human Resource Training Project for Regional Innovation.

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