Hardware Implementation of a Phase-Locked Loop for Communication Systems

K. Kalita, J. Handique and T. Bezboruah, IAENG Member

Abstract **- We have implemented the hardware of a prototype Phase-Locked Loop (PLL) system in Instrumentaion and Informatics Research Laboratory, Department of Electronics Science, Gauhati University, Assam, India for communication systems. The system is tested using Digital Storage Oscilloscope (DSO) (Model: Tektronix TDS 1012B; 1GS/Sec). We also simulate the system using Circuit Maker's Berkeley SPICE3f5/XSpice-based simulator. In this paper we are presenting the result of our experimental test of the system and compared it with the simulated output.**

I. INTRODUCTION

Phase Locked Loops (PLL) has been one of the basic building blocks in modern electronic system. A PLL is a feedback control system in which the feedback signal is used to lock the output frequency and phase corresponding to the frequency and phase of the input signal. It was conceived by H. De Bellescize in 1932 [1, 2]. Ideally, there should be zero difference in phase and frequency between the controlled oscillator output and reference output at the steady-state condition. The basic form of PLL consists of a Voltage Controlled Oscillator (VCO), Phase Detector (PD), Loop Filter (LF) and a Frequency Divider (FD) network.

The phase locked loop has been found to be a useful element in many types of communication systems. They are at the heart of the circuits and systems ranging from clock recovery blocks in data communications to the local oscillators that powered the ubiquitous cellular phones. It also plays important roles in many applications ranging from frequency synthesis to clock recovery in wireless receivers. They are employed in a wide variety of communication circuits including frequency synthesizers, modulators and demodulators, motor speed control, signal detection etc[3, 4]. A PLL may be an analog or a digital. But most of them composed of both analog and digital components.

PLL is essentially a control system that employs feedback to maintain the phase of output signal in step with the phase of a reference signal. When the PLL is in lock, there will be a small phase difference between the two input signals of the phase detector. This phase difference results in a dc voltage at the detector output which is required to shift the VCO from its free-running frequency and keep the loop in lock.

A PLL has several states of operation. Initially the loop begins in the unlocked state, which occurs at the moment, when power is applied to it. After the transition period, a locked state arrives, in which the frequency of VCO equals the average frequency of the input signal, and each input cycle has only one cycle of VCO output. The transition from the unlocked to the locked state defines the acquisition response for the PLL [5, 6].

The PLL is a highly non-linear system, because the phase detector is non-linear [1, 2]. The lack of a non-linear theory was not a serious problem because most of the PLL applications were related to high frequencies and small variation about them. Therefore, the needs of engineering practice were satisfied by the conventional linear theory (small signal analysis) and interest for the development of a non-linear theory has been limited. In addition, the PLL has long simulation times because the high frequency VCO clock of 1GHz requires small time steps and low reference frequency of 1 MHz requires hundreds of microseconds for simulation to settle down. Because of these simulation problems, there is not even close to 100% coverage of PLL performance. One simulation tool can not measure all the characteristics and design requirements of the PLL. Multiple methodologies and developing one's own simulation tools added to the difficulty. Laboratory measurements require specialized equipment and measurements that have state of the art accuracy.

II. MOTIVATION OF THE WORK

High speed data communication over both wired and wireless media has become a major area of innovation and research. Increased bandwidth demand has been caused by the rapid growth of the internet and widespread use of cellular phones. To deliver this bandwidth, new technology has been developed to compress the data, to place the data on the physical medium at higher frequencies, and to receive the signal accurately. Among the requirements for digital transmission of data is the need to clock both transmitted and received data. A dedicated clock signal is usually not transmitted with the data, since that would require extra bandwidth for a signal that carries no actual information. Thus, clock must be reliably generated on both ends of the channel. PLL is the principal method of clock generation. It

K. Kalita is with the Department of Electronic Science, Gauhati University, Guwahati-781014, Assam, INDIA (e-mail: kalita.kakali@gmail.com)

J. Handique is with the Department of Electronics, Digboi College, Digboi - 786171, Assam, INDIA. He is presently with the Department of Electronics, Gauhati University, Guwahati-781014, Assam, INDIA(e-mail: jhandique@yahoo.com)

T. Bezboruah with the Department of Electronics Science, Gauhati University, Guwahati-781014, Assam, INDIA (E-mail: zbt_gu@yahoo.co.in, Tel: +91-361-2671262, Fax: +91-361-2700311)

has the ability to generate high frequency clock signals from lower frequency ones, as well as the ability to generate a clock directly from the received data. As such we have implemented the hardware and simulate the PLL in our Laboratory in an attempt to study the various characteristics of the system and to add innovative idea to it.

III. EXPERIMENTAL ARRANGEMENT

The basic hardware circuit of the PLL is shown in fig.1. The printed circuit board (PCB) for the same is shown in fig.2. Fig.3 shows the complete experimental arrangement for our present prototype system. The PD generates an output signal that is function of the difference between the phases of two input signals. The detector output is filtered, amplified and is applied to the VCO. The signal is fed back to the PD is the VCO output frequency divided by 2. The VCO output forces it to change the frequency in the direction that reduces the difference between the input frequency and the

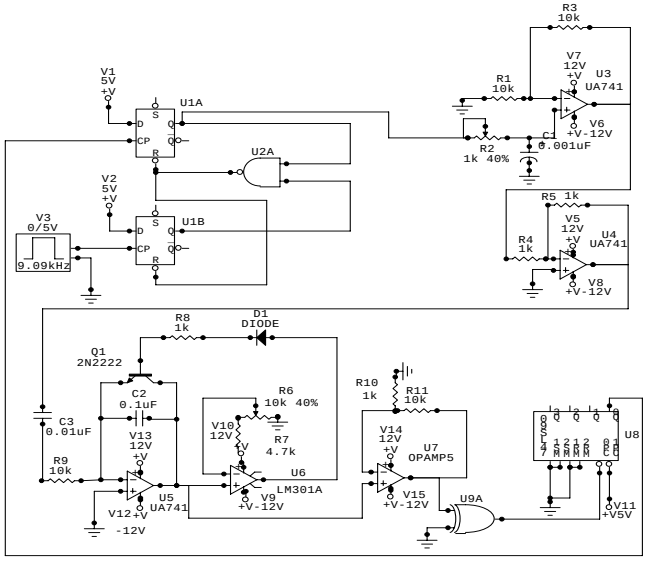

Figure 1: Circuit Diagram of Phase Locked Loop

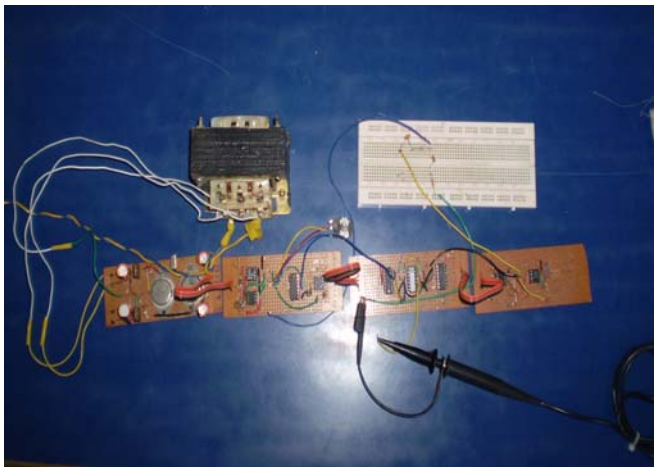

Figure 2: The printed circuit board of Phase Locked Loop

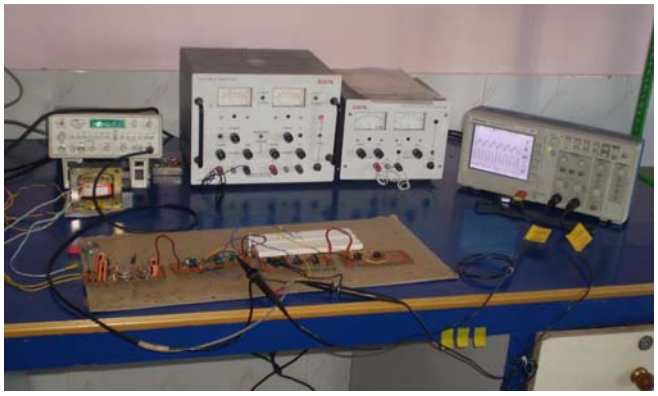

Figure 3: Basic arrangement of Phase Locked Loop

divider output frequency. If the two frequencies are sufficiently close, the feedback mechanism forces the two phase detector frequencies to be equal, and the VCO is locked with the incoming phase and frequency.

The hardware implementation of the system has been done by using the commercially available Integrated Circuits (ICs) in combination with the discrete components. We have designed and tested (i) the VCO (ii) the charge pump (amplifier) [7] (iii) the low pass filter (iv) the comparator (v) the frequency divider and (vi) the phase detector unit separately. Then we cascaded all the blocks together to design the complete circuit block of the PLL.

A. The Phase Frequency detector

The Phase frequency detector (PFD) is a circuit that produces an output signal that is proportional to the phase difference between two input signals. It compares the input frequency and VCO frequency that is processed by a LF to produce a dc voltage for controlling the oscillator for minimum phase error. The performance of the PLL characteristics varies depending on the type of PFD used. The PFD unit consists of dual D flip-flop (IC74LS74). It is often used because it is implemented with inexpensive digital logic and it inherently incorporates frequency steering when the PLL is out of lock.

B. Loop Filter

The LF used in our present PLL is a low pass filter (LPF) of first order. The LPF is utilized to remove the unwanted high frequency components which might pass out of the PD and appear in the VCO tune line, as they would appear on the output of VCO as spurious signals. It is used to tailor the PLL response in order to optimize the bandwidth, switching speed, settling time, spurious levels or other design parameters. The LF also governs the stability of the loop. The high cutoff frequency of the LF section is given by:

$$f_H = \frac{1}{2\pi RC}$$

C. Charge Pump

The charge pump is designed by using IC741 and along with passive components. In non inverting configuration the gain of the amplifier is given by

$$A_F = 1 + \left(\frac{R_f}{R_1} \right)$$

The theoretical gain of the charge pump for our present system is fixed at 2.

D. VCO

The VCO is one of the most crucial components in PLL design. Most of the major output characteristics are determined by the VCO. For instance, the sensitivity of the PLL to inject noise on the supply, the time jitter of the output, the phase noise, the frequency tuning range width, nonharmonically related spurious modes, loop stability, linear modulation and demodulation, and output that toggles in unlocked conditions, all depend on the characteristics of the VCO. For the present PLL system we have designed the VCO using IC741, differential amplifier LM301, and transistor 2N2222 and along with necessary passive components [8].

E. Frequency Divider

The PFD input reference clock frequency (F_{REF}) is equal to the input clock (F_{IN}) divided by the pre-scale counter (N=2). Therefore, the feedback clock (F_{FB}) applied to one input of the PFD is locked to the F_{REF} that is applied to the other input of the PFD. The VCO output feeds post-scale counters which allow a number of harmonically related frequencies to be produced within the PLL. We have designed frequency divider using BCD counter IC7490.

V. RESULT AND DISCUSSION

Fig.4 shows the output of the various stages, measured with DSO **(Model: Tektronix TDS 1012B; 1GS/Sec)** of the PLL system which we have developed in our Laboratory. Fig. 4(a) shows the Exclusive OR output whose frequency is 28.1380 KHz. This frequency is divided by two using frequency divider. The signal frequency at the output of the divider is 14.0560 KHz as shown in fig.4 (b). Fig.4 (c) shows PFD output for the present model. The maximum voltage recorded is 4.36V and the frequency of the output signal is 10.42 KHz compared to simulated value of 10.22 KHz [9]. The CH2 output in fig. 4(d) is the output of the VCO, when the reference input is triggered by a variable DC voltage source. The CH1 output is the output of the VCO under the same condition. Fig.4 (e) shows the final output for the system when the reference voltage is replaced by the signal from the receiver.

The various blocks which have developed generate the proposed model of PLL. PLL can be modeled accurately as a linear device when the phase difference between the phase detector input signals is small. Its performance characteristics vary depending upon the type of phase detector used. To overcome the limitation of substantial filtering of output and slow loop response of Exclusive–OR and flip-flop phase detector, we have designed phase frequency detector using Flip-Flop (IC7474) and NAND gate (IC7400)

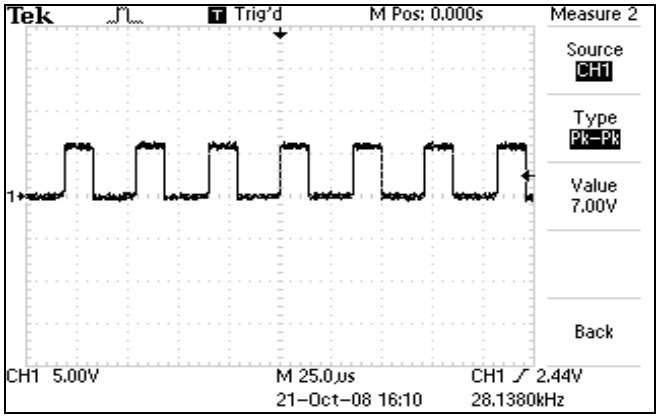

Figure (a): Exclusive OR output

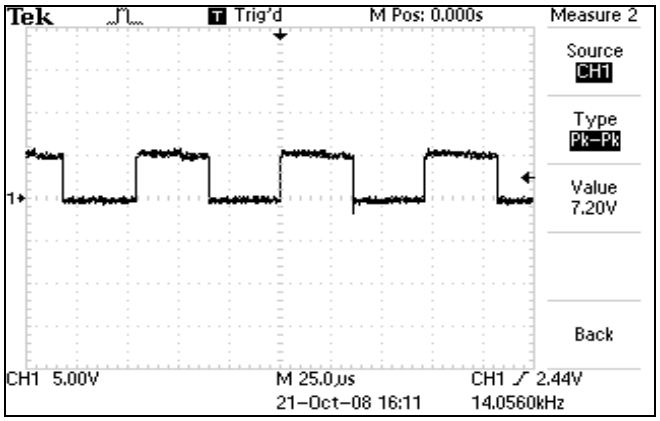

Figure (b): Frequency Divider output (Divide by 2)

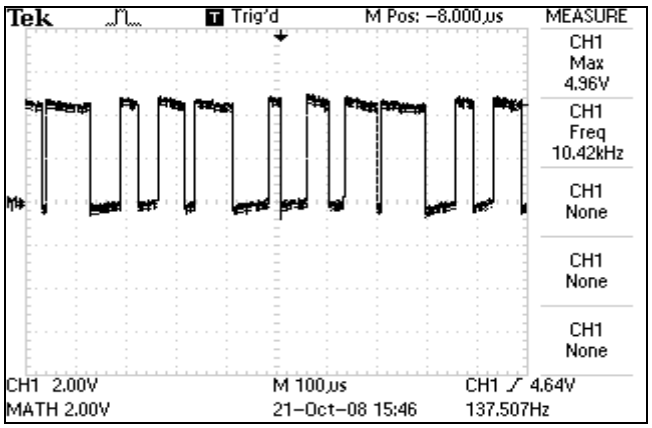

Figure (c): Phase Frequency Detector output

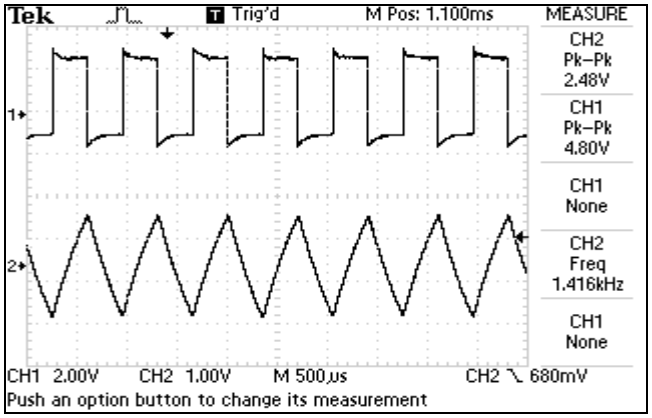

Figure (d): CH1 EX-Or output when dc voltage is applied to the reference, CH2 VCO output

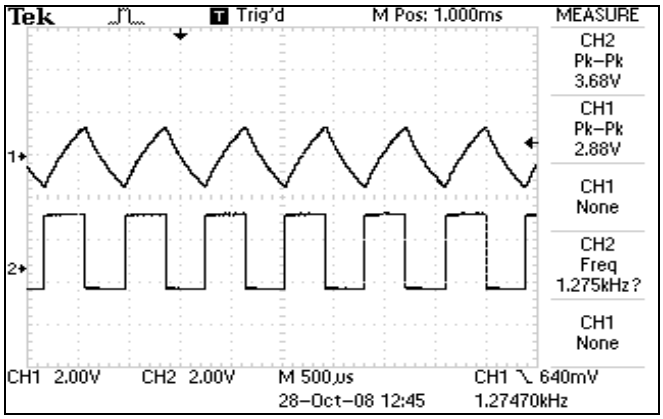

Figure (e): CH1 Final VCO output, CH2 Reference input

Figure 4: Output of different blocks of the PLL system developed in our laboratory measured by DSO (Model: Tektronix TDS 1012B; 1GS/Sec)

VI. CONCLUSION

In this paper we have presented the prototype of PLL that we have developed in our laboratory. The system is also simulated using Circuit Maker's Berkeley SPICE3f5/XSpice-based simulator. The simulation results have been presented elsewhere [9]. The system level simulation shows that the designed hardware output response matched with the simulation output response. As a future work, the dynamic behavior and noise performance of our prototype system will be evaluated by simulating the system on a mixed MATLAB™ and CMEX ™ Platform [10].

ACKNOWLEDGEMENT

The authors would like to thanks **University Grant Commission, Government of India** for partial financial support towards the work. They are also grateful to the **Head of the Department of Electronics Science, Gauhati University** for providing infrastructural support for implementation of the present work.

REFERENCES

[1] Nikolaos I. Margaris "Theory of the Non-linear Analog Phase Locked Loop", Springer Verlag, 2004
[2] A.R.Ball "Simulation of acquisition in PLL using Phase Frequency Detector" IEEE 1997.
[3] W. Rhee and A. Ali, "An On-Chip Compensation Technique in Fractional-N Frequency Synthesis," Proceedings of the 1999 IEEE ISCAS, Vol. 3, pp. 363-366, July 1999
[4] Y. Fan, "Modeling and Simulation of ∑Δ Frequency Synthesizers," Proc. Of the 2001 IEEE Symposium on Industrial Electronics, pp. 684-689, June 2001.
[5] Jack Smith, Modern Communication Circuits, Second Edition, Tata McGraw Hill, Edition, 2003.
[6] Stanley Goldman "PLL Engineering Handbook for Integrated Circuits".
[7] Pavan Kumar Hanumolu, Merrick Brownlee, Kartikeya Mayaram, Un-Ku Moon, IEEE Transactions on Circuit & Systems-I, Vol. 51, No. 9, Sept, 2004. "Analysis of Charge Pump Phase Locked Loops"
[8] Ramakanta A.Gayakwad "OP-AMP and Linear Integrated Circuit".
[9] K. Kalita and T. Bezboruah, "Modeling and simulation of Phased-locked loop for communication systems, Proceedings of the 33rd National Symposium on Instrumentation, Bisakhapatnam, INDIA, pp.133, December 2008.
[10] MEX-Files Guide, The Mathworks Inc., Natwick, Massachusetts, 2003.