A Novel Ultra-Low-Energy Bulk Dynamic Threshold Inverter Scheme

S.Soleimani, A.Sammak, B.Forouzandeh, *IAENG*

***Abstract*— In this paper we propose the use of a new DTMOS scheme in sub-threshold inverters. The results indicate that this scheme can provide better power efficiency than standard sub-threshold DTMOS inverters. Furthermore, we evaluate the stability of several sub-threshold DTMOS inverter schemes to temperature variation using deep-submicron CMOS technology.**

***Index Terms*— Subthreshold dynamic threshold voltage MOS (Sub-DTMOS), subthreshold logic, temperature variation, power and performance.**

I. Introduction

The increasing demand for portable applications has caused a significant growth of low-power design, from system level to device level [1]. Operating the transistors of a digital logic in the sub-threshold region has recently been proposed to achieve ultra-low power consumption [2]. However, the performance of the digital sub-threshold circuits is several orders of magnitude lower than their normal strong-inversion counterparts. One solution to this problem is a dynamic threshold operation which applies an active body-bias to MOSFETs [3]. Because of low threshold voltage during the logic transition and high threshold voltage during the off-state, the dynamic threshold circuit operates at high speed with low power [4]. Another important feature, which limits the robustness of the sub-threshold logic circuits using regular MOS transistors, is their extremely high sensitivity to the variation of temperature and process parameters. The exponential dependence of sub-threshold current on threshold voltage (Vth), which in turn depends on the temperature and process parameters, calls for additional stabilization scheme to ensure proper operation[5,6]. So it is important to study the stability of sub-threshold DT-MOS logics to temperature and Vth variations to compare their robustness over regular sub-threshold MOS circuits.

In this work we propose a new scheme of high speed, low power inverter using sub-threshold DTMOS transistors, and compare the power efficiency characteristics and temperature stability of proposed design to other schemes by SPICE simulation using the BSIM4 90nm process technology[7].

Manuscript received February 9, 2009.

S. Soleimani, A. Sammak, B. Forouzandeh are with Nano-Lab of ECE Department of Tehran University, Po. Box: 123456-1234 Tehran. Emails: (ssoleimani,ah.sammak)@ece.ac.ir and bforooz@ut.ac.ir

This paper is organized as follows: section II reviews different styles of DTMOS introduced in [8]-[10] and then uses them in sub-threshold inverter chains and discusses their merits and demerits. In section III, we propose a new scheme of high speed, low power inverter chain using sub-threshold DTMOS transistors. Then the characteristics of proposed scheme are evaluated and compared with other schemes previously reported. Section IV compares the temperature variation stability of various sub-threshold DTMOS inverter schemes with each other and with new scheme. Finally, the conclusions are provided in Section V.

II. Different Styles of DTMOS Transistors in Sub-threshold Logic Applications

In this section, some different styles of DTMOS transistors (Fig. 1) are used in sub-threshold inverters. Standard DTMOS logic uses transistors whose gates are tied to their substrates (Fig. 1.a) [8].However; in standard DTMOS topology the body-drain capacitor forms a Miller capacitance that may eliminate any gain from added current drive. The second style of DTMOS uses minimum-sized auxiliary devices to augment the current drive by manipulating the body bias (Fig. 1.b) [9]. In this style any excess current caused by forward biasing is used to charge/discharge the output. Fig 1.c shows another scheme of DTMOS which is similar to Fig 1.b but the gates of auxiliary devices are tied to main transistor's drain instead of gate [10].

The power-delay product (PDP) is a measure of the amount of energy/switching and can be used to determine whether the increase of power consumption is more dominant than the delay improvement, or vice-versa.

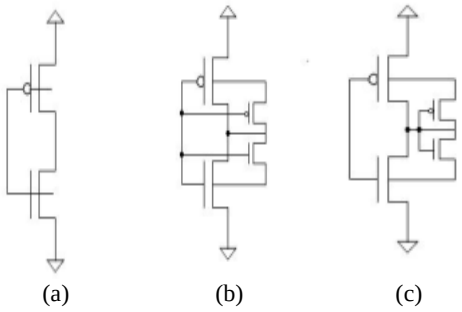

Fig. 1. Previously reported inverter designs (a) Standard DT-CMOS (b) DT-CMOS with augmenting devices (c) another topology of DT-CMOS with augmenting devices.

Figs. 2, 3 and 4, respectively, show the delay, power and PDP of 6 stage inverter chains as a function of Vdd for regular sub-threshold CMOS and three types of Sub-threshold DT-CMOS logics introduced in [8]-[10]. Results are obtained from SPICE simulations using BSIM4 90nm process technology at 25 ^{o}C[7]. Figs. 2, 3 and 4 indicate that the higher on-current of sub-DT-CMOS logics causes them to have higher power consumption, but they can switch much faster than regular sub-CMOS logics. Fig. 3 shows that, although sub-threshold DT-CMOS logics have higher power consumption, but the power consumption is still comparable with regular sub-threshold CMOS ,so Energy/switching becomes better than regular sub-CMOS and operating switching frequency can be higher. It can be understood from Fig. 4 that the best way to achieve maximum power efficiency in sub-threshold DT-CMOS logics is using the third topology shown in Fig. 1 [11].

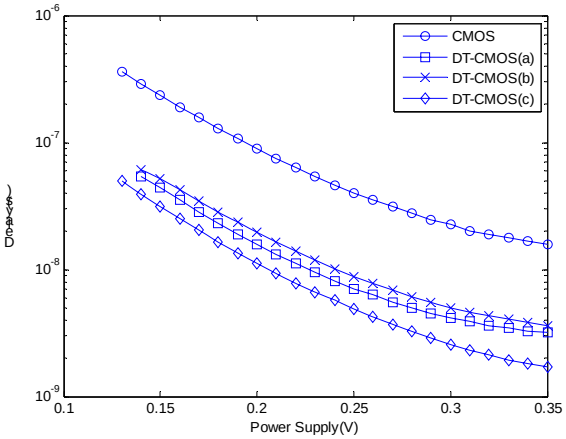

Fig. 2. Delay versus Vdd

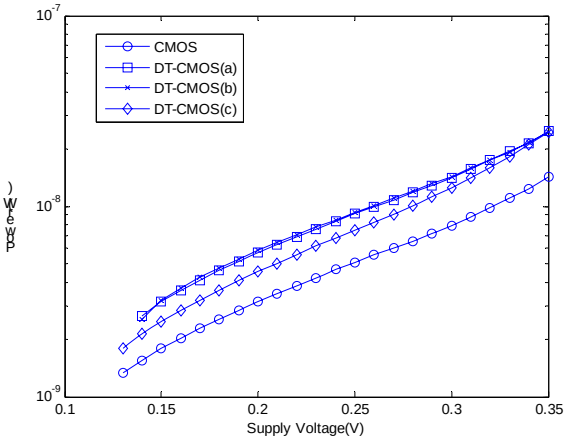

Fig. 3. Power versus Vdd

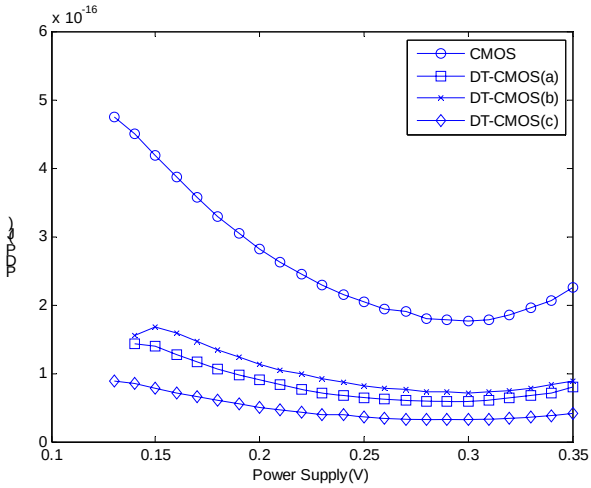

Fig. 4. Power-delay product versus Vdd

III. New Style of DTMOS Transistors in Sub-threshold Logic Applications

In this section we propose using a new style of DT-MOS transistors in sub-threshold logics. The proposed inverter circuit is shown in Fig. 5. As it can be seen in this inverter, drains are tied to substrates. Where the n-transistor body is low, causing a weak transistor trying to pull down the output against a strong p-transistor. Using this style of DT-MOS in sub-threshold logics, favorable conditions can be obtained to maximize gain and minimize leakage currents in the transistors [10]. The standard DT-CMOS (Fig. 1.a) only while the transistor is driving the output and proposed DT-CMOS at all other times can minimize leakage. For the DC analysis, the voltage transfer characteristic (VTC) of standard DT-CMOS inverter(Fig. 1.a) and proposed DT-CMOS inverter at the supply voltage of 0.2volt are simulated and shown in Fig. 6.The VTC of new design shows acceptable noise margin and gain. Plots for delay, power and PDP versus supply voltage are shown in Figs. 7, 8 and 9.

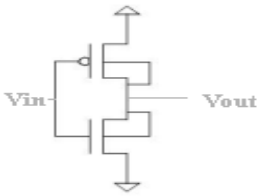

Fig. 5. The proposed circuit scheme

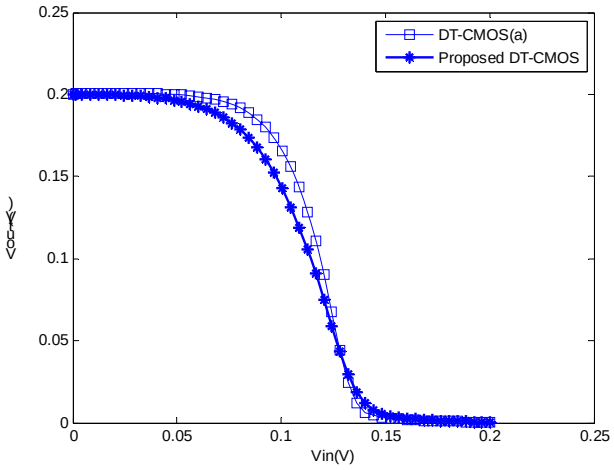

Fig. 6. VTC of standard and proposed DT-CMOS inverters

Fig. 7 shows that the delay of proposed scheme in sub-threshold applications is less than other DT-CMOS schemes. This is because in this scheme, during the transition (e.g. high to low) the strong n-transistor starts to pull down the output while simultaneously it becomes weak, so the output achieves enough voltage to switch next inverter faster compared to the other sub-DT-CMOS inverter chains. Power is much more saved in proposed DT-CMOS inverter chain (Fig. 8). So the new design is more power efficient in sub-threshold applications as shown in Fig. 9.

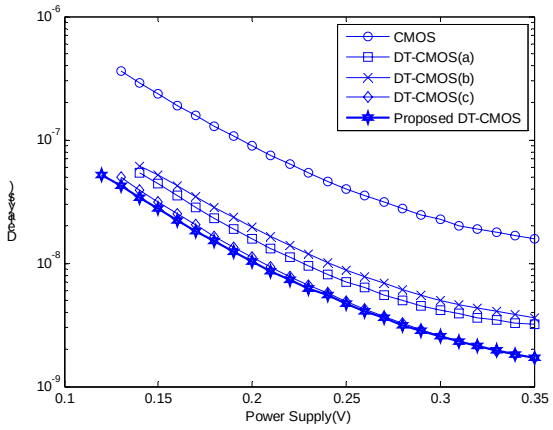

Fig. 7. Delay versus Vdd

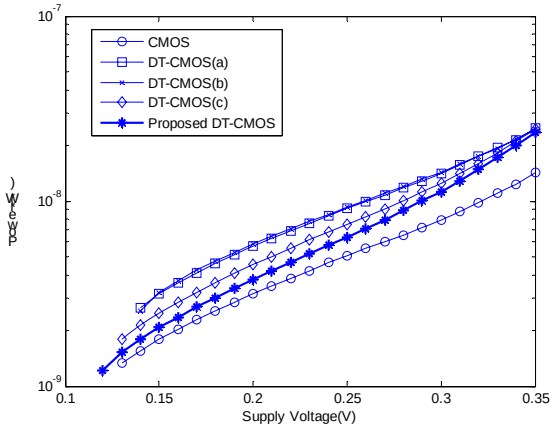

Fig. 8.Power versus Vdd

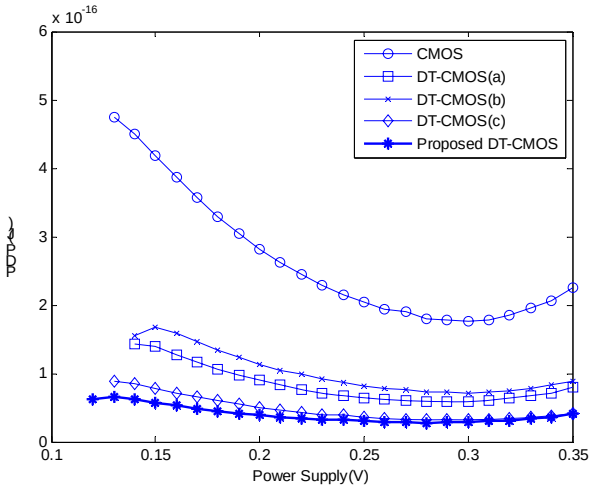

Fig. 9. Power-delay product versus Vdd

IV. Temperature Variations

In this section the stability of sub-threshold DT-CMOS logics to temperature variation is investigated. We analyze the effects of temperature on power and delay of both previously reported and the proposed scheme of sub-DT-CMOS inverter chains. The effect of temperature variation is analyzed using SPICE simulation with Vdd=0.2 V and the temperature parameter is being swept from room temperature (25^{o}C) to 125^{o}C. The effects of temperature variation are given in Table I. For a temperature change from 25^{o}C to 125^{o}C, the delay of proposed design changes by 64.55%. Standard sub-threshold DT-CMOS shows a change of 62.12% in its delay, so applying the new design to sub-threshold logics does not degrade the stability of circuit to temperature variation significantly.

TABLE I
EFFECTS OF TEMPERATURE

Temp=25 ^{o}C	Power(nW)	Delay(s)	PDP(J)
Sub-CMOS	3.145	8.94e^{-8}	2.8e^{-16}
Sub-DT-CMOS(a)	5.699	1.577e^{-8}	8.99e^{-17}
Sub-DT-CMOS(b)	5.836	1.948e^{-8}	1.137e^{-16}
Sub-DT-CMOS(c)	4.53	1.113e^{-8}	5.041e^{-17}
Proposed CMOS	3.784	1.031e^{-8}	3.902e^{-17}
Temp=125 ^{o}C	Power(nW)	Delay(s)	PDP(J)
Sub-CMOS	10.61	2.924e^{-8}	3.102e^{-16}
Sub-DT-CMOS(a)	13.78	5.973e^{-9}	8.232e^{-17}
Sub-DT-CMOS(b)	15.83	6.603e^{-9}	1.045e^{-16}
Sub-DT-CMOS(c)	16.85	4.067e^{-9}	6.851e^{-17}
Proposed CMOS	15.22	3.655e^{-9}	5.561e^{-17}

The effects of temperature variation on the performance and energy/switching for three previous types of sub-DT-CMOS Inverter chains are simulated and compared to that of proposed sub-DT-CMOS in Figs. 10 and 11.

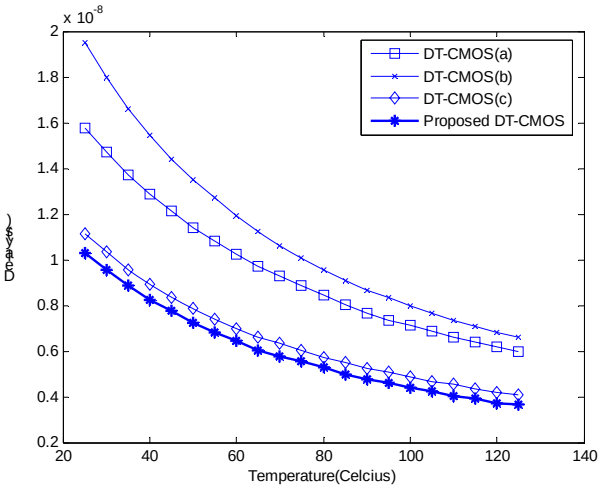

Fig. 10. Delay versus Temperature

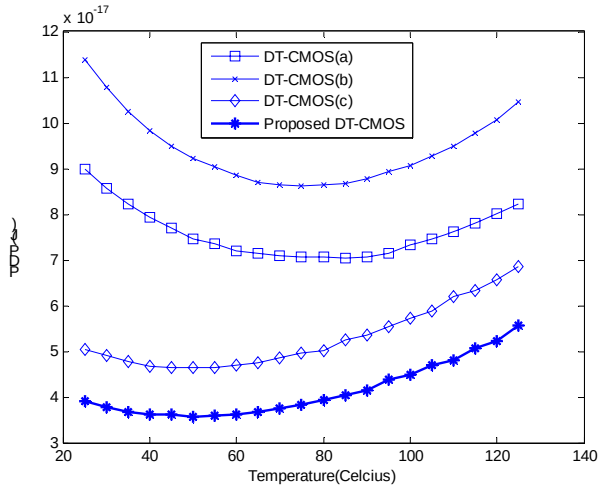

Fig. 11. Power-delay product versus Temperature

V. Conclusion

We have proposed a new scheme of DT-CMOS for sub-threshold logic applications. The power, delay and PDP of the new scheme were evaluated by SPICE simulations. The proposed scheme shows improved power efficiency for sub-threshold applications. The delay variation of the proposed scheme with temperature was also investigated. Although the stability of proposed design to temperature variation was not as well as standard sub-threshold DT-CMOS, but in general the design shows good characteristics in ultra-low power and high speed applications.

References

[1] H. Soeleman, K. Roy, B. Paul, "Robust ultra-low power sub-threshold DTMOS logic," in *Int. Symp. Low Power Electron. Design*, 2000 ,pp.25 – 30.

[2]H. Soeleman and K. Roy, "Ultra-low power digital subthreshold logic circuits," in *Int. Symp. Low Power Electron. Design*, 1999, pp. 94–96.

[3] F. Assaderagi, et. al., " Dynamic Threshold Voltage MOSFET (DTMOS) for ultra-low voltage VLSI," IEEE *Trans. Electron Devices*, vol. *44*, no. 3, pp. 414- 422, Mar. 1997.

[4] J. Gil, M. Je, J. Lee and H. Shin, "A High Speed and Low Power SOI Inverter using Active Body-Bias," in *Int. Symp. Low Power Electron.Design* , 1998 , pp.59-63.

[5]T. Kobayashi and T. Sakurai, "Self-adjusting threshold-voltage scheme (SATS) for low-voltage high-speed operation," in Custom Integrated Circuits Conference, pp. 271-274, May 1994.

[6] T. Kuroda et. al., "A 0.9-V, 150-MHz, 10-mW, 4-mm2, 2-D discrete cosine transform core processor with variable threshold-voltage (VT) scheme," IEEE Journal of Solid-State Circuits, vol. 31, n. 11, pp. 1770-1779, November 1996.

[7] Predictive Technology Model (PTM), http://www.eas.asu.edu/~ptm/

[8] F. Assaderaghi, D. Sinitsky, S. Parke, J. Bokor, P. K. Ko, and C. Hu, "A dynamic threshold voltage MOSFET (DTMOS) for ultra-low voltage operation," in *IEDM Tech. Dig.*, 1994, pp. 809–812.

[9] I. Chung, Y. Park, and H. Min, "A new SOI inverter for low power applications," in *Proc. 1996 IEEE Int. SOI Conf.*, 1996, pp. 20–21.

[10]A. Drake, K. Nowka, R. Brown, " Evaluation of Dynamic-Threshold Logic for Low-Power VLSI Design in 0.13um PD-SOI," VLSI-SOC 2003,pp. 263-266.

[11] M.R. Casu, G. Masera, *G.* Piccinini, M. Ruo Roch, M. Zamboni ,"Comparative Analysis of PD-SOI Active Body-Biasing Circuits," *Proc. IEEE International SOI Conference*, pp. 94-95, Oct. 2000.