A 300 mA 0.18 μm CMOS Low-Dropout Regulator with High Power-Supply Rejection

Yali Shao*, Lenian He

Abstract— A CMOS high power supply rejection (PSR) low-dropout regulator (LDO) with a maximum output current of 300 mA is proposed. The existing architectures of high PSR LDO were classified and analyzed. And one overall design principle was illustrated，that is to obtain a constant gate-source-voltage V_{gs} of the main power transistor. A LDO based on this principle was designed with standard TSMC 0.18 μm CMOS process. The input voltage range is 2 V to 3.5 V with a minimum dropout voltage of 200 mV. Simulation results show that the PSR is better than -51.8 dB @ all frequency if the output current is 10 mA, and when fully loaded, the PSR is -59 dB @ 1 KHz. It is of high performance compared with the other works. The temperature characteristic of PSR is also concerned in this work.

***Index Terms*—PSR, LDO, 300 mA, constant gate-source -voltage.**

I. INTRODUCTION

With the prevalence of handsets, Low drop-out (LDO) linear regulators have become a key building block in portable communication systems, due to its accurate output voltage, low noise, low power consumption and fully CMOS integrated [1]-[3], especially the high power supply rejection (PSR) .

The output of LDO is often used as the power supply of cellular phones, MP3 players, personal digital assistances (PDA), and numeral cameras and so on. In these systems, a large load current is required. For example, in the mobile phone audio power supply system, a current of 300 mA or even larger is required, as well as the range of the audio frequency is usually 20Hz to 20KHz [4]. However, due to the feedback nature of the system, the LDO should be stable for a wide range of supply currents, but the PSR usually becomes bad with a large load current.

In recent years, many researches are focus on the PSR of LDO. However, these studies often concern about a small load current range. For example, the maximum load current is 10 mA in [5], which won the best paper prize of ISIC 2009 (International Symposium on Integrated Circuit). Reference [6] proposed on ISSCC 2009(International Solid-State Circuits Conference) is 25 mA. It is only 5 mA in [7], which is lamentably inadequate for a 300 mA application requirement. In [8], a maximum load current of 100 mA is presented, whereas the PSR of low frequency is not improved at all. To make matter worse, the power consumption increases rapidly with the growing of load current: it is 270 uA quiescent current when the output is 100 mA. Reference [9] also offers a 100 mA maximum load current. However, the input voltage is as high as 4.2 V and the minimum dropout voltage is 410 mV, which is not suitable for a low voltage application. The same defect remains in [10], whose dropout voltage is 541 mV, even though the maximum load current is 150 mA. Reference [11], using 0.13 μm state-of-art technology, also delivers a 150 mA output current, and the dropout voltage is as small as 200 mV, but the output voltage is 2.8 V, which maybe not appropriate for a low power supply demand.

The PSR of LDO also changes with temperature. As we know, Industrial temperature range is -40°C to +85°C. Therefore, the PSR should always keeps at a good level with different temperatures. There are few researches concerning about this.

Here, A LDO with the maximum load current as large as 300 mA is proposed. The output voltage is 1.8 V and the dropout voltage is only 200 mV. At the same time, it is of high PSR even at different temperatures with different load currents. In Sec. II, the existing architectures of high PSR LDO are presented, summarized and analyzed. By a thorough investigation, one overall design principle is illustrated. In Sec. III, a high PSR LDO circuit and the implementation details using a standard 0.18 μm CMOS process are discussed. The simulation results are provided in Sec. IV, and finally in Sec. V the conclusion is remarked.

II. EXISTING ARCHITECTURES OF HIGH PSR LDO

PSR of LDO represents the gain from power supply v_{dd} to the output v_{out},

$$PSR = \frac{v_{out}}{v_{dd}} \quad (1)$$

A. The existing architectures of high PSR LDO

There are mainly two ways to improve the PSR of LDO, reviewing of the existing researches. The first is isolating the source (or drain) voltage of the pass transistor from the power supply noise. In this method, always an additional power transistor is used. For instance, an NMOS transistor in cascode with the NMOS pass transistor is proposed in [12]. The bias for the cascading NMOS and the error amplifier of the core regulator is provided by a charge pump, which occupies a large silicon area. In [13], an NMOS in cascode with a PMOS pass transistor is presented. A different bias circuit with almost similar structure is adopted in [7]. Reference [5] proposes an LDR architecture that has a power path of cascoding an NMOS transistor with the PMOS pass transistor, but the gate bias of the NMOS is controlled by an auxiliary LDR together with a first-order low-pass filter (LPF).

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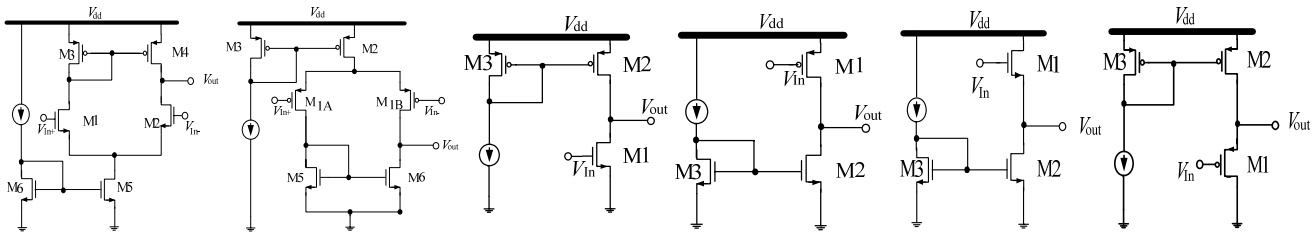

Fig. 1. Six kinds of basic amplifiers (a) NMOS differential input amplifier (N-DA); (b) PMOS differential input amplifier (P-DA) ; (c) NMOS input common source amplifier (N-CS) ; (d) PMOS input common source amplifier (P-CS); (e) NMOS input source follower (N-SF); (f) PMOS input source follower (P-SF).

Whatever the types of the power transistor cascoded, charge pump is always used. Then a clock is necessary along with RC filtering to remove the clock ripples, which leads to a higher complexity of the system, and the larger silicon area. What is worse, the drop-out voltage is usually high, even the best dropout voltage I have seen so far is 400 mV (in [5]), which is not suitable for low-voltage state-of-the-art technologies.

The second method is just employing one pass transistor, one of whose terminal is directly connected to the supply voltage V_{dd}, letting the gate of the power transistor, namely the output of the Error Amplifier (EA), change exactly the same with V_{dd}, as to achieving a high PSR. All the analysis of the monolithic, linear regulators for SoC applications in [3] is based on this hypothesis. It only concerns amplifiers of one stage, whereas amplifiers of two stages are more often used. Reference [6] also adopting this train of thought. A technique of feedforward ripple cancellation (FFRC) was proposed. The supply ripples, appearing at the source of pass transistor MP, are reproduced on the gate of MP through the feedforward path. However, the feedforward amplifier and the summing amplifier are required to have a wide bandwidth; which means a large bias current. Both the two amplifiers are designed to consume about 14 μA when a maximum load current is only 25 mA; if extending the load current to 300 mA, the quiescent dissipation is no less than 300 μA, which is not desirable for low power design art.

B. The essence of existing architectures--design principle

By a thorough investigation, the existing two architectures both base on one overall principle: that is to obtain a constant gate-source-voltage V_{gs} of the main pass transistor. The first way is employing pass transistor as a pre-regulator to achieve a ripple suppressed source (or drain) voltage of the main pass transistor, whose gate voltage is also made free of supply ripple; thus an invariable V_{gs} is got. The second method is exactly the opposite: just leaving the power supply ripple to one terminal of the pass transistor, all that is needed is a correlated ripple at the gate of the pass transistor, which, in nature, is also the same changeless V_{gs} of the main pass transistor.

Why high PSR means a constant V_{gs} of the main pass transistor？ Because an unchangeable gate-source-voltage means a change in V_{dd} does not result in a change in the output current. Thus, the output voltage of LDO is free of ripples.

The same quantized calculation can be found in [14]. The PSR of a closed-loop LDO, ignoring the noise of V_{ref}, could be described as:

$$PSR_{\text{loop}} = \frac{V_{\text{out}}}{v_{\text{dd}}} = \frac{A_{\text{ddEA}} A_{\text{power}} + A_{\text{ddpower}}}{1 + \beta A_{\text{EA}} A_{\text{power}}} \quad (2)$$

PSR_i and A_{ddi} both represent PSR of the ith stage, v_{ini}, v_{oi}, and A_i represent the input, output voltage and the small signal gain of the ith stage, respectively.

In most low voltage applications, in order to get a low dropout voltage and make the system not too complex, a PMOS pass transistor is much better than the NMOS one. Therefore the DC PSR of closed-loop LDO from (2) can then be described as:

$$PSR_{\text{loop}}(0) \approx -\left[\frac{1 - A_{\text{ddEA}}}{\beta A_{\text{EA}}} + \frac{g_{\text{o}}}{\beta A_{\text{EA}} g_{\text{m}}}\right] \quad (3)$$

g_m and g_o is the transconductance and source-drain admittance of the power transistor, respectively. So adjusting A_{ddEA} approach to 1 is the obvious way to get a high PSR of LDO, whereas A_{ddEA} approach to 1 is just the same meaning of a constant V_{gs} of the main pass transistor.

III. PROPOSED HIGH PSR LDO CIRCUIT

According to [14], we can see that, of the six basic amplifiers (Fig.1) and the eight combinations (Of the six basic structures, the first two kinds of differential amplifiers are used as the first stage of EA, and the rest as the second stage), the best one is the N-DA+P-CS structure.

Based on this configuration, we can get an even better high PSR LDO circuit with a little improvement according to (3). At the same time, the frequency compensation for stability of the circuit should be designed with caution, especially when a large load current as 300 mA is wanted.

The schematic of the circuit (not including the bias part) is shown in Fig.2, both considering the PSR and the stability.

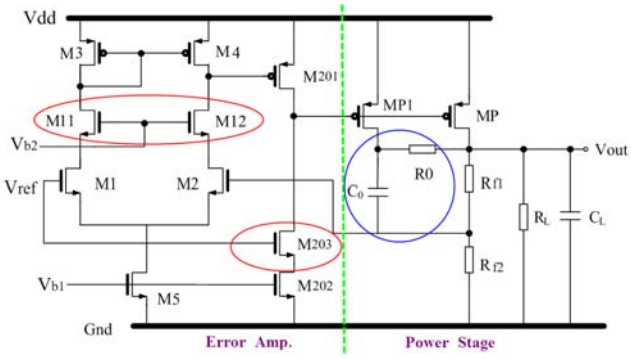

Fig.2. Schematic of the proposed high PSR LDO

The left side of the green dash line is the Error Amplifier. The circuits in red oval-shaped circle are the additional part compared with the N-DA+P-CS structure in [14]. M11, M12 and M203 all make the small signal resistances to the ground larger than those to the power supply V_{dd}, intuitively; the output of EA can then track V_{dd} better, which can also be

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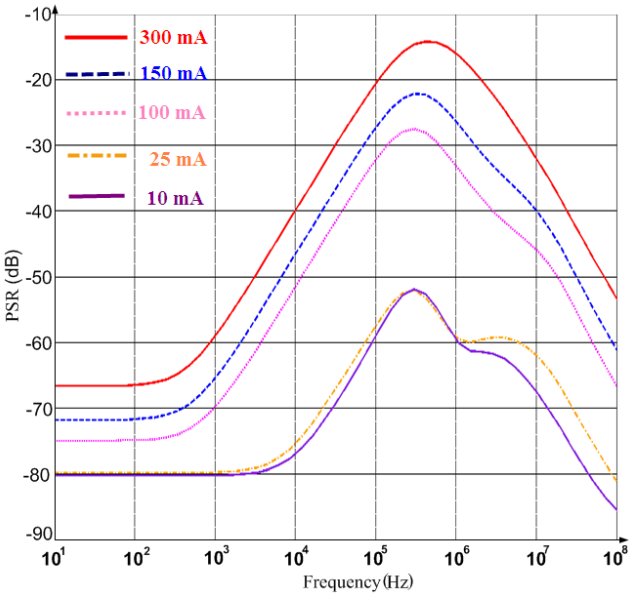

Fig.3. The PSR of LDO under different load currents at 27 °C temperature when input voltage V_{dd} is 2 V

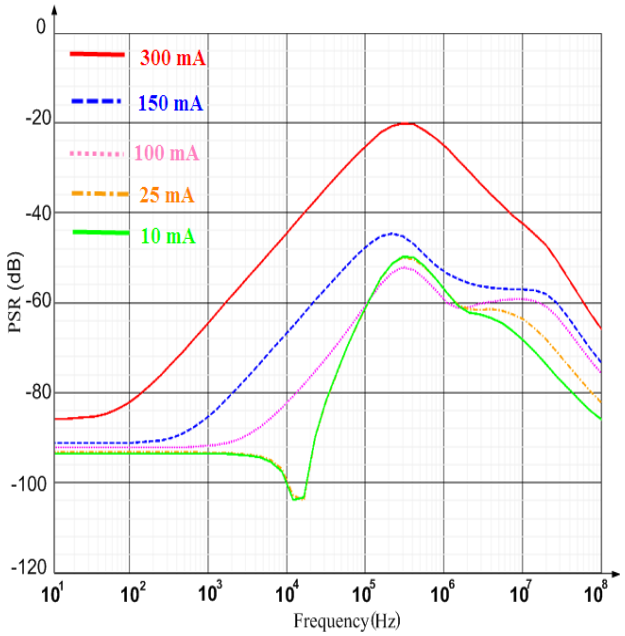

Fig.4. The PSR of LDO under different load currents at 27 °C temperature when input voltage V_{dd} is 2.2 V

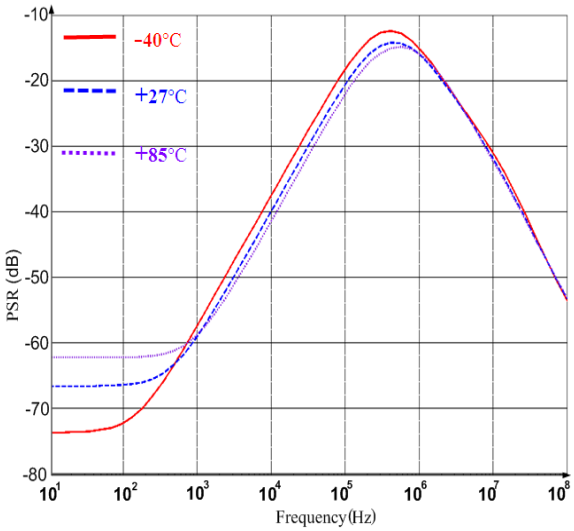

Fig.5. The PSR of LDO under different temperatures at 300 mA load current when input voltage V_{dd} is 2 V

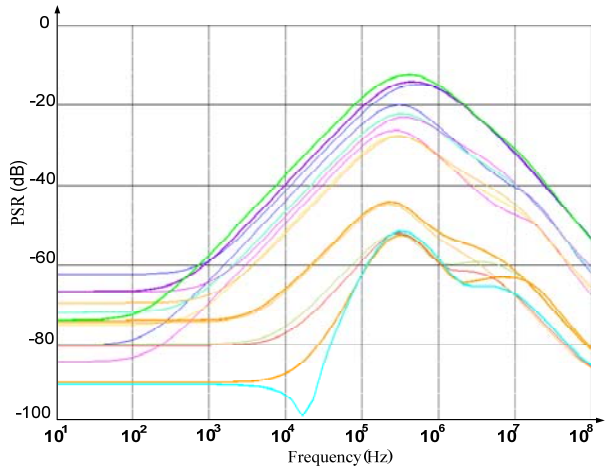

Fig.6. The PSR of LDO under different temperatures and different load currents when input voltage V_{dd} is 2 V

proved by careful calculation.

The right side of the green dash line is the Power Stage with the compensation network (R0 and C0, in blue round circle) and the feedback network (Rf1 and Rf2). MP1, of the same V_{gs} of the pass transistor MP, is a smaller current copy of the MP and a bias of the compensation network. The components of R0 and C0 provide a zero of the whole circuit, and the output pole of the first EA stage is much larger than the unit gain bandwidth (UGB) of the system. The external load capacitor CL is 1 μF to minish the output pole. Through carefully setting up the component parameters, the circuit can be stabile with a wide load current range as 5μA to 300 mA.

The bias part of LDO is the traditional self-bias circuit, which is not shown here. It has considered the influence of the temperature, so two different temperature coefficient resistances are employed together to get a parabolic temperature curve.

IV. SIMULATION RESULTS

The proposed LDO was designed with TSMC standard 0.18 μm CMOS process. The input voltage range is 2 V to 3.5 V with a precision 1.8 V output voltage. Therefore the dropout voltage is only 200 mV. The maximum output current is 300 mA. The reference voltage is 1.2 V from external.

The PSR curves of LDO shown in Fig.3 are simulated at 27 °C temperature when the input voltage V_{dd} is 2 V, under different load currents, which, from bottom to top, are 10 mA, 25 mA, 100 mA, 150mA and 300 mA, respectively.

From Fig.3 we can see that, the PSR of LDO becomes bad with the increase of the output current. It is a very natural process, and we can just get the same theory reasoning from (3):

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TABLE 1 PERFORMANCE SUMMARY AND COMPARISON

	Unit	[7]	[5]	[6]	[8]	[9]	[10]	This work
Paper	year	2007	2009	2009	2009	2009	2009	2010
Technology	μm	0.6	0.35	0.13	0.35	0.35	0.18	0.18
V_{dd}	V	> 1.8	> 1.6	> 1.15	1.2	4.2	2.04	2~3.5
V_{out}	V	1.2	1.2	1	1	3.3	1.5	1.8
Dropout Voltage	mV	600	400	150	200	410	541	200
Quiescent Current	μA	70	70	50	270	170	35	153
Max. Load Current	mA	**5**	**10**	**25**	**100**	**100**	**150**	**300**
PSR	dB	<-22.7 up to50 MHz	<-22.7 up to 60 MHz					<-51.8 @ all frequency @10mA
				-67@1MHz				-60@1MHz@25mA
				-56@10MHz				-62@10MHz@25mA
					-49.8@ 10KHz	-63 @ 1KHz	-64.3 @1KHz @50mA	-70@1KHz@100mA -51@10KHz@100mA
								-65 @1KHz @150mA
								-59 @1KHz @300mA
load regulation	mV /mA	N.A.	0.32	0.048	0.0012	N.A.	0.101	0.0009
△Vout /Vout	mV/ V	N.A.	0.25/1	26/1	0.027/1	50/3.3	——	0.000045/1.8

$$PSR_{loop}(0) \approx -\left[\frac{1-A_{ddEA}}{\beta A_{EA}} + \frac{\lambda_{power} I_{out}}{\beta A_{EA}\sqrt{2k_p' I_{out}\left(\frac{W}{L}\right)_{power}}}\right] \quad (4)$$

$$= -\left[\frac{1-A_{ddEA}}{\beta A_{EA}} + \frac{\lambda_{power}\sqrt{I_{out}}}{\beta A_{EA}\sqrt{2k_p'\left(\frac{W}{L}\right)_{power}}}\right]$$

In (4), the power transistor is supposed to work in the saturation region, which is often the case. So it is clear that the larger the I_{out} is, the worse the PSR will be.

Fig.4 is obtained almost the same as Fig.3 with only one difference: the input voltage V_{dd} is 2.2 V.

Comparing Fig.3 and Fig.4, about -10 dB better the PSR is when the input voltage increases 200 mV. Thus, it is obvious that the larger the input voltage is, the higher the PSR will be. So it is relatively easy for [5], [7], [9] and [10] to acquire a better PSR, whose dropout voltage is at least 400 mV.

Fig.5 is the PSR of LDO under different temperature at 300 mA load current when input voltage V_{dd} is 2 V. It shows that the PSR changes with temperature, but mainly in low frequency, and when the frequency is high, the impact is negligible, as long as the EA carefully designed works in normal area. That's the reason why there are so few papers concerning about the temperature influence over PSR.

Fig.6 illustrates the PSR of LDO under different temperatures and different load currents when the input voltage V_{dd} is 2 V, which ensures the continuity of PSR with the change of currents and temperatures.

Table 1 summarizes and compares the performance of the proposed LDO with other researches. The most remarkable characteristic of this work is the large output current, which meets the requirement of the mobile phone audio power supply system and something alike. Also the LDO is of high PSR quality, whatever the load current is, compared with other works. That is because the design principles are clearly summarized by a thorough investigation of the existing researches and a quantized analysis.

By the way, on account of the simple architecture of this work, the on-chip silicon area (without the pass transistor) is much smaller compared with the others.

V. CONCLUSION

A LDO with a 300 mA maximum load current is proposed. The output voltage is 1.8 V and the dropout voltage is 200 mV. Simulation results show that it is of high PSR performance. The PSR is better than -51.8 dB @ all frequency @10 mA, and is -70 dB @1 KHz @ 100 mA. When fully loaded, the PSR is -59 dB @1 KHz.

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