A 20μW 95dB DR Single-Bit Delta-Sigma Modulator for Portable Measurement Applications

Jian Xu, Hanqing Wang, Xiaobo Wu†

***Abstract*–A low power high performance Delta-Sigma modulator for portable measurement applications is presented in this paper. To reduce the power consumption and ensure high performance, a comprehensive system-level design adopting a new method to determine the DC gain value of Operational Transconductance Amplifier (OTA) and considering the effect of 1/f noise is introduced. Besides, a novel power efficient current mirror Class-AB OTA with a fast-settling less-error switched-capacitor common-mode feedback (SC CMFB) circuit is proposed in this design. And the bottom terminal parasitic-effect of Poly-Insulator-Poly (PIP) capacitors is also considered. Therefore, about extra 20% of the capacitance is added to the total capacitance load. In addition, an area-efficient power-efficient resonator is adopted to realize a coefficient of 1/90 for 50% power and 75% area cost reduction over the conventional design. The chip is implemented in a low cost standard 0.35μm CMOS. Its total power is only 20μW at a 1.5V supply, and the measured Dynamic Range (DR) is 95dB over the 1 kHz bandwidth. The designed modulator shows very high Figure-of-Merit (FOM) among the recent low power high performance modulators.**

***Keywords*–low power, high performance, Delta-Sigma modulator, switched capacitor circuits**

I. Introduction

Recently, portable electronic devices, such as portable measurement, implantable medical devices and digital cameras, were greatly demanded in the consumer market [1]. Low power is of great importance for these battery-powered devices to increase the battery lifetime. Hence, more power efficient circuits have been demanded than ever [2]. As an important building block, Delta-Sigma modulators are widely used in these portable devices. Therefore, the design of low power high performance modulators is essential to these devices.

The improvement of low power high performance modulators has been continuing to develop [1]-[8]. Utilization of an advanced CMOS process with a low threshold voltage is a common method, but its cost is high [1], [2]. Some works were implemented with a switched-opamp (SO) technique, which can reduce both the power and supply voltage [4], [5]. However, the power efficiency of the SOs used in these works is not high. Considering the OTA itself, a body-driven technique was also used to reduce both the supply voltage and power consumption [6]. The drawback is that the body-driven transistors have some limitations caused by bad noise performance [7]. To remove the need of OTAs, comparator-based and inverter-based SC circuits have been proposed in [3], [8]. Both two techniques have the ability to operate with low supply voltage and power consumption. However, it is difficult for these two techniques to realize a resolution up to 14-bit or more due to the residual offset and stringent conditions for the required operation region.

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To reduce the cost of chip fabrication, this paper focuses on the design in a low cost 0.35μm CMOS. Through the comprehensive system-level design and the use of novel power efficient OTA and resonator, the proposed modulator in this paper can also achieve low power and high performance without needing an advanced or special process.

Section II discusses the details of system-level design for low power high performance applications. A new method to determine the DC gain values of OTAs and the effect of 1/f noise are introduced. Then, section III shows the main circuit building blocks design. A novel power efficient OTA and an area-efficient power-efficient small-coefficient resonator are adopted in this design. The measurement and conclusion are given in Section IV and Section V, respectively.

II. System Level Design

A. Modulator Topology

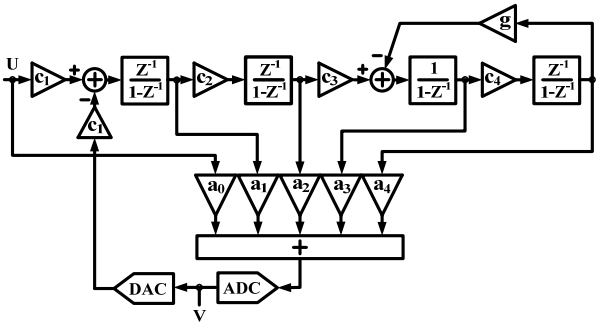

Fig.1. Single-loop 4th-order modulator topology.

The proposed 4th-order modulator topology with OSR= 64 is shown in Fig.1. Single-loop topology is preferable for low voltage low power applications because it is more insensitive to analog circuit non-idealities, such as OTA DC gain, switch on-resistance and so on [1]. Also, a fully feedforward architecture widely used in recent years is adopted [1], [9]. This feedforward architecture has extra signal paths from the outputs of the integrators to the quantizer, so most signal energy can be prevented from leaking into the loop. The design requirements of the OTAs can be relaxed, and the power consumption can be also reduced greatly. Although single-loop multi-bit modulator topology can allow lower power with a lower OSR, it is hard to realize a feedback Digital-to-Analog Converter (DAC) with a linearity much better than 10~12 bits without trimming [10]. Usually, a Dynamic Element Matching (DEM) circuit consuming extra power and area is required to remove the nonlinearity and in-band tones caused by the capacitor-element mismatch of the feedback DAC [10]. Besides, a super low power multi-bit quantizer is difficult to be implemented due to the reference resistor string consuming much extra power and area. Finally, single-loop single-bit modulator architecture with inherent linearity was proposed in this paper.

The coefficients of the proposed modulator are summa-

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rized in Table I. There is a local resonator feedback loop with a gain efficient of g between the last two integrators, which is to put two zeros at the edge of the signal band and improve the performance. Its Noise Transform Function (NTF) can be calculated as

$$NTF(z)=\frac{(z-1)^2[(z-1)^2+c_4gz]}{[(z-1)^2+a_1c_1(z-1)+a_2c_1c_2][(z-1)^2+c_4gz]+[a_3(z-1)+a_4c_4]c_1c_2c_3z} \quad (1)$$

TABLE I
MODULATOR COEFFICIENTS

Integrator Coefficients	Feedforward Coefficients	Resonator Coefficients
	a_0=1.0	
c_1=1/3	a_1=2.0	g=1/90
c_2=2/7	a_2=3.0	
c_3=1/4	a_3=1.5	
c_4=1/7	a_4=2.0	

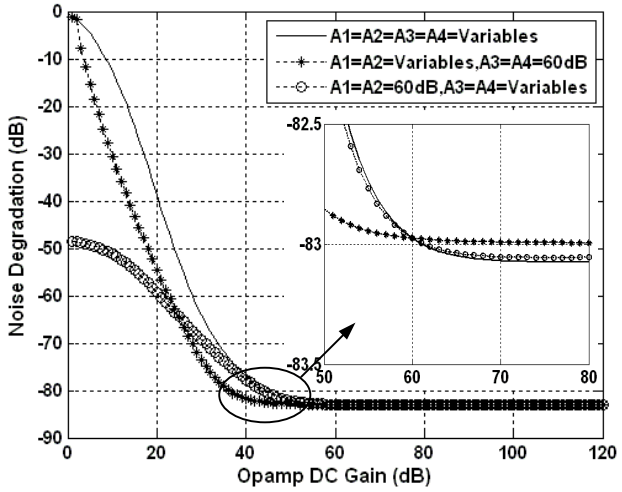


Fig. 2. Noise degradation versus different DC gain values.

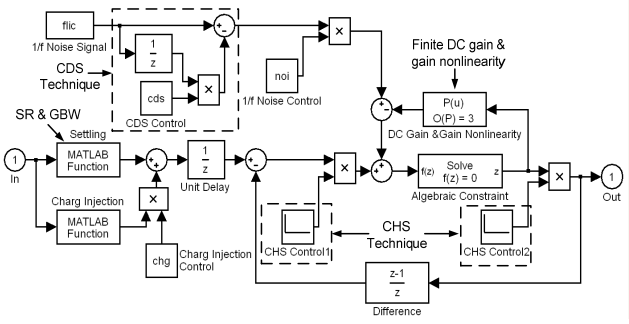


Fig.3. An improved integrator behavioral model.

B. OTA DC Gain Requirement

OTA, a key block in Delta-Sigma modulators, is adopted to compose a switched-capacitor integrator. The modulator performance is greatly affected by the non-idealities of OTA, including finite DC gain, finite GBW, finite SR, etc.

As mentioned in [1], to save the energy and time of the system-level design, the DC gain values of all the OTAs are regarded as a same value when considering the finite DC gain effect on the performance. There is no doubt that this analysis is inadequate. In this paper, a simple and efficient method is presented to determine the OTA DC gain values. When taking into account the finite DC gain factor, the NTF of the proposed modulator can be rewritten as

$$NTF(z)=\frac{(z-p_1)(z-p_2)[(z-p_3)(z-p_4)+c_4g_2p_3p_4z]}{[(z-p_1)(z-p_2)+a_1c_1p_1(z-p_2)+a_2c_1c_2p_1p_2][(z-p_3)(z-p_4)+c_4g_2p_3p_4z]+A^*z} \quad (2)$$

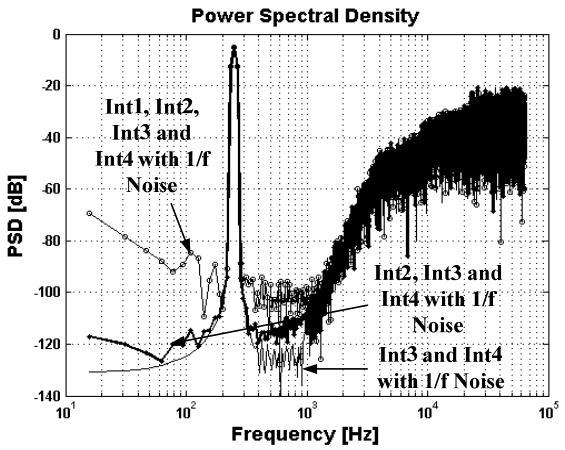
Where

$$A=c_1c_2c_3p_1p_2p_3[a_3(z-p_4)+a_4c_4p_4]$$

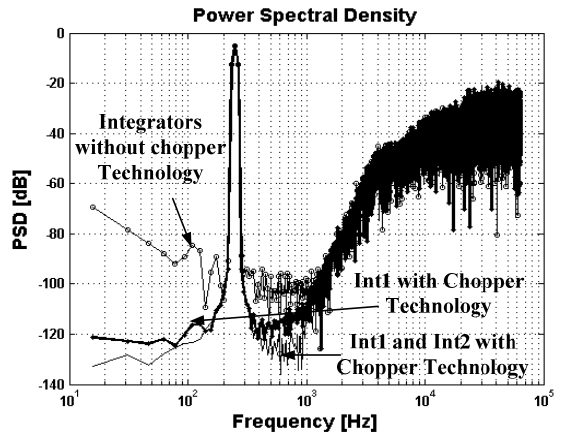
$$p_i=1-\frac{1}{A_{dc}(i)}\ (i=1\sim4)$$

$A_{dc}(i)$ is the DC gain value of the i-th OTA.

Then, this equation is processed by MATLAB, and the modulator's noise degradation versus different DC gain values is shown in Fig. 2. There are three curves with different meanings in this figure. One curve is that the DC gain values of all the OTAs are variable. In another curve, the DC gain values of the first two OTAs are variable while the other OTAs' DC gain values are set to 60dB. The last curve means that the DC gain values of the last two OTAs are variable while the other OTAs' DC gain values are chosen to 60dB. From the figure, it can be seen that the DC gain values of all the OTAs should be as large as possible (≥ 60dB) in order to attain the best noise degradation.



(a) With considering 1/f noise in each integrator.



(b) With adopting CHS technique in each integrator.

Fig.4. Simulation results with the effect of 1/f noise.

C. Effect of 1/f Noise in Integrators

The required bandwidth of the proposed modulator is between 20Hz~1 kHz. And the 1/f noise is a well-known low frequency noise. Hence, a noise cancellation technique

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should be adopted to ensure the noise degradation good over the required bandwidth. Correlated Double Sampling (CDS) and Chopper Stabilization (CHS) are two typical low frequency noise cancellation techniques, which are usually adopted to reduce the effects of the opamp imperfections including noise (mainly 1/f and thermal noise) and the input-referred DC offset voltage. However, the CDS technique requires more capacitor area and induces more thermal noise [11]. So this design uses the CHS technique to cancel the 1/f noise since its implementation is simple and area-efficient.

Fig.3 shows an improved integrator behavioral model in SIMULINK. The implementation of the CHS technique model is similar with the circuit operation principle. 1/f noise signal is generated by a MATLAB procedure. The simulation results with considering 1/f noise and adopting the CHS technique in each integrator are shown in Fig.4. From these figures, it can be inferred that the 1/f noise in INT3 and INt4 does not have dominant impact on the performance while the noise in INT1 and INT2 does, especially the 1/f noise in the first integrator. Therefore, the CHS technique should be adopted in the first two integrators to reduce the 1/f noise.

D. Sampling Capacitors

The sampling capacitor in the first integrator is chosen to satisfy the KT/C noise requirement shown as below

$$C_S = \frac{8KT^* DR}{V^2_{in,max} * OSR} \tag{3}$$

where K is the Boltzmann constant, T is the absolute temperature, DR is the dynamic range, OSR is the oversampling ratio and $V_{in,max}$ is the maximum amplitude of a sinusoidal input. Usually, $V_{in,max}$ is regarded as the amplitude of a full-scale sinusoidal input [3]. However, actually, $V_{in,max}$ is impossible to reach the full-scale range due to the stability requirement. So the maximum input amplitude is used in this paper. The OSR is 64 and the $V_{in,max}$ is $0.6V_{pp}$. The DR is set to 100dB for a design margin. For a 1.5V reference voltage, the required sampling capacitance in the first integrator is 6.4pF. The final sampling capacitance is selected as 7 pF for an extra noise margin. The values of other capacitances are shown in Table II.

To evaluate the effect of non-idealities completely, a developed integrator behavioral model including the slew rate, gain bandwidth, finite DC gain and gain nonlinearity, leakage current, 1/f noise, CHS technique and CDS technique is shown in Fig. 3. Through the comprehensive system-level design, a low power high performance modulator structure is proposed in this design.

TABLE II
CAPACITORS OF THE PROPOSED MODULATOR

Sampling Capacitors	C_{s1}=7.0pF	C_{s2}=1.0pF	C_{s3}=0.5pF	C_{s4}=0.2pF
Integrating Capacitors	C_{i1}=21.0pF	C_{i2}=3.5pF	C_{i3}=2.0pF	C_{i4}=0.7pF

III. BUILDING BLOCK CIRCUITS DESIGN

A. Low Voltage Low Power OTA

As the most critical part of a modulator, OTA usually consumes most of the total power. Especially, the OTA in the first integrator sometimes consumes more than half of the total power and has dominant impact on the performance. Hence, it is necessary to design a robust OTA.

An OTA topology with a rail-to-rail output swing is usually required in low voltage low power designs [1]. Also, a high-gain and wide-bandwidth OTA is needed to ensure the performance good. Furthermore, single-stage OTA is more power efficient than two-stage type because the latter consumes much more power to drive the compensation capacitor [1]. Therefore, a single-stage OTA topology with rail-to-rail output swing becomes a preferred one in the recent designs. Current mirror OTA topology is a typical one satisfying the requirements. However, the gain value of such an OTA is just about 40dB. A gain enhancement technique without consuming much extra power was proposed in [1], which could provide a more than 60dB voltage gain. However, the OTA proposed in [1] cannot operate normally at a 1.5V supply in a 0.35μm CMOS.

Thus, a novel Class-AB current mirror OTA structure with the current starving technique is proposed in this paper. The proposed OTA is shown in Fig. 5. Its amplifier voltage gain and gain bandwidth product are shown as

$$A_{Gain} \approx \frac{2B^*I}{(V_{GS1}+V_{THP1})} \frac{1}{(1-k)B(\lambda_{N9}+\lambda_{P12})I} = \frac{A_0}{(1-k)} \tag{4}$$

$$GBW \approx \frac{2B^*I}{(V_{GS1}+V_{THP1})C_L} \tag{5}$$

The proposed technique is realized by the transistors M_3 and M_4, which take away most (kI) of the DC current provided by the input transistors M_1 and M_2. In this case, the DC current in the output transistors M_9 and M_{10} is smaller and the output resistances are higher. So the OTA voltage gain is increased. Its class-AB output stage consisting of the current mirrors M_6~M_{13} is implemented through the push-pull operation.

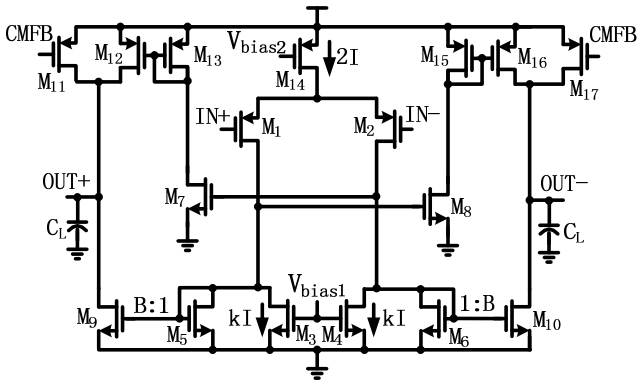

Fig.5. Schematic of the proposed class-AB current mirror OTA with the current starving technique.

An additional CMFB circuit is necessary for a fully differential OTA to ensure the required output CM voltage [12]. The traditional SC CMFB circuit is shown in Fig. 6. Φ_1 and Φ_2 are two non-overlap clocks, V_{cmref} is the desired output common-mode (CM) voltage, V_{bias} is the expected bias voltage, and V_{cmfb} is the CM feedback voltage. However, the effective capacitor load C_T of the CM loop is $C_T = C_2$ when Φ_1 is high and $C_T = C_1+C_2$ when Φ_2 is high. The stability problem may occur due to the variable load. One solution is to set $C_1 << C_2$. But it will degrade the CM loop accuracy and increase the DC settling time [12].

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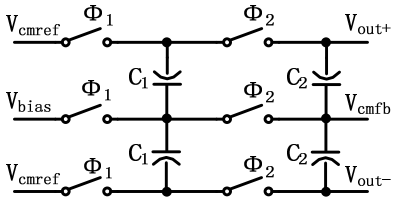

Fig.6. The traditional SC CMFB circuit

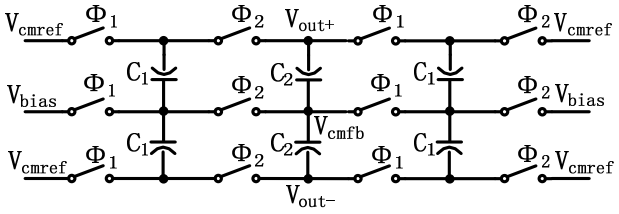

Fig.7. An improved SC CMFB circuit

TABLE III
SIMULATED PERFORMANCE OF THE OTAS

Parameter	OTA1	OTA2	OTA3 & OTA4
Supply Voltage (V)	1.5	1.5	1.5
DC Gain (dB)	65	67	66
Phase Margin (degree)	63	61	71
Slew Rate (V/μs)	1.1	0.9	0.8
GBW (MHz)	2.3	1.7	0.9
Load Capacitor (pF)	11.4	2.9	1.9
Static Current Power (μA)	6.6	2.2	1.4

Therefore, an improved CMFB circuit shown in Fig. 7 is proposed [12]. In this circuit, an extra set of capacitors C_1 and switches are used. Thus, during every clock phase, the total load capacitor is constant ($C_T = C_1+C_2$). The circuit also has very lower error and settles faster than the traditional circuit [12]. Its main drawback is that it needs a little more switchers and capacitors.

Table III shows the simulation results of the designed OTAs. The results show that the proposed OTA in the first integrator achieves a DC voltage gain of 65 dB at a 1.5 V supply. For an 11.4pF load capacitor, the GBW is 2.3MHz and the static current power consumption is only 6.6μA.

Actually, there is some parasitic capacitance at the bottom terminal of the PIP capacitor when the capacitor is fabricated, which is always ignored in many works [1]-[3]. In this design, this bottom terminal parasitic effect is considered, so about extra 20% of the capacitance is added to the total OTA capacitor load. The effective load capacitances $C_{L,eff}$ is shown below:

$$C_{L,eff}(i)=C_S(i)||C_I(i)+0.2*C_I(i)+(1+0.2)*C_{Sum} \quad (6)$$

where $C_{Sum}=C_S(i+1)+C_{cmfb1}+C_{cmfb2}+C_{ff}(i)$

$C_S(i)$, $C_I(i)$ and $C_{ff}(i)$ are the sampling capacitor, the integrating capacitor and the feedforward capacitor of the i-th integrator, respectively. $C_S(i+1)$ is the sampling capacitor of the (i+1)-th integrator. C_{cmfb1} and C_{cmfb2} are the capacitors in the SC CMFB circuit. Because the designed integrator is a half-delay one, so the sampling capacitance of the next stage should be considered.

B. Novel Efficient Resonator Circuit

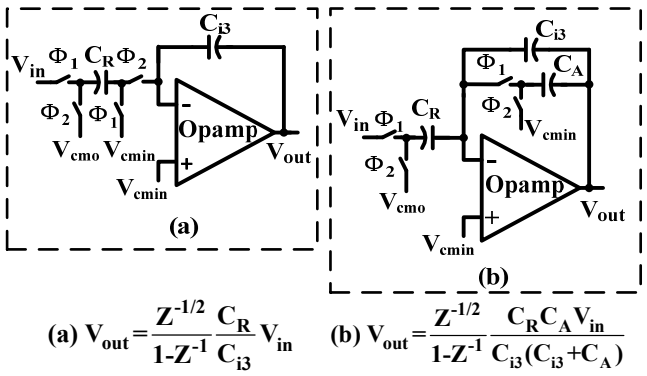

Fig.8. Schematic diagrams and transfer functions of two resonators: (a) traditional type (b) proposed type.

A local resonator with a coefficient value of 1/90 is between the third integrator and the fourth integrator. If a conventional resonator structure with a coefficient gain of C_R/C_{i3} shown in Fig.8 (a) is used in this design. Thus, the values of the sampling capacitor and the integrating capacitor in the third integrator must be greatly increased to realize this very small ratio. For example, when the resonator capacitance C_R is set to 0.1pF, the value of the integrating capacitor C_{i3} should be 9pF. And the value of the sampling capacitor C_{s3} is also increased to 2.25pF. Obviously, according to the equation (6), the effective capacitor load of the 3rd-OTA is changed to be 4.6pF. Hence, this will increase both area cost and power consumption.

In this paper, an area-efficient power-efficient parasitic-insensitive integrator was proposed to realize this local resonator. This proposed integrator has been used to implement a notch filter in [13]. According to its operating principle, it can be also adopted to realize a resonator in Delta-Sigma modulators. Fig.8 (b) shows the schematic of the proposed inverting integrator. To realize a small-coefficient resonator, C_{i3} is typically a large capacitor while C_R and C_A are small capacitors. The operation of this resonator is as follows. During phase1, a charge $V_{in}C_R$ is transferred to C_{i3} and the intermediate output voltage $V_o(n-1/2)$ is sampled by C_A. During phase2, C_R withdraws the charge $V_{in}C_R$ from C_{i3} and C_A redistributes its charge with C_{i3}.

When realizing a coefficient of 1/90 with this resonator, the values of both C_{s3} and C_{i3} are not changed. The values of C_R and C_A are just set to 0.2pF and 0.25pF, respectively. Thus, the effective 3rd-OTA capacitor load is reduced to 1.9pF. Compared with the conventional resonator, the proposed resonator can save about 75% capacitor area and 50% power consumption based on the estimation and simulation.

C. Complete Modulator Circuit

The complete modulator circuit is shown in Fig.9. It is a fully differential feedforward type and has four integrators with a one-bit quantizer. CHS technique was used in the first two integrators, and a proposed resonator with a coefficient of 1/90 is between the third integrator and the fourth integrator. The input CM voltage is set to 0.3V, and the output CM voltage is chosen to $1/2V_{DD}$.

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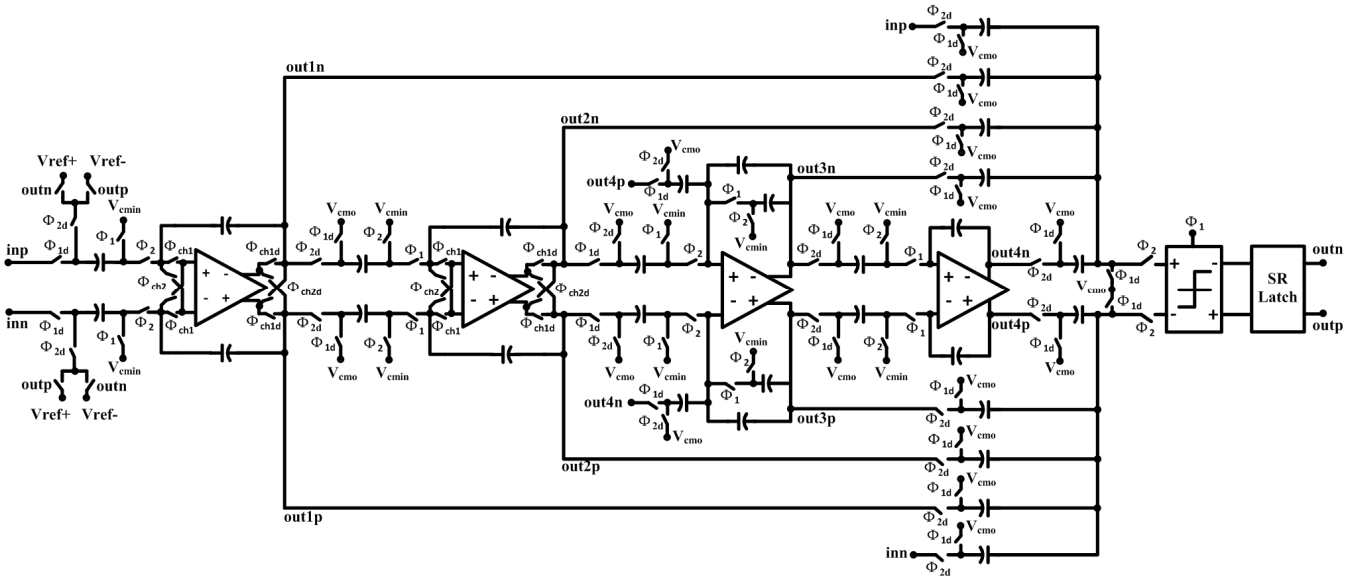

Fig. 9. Schematic of the complete proposed modulator circuit.

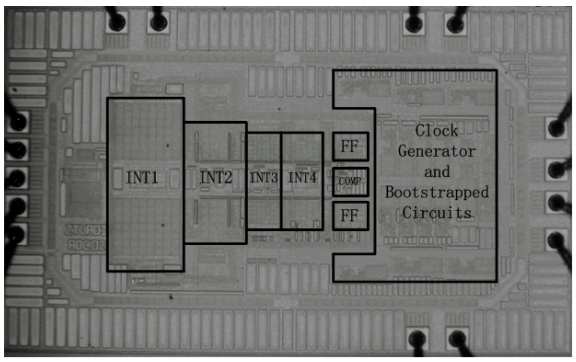

Fig.10. Chip photograph.

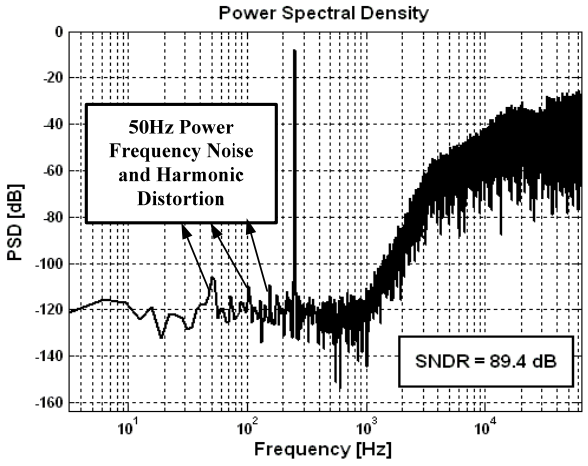

Fig.11. Measured output spectrum of the designed modulator with 40960 samples.

IV. Measurement Results

The designed modulator is implemented in a 0.35μm CMOS process and the chip photograph is shown in Fig.10. The chip's core size with pads is 2mm x 1mm. Fig.11 shows the measured output spectrum of a 250Hz sinusoid signal with 40960 samples. Fig.12 shows the measured SNR and SNDR curves versus the input signal amplitudes normalized by reference voltage. The amplitudes of harmonic distortions are low due to the large enough GBW and slew rate in this design. The peak SNR reaches 90.2dB while the peak SNDR without (with) power frequency noise is 89.8dB (88.4dB). The DR is 95dB over the 1 kHz bandwidth. Clocked at 128 kHz, the analog power is only 18μW at a 1.5V supply, and the digital power is less than 2μW due to the low clock frequency. The measured performance is summarized in Table IV.

Table V shows the performance comparison with recent published low power high performance Delta-Sigma modulators. The Figure-of-Merit (FOM) is defined as

$$\mathrm{FOM} = \mathrm{DR}_{\mathrm{dB}} + 10 * \log\left(\frac{\mathrm{BW}}{\mathrm{P}}\right) \qquad (7)$$

where BW is the signal bandwidth and P is the total power consumption of the modulator.

V. Conclusion

A 20μW 95dB DR sing-bit 4th-order Delta-Sigma modulator using novel power efficient OTA and resonator is implemented in a low cost 0.35μm CMOS process. Through the comprehensive system-level design witch uses a new method to determine the DC gain values and considers the effects of 1/f noise, a low power high performance modulator topology is proposed in this paper. In the circuit-level design, a novel power efficient current mirror Class-AB OTA with a fast-settling less-error SC CMFB circuit is introduced. And the bottom terminal parasitic-effect of PIP capacitors is also considered. About extra 20% of the capacitance is added to the total capacitor load. Besides, an area-efficient power-efficient parasitic-insensitive resonator is adopted to realize a coefficient of 1/90 for 50% power consumption and 75% area cost reduction over the conventional design. The measured results show this modulator can be used in portable measurement applications. The designed modulator shows very high FOM among the recent low power high performance modulators.

Acknowledgment

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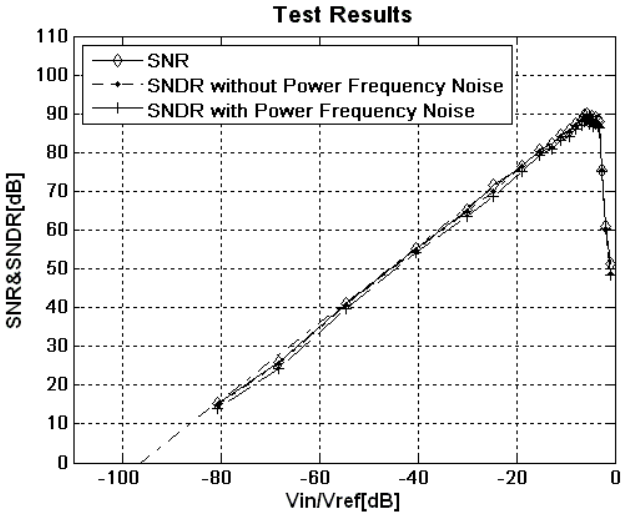

Fig.12. Measured SNR and SNDR versus input amplitude.

TABLE IV
PERFORMANCE SUMMARY

Parameter		Measurement Results
Supply Voltage (V)		1.5V
Power	Analog circuits	18μW
	Digital circuits	2μW
Peak SNR		90.2dB
Peak SNDR		89.8dB
Dynamic Range		95.0dB
Sampling Frequancy		128kHz
Signal Bandwidth		1kHz
OSR		64
FOM		172

TABLE V
PERFORMANCE COMPARISON WITH RECENT MODULATORS

Modulator	ISSCC02 18.3 Jens[5]	JSSC04 Yao[1]	JSSC08 Roh[2]	JSSC09 Chae[3]	This Work 2008
Process (nm)	180	90	130	350	350
V_{DD} (V)	0.7	1.0	0.9	1.2	1.5
f_S (MHz)	1.024	4	2	2	0.128
BW (kHz)	8	20	20	8	1
Power (μW)	80	140	60	5.6	20
DR (dB)	75	88	83	76	95
Peak SNR (dB)	70	85	82.2	72	90.2
Peak SNDR (dB)	67	81	73.1	63	89.8
FOM of Modulator	155.0	169.5	168.2	167.5	172.0

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