High-Conversion-Ratio Switched-Capacitor Step-Up DC-DC Converter

Yuen-Haw Chang and Chen-Wei Lee

Abstract—**A closed-loop scheme of high-conversion-ratio switched-capacitor (HCRSC) converter is proposed based on pulse-width-modulation (PWM) control for step-up conversion and regulation. In the HCRSC, there are totally 4 sets of series-parallel SC cells between source Vs and output Vo, where each cell has 3 capacitors. With the capacitors charging in parallel and discharging in series cyclically, each cell will be a small converter of triple voltage gain. And by the 4 cells working complementarily, the main function is to boost Vo voltage up to 3×3 times of Vs at most. In addition, this SC converter needs no magnetic element, e.g. inductor/transformer, so I.C. fabrication will be promising for VLSI applications. Here, the closed-loop HCRSC is simulated by OrCAD Spice, and some cases are included as: voltage conversion and output ripple percentage, output robustness against source variation, and regulation capability of converter with loading variation. The results are illustrated to show the efficacy of the proposed scheme.**

***Index Terms*—high-conversion-ratio; step-up; pulse-width-modulation; switched-capacitor.**

I. INTRODUCTION

In recent years, due to the popularity of portable electronic equipments, for example, PDA, notebook, cellular phone, digital camera, pager, and e-book …etc., their DC-DC power module always asks for some good features of small volume, light weight, high power density and efficiency, and good regulation capability. Besides, to fit in with requirements of various functions all in one, both multiple output choice and flexible controller design become essential to power module design gradually. So, more manufactures and researchers pay much attention to this topic on development of a more flexible converter for low-power applications, ultimately requiring DC-DC converters realized on a chip by mixed analog VLSI technology.

The idea of switched-capacitor (SC) circuit has existed for nearly half a century. In the last decade, the various types of SC converters have been suggested to achieve the power conversion because the SC does not require any magnetic elements, so the integrated circuit fabrication is not only pretty promising but also avoiding classical converter restriction on the physical size of the magnetic devices. In 1990, the first SC step-down converters were proposed by Japan researchers [1], and their idea is to switch MOSFETS cyclically according to 4 periods of capacitors charging/discharging for step-down conversion. In 1993, Cheong *et al.* suggested a modified SC converter with two symmetry SC cells working in the two periods [2]. In the first period, the capacitors of one SC cell are charged by a constant voltage source, and at the same time the capacitors of the other cell are discharged into the load. Then, in the second period, the two cells exchange each other. Then, combining with pulse width modulation (PWM) technique, they proposed a new step-up DC-DC converter by using duty-cycle control [3]. In 1994, Ngo *et al.* first proposed a current control of SC converters by using a saturated transistor as a controllable current source [4]. In 1996, Chung and Ioinovici suggested a current-mode SC for improving current waveforms [5]. Following this idea, Chang proposed an integrated SC step-up/down DC-DC/DC-AC converter [6-8]. In 2008, Axelrod *et al.* suggested a hybrid PWM converter based on switched-capacitor/inductor structure [9]. However, these SC circuits still provide the maximum gain proportional to the number of pumping capacitors. In this paper, the high-conversion-ratio SC converter is proposed for the step-up conversion with the voltage gain of multiplication of 3×3, and the closed-loop control is also considered for the regulation capability.

This work was supported in part by the National Science Council of Taiwan, R.O.C., under Grant NSC 98-2221-E-324-024.

Yuen-Haw Chang and Chen-Wei Lee are with the Department and Graduate Institute of Computer Science and Information Engineering, Chaoyang University of Technology, Taichung County, Taiwan, R.O.C. Post code:413. (e-mail: cyhfyc@cyut.edu.tw, s9727615@cyut.edu.tw).

II. CONFIGURATION OF HCRSC CONVERTER

Fig.1 shows the overall circuit configuration of HCRSC step-up DC-DC converter, and it contains two parts: "power part" and "control part" for achieving the closed-loop step-up conversion and regulation.

A. HCRSC scheme:

Firstly, the power part: HCRSC step-up DC-DC converter is as shown in the upper half of Fig. 1. The converter is mainly composed of four SC cells (Cell A1, A2, B1 and B2) between source and output. For more details, it includes 12 pumping capacitors (C_{A11}~C_{A13}, C_{A21}~C_{A23}, C_{B11}~C_{B13}, C_{B21}~C_{B23}), 30 switches (S1~S6, S_{A11}~S_{A16}, S_{A21}~S_{A26}, S_{B11}~S_{B16} , S_{B21}~S_{B26}), where each capacitor has the same capacitance C (C_{A11}=…=C_{B11}=…=C_{A21}=…=C_{B21}=…=C). Fig. 2 shows the theoretical waveforms of HCRSC converter.

ISBN: 978-988-18210-4-1
ISSN: 2078-0958 (Print); ISSN: 2078-0966 (Online)

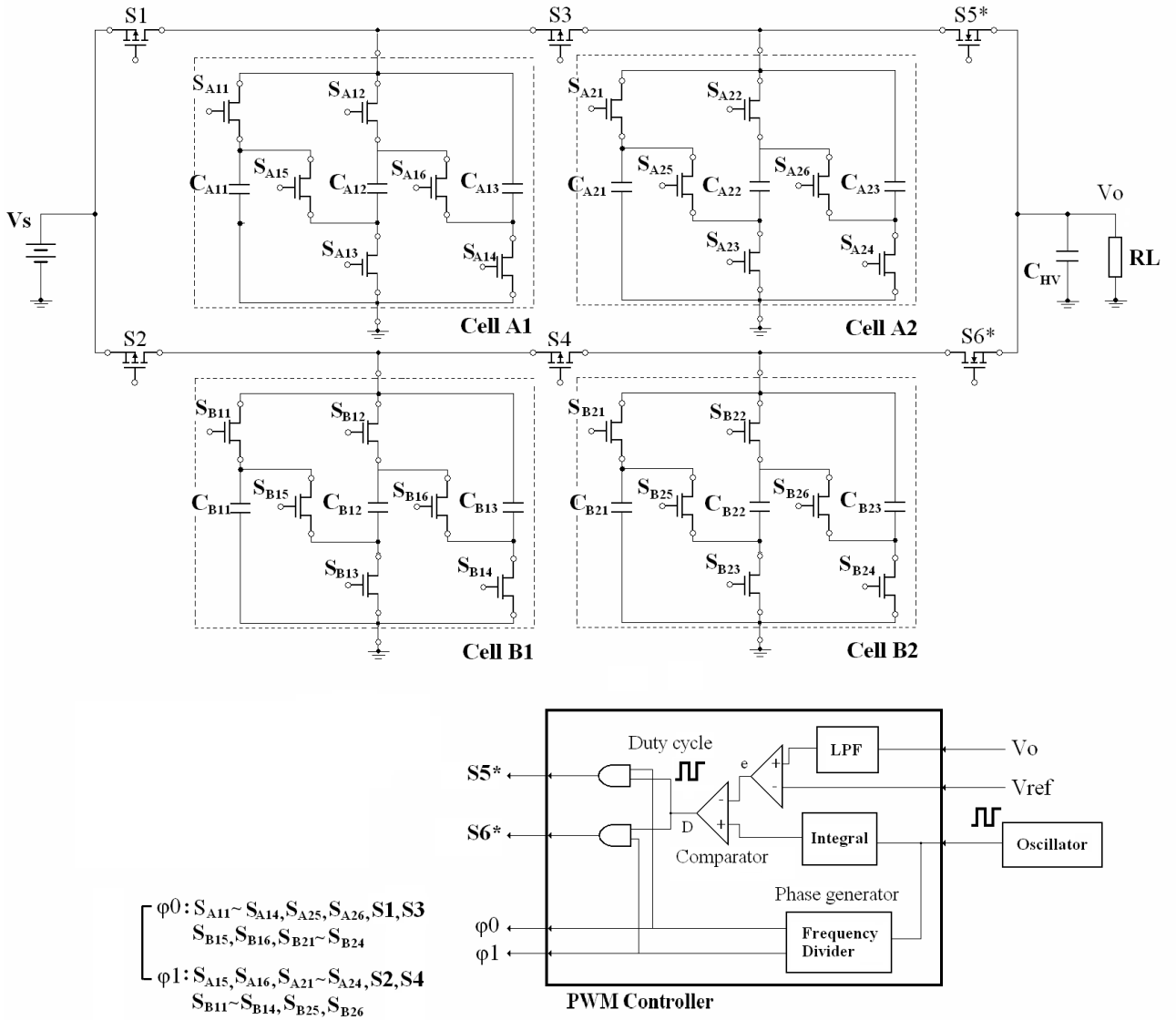
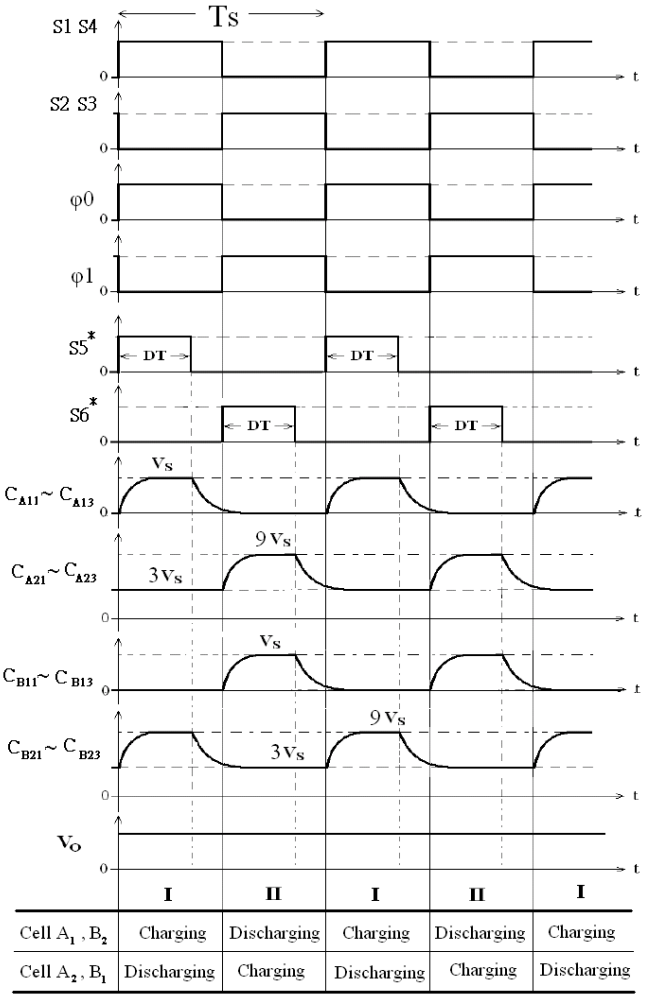


Fig.1 Configuration of HCRSC converter

Obviously, there are totally two phases (Phase I and Phase II) in a switching cycle Ts. In Phase I, Cell A1, B2 are running at capacitor-in-parallel-charging, and Cell A2, B1 are at capacitor-in-series-discharging. Fig. 3(a) shows the topology of Phase I. In Phase II, Cell A2, B1 are working at capacitor-in-parallel-charging, and Cell A1, B2 are at capacitor-in-series-discharging. Fig. 3(b) deals with the Phase II topology. Because (A1,B2) and (A2,B1) are working complementarily, their operations are symmetrical. Such an interleaved scheme will be helpful to the reliability of conversion.

Secondly, the control part: PWM controller is used as shown in the lower half of Fig. 1, which is functionally composed of low-pass filter (LPF), PWM block and phase generator. From the view of controller signal flow, the feedback signal: the attenuated output Vo is sent into the OP-amplifier LPF for high-frequency noise rejection. Next, the filtered Vo is compared with the desired output reference V_{ref} so as to produce the duty cycle D via the PWM block. At the same time, a phase generator can be realized based on frequency divider to generate the MOSFET drive signals (S1~ S4 and S_{A11}~S_{A16}, S_{A21}~S_{A26}, S_{B11}~S_{B16}, S_{B21}~S_{B26}) just like the waveforms in Fig. 2. To avoid the overlap between φ0 and φ1, a simple non-overlapping latch is needed as show in Fig. 4. In the figure, there are 4 inverter gates respectively at the upper / lower branch for increasing delay time. Through XOR gate, φ0(f0) and φ1(f1) can be obtained as a set of non-overlapping signals to drive the MOSFETs. In addition, signal S5*/S6* can be generated via logic AND combination between signal φ0/φ1 and duty cycle D. In this

ISBN: 978-988-18210-4-1
ISSN: 2078-0958 (Print); ISSN: 2078-0966 (Online)



Cell A_1 , B_2	Charging	Discharging	Charging	Discharging	Charging
Cell A_2 , B_1	Discharging	Charging	Discharging	Charging	Discharging

Fig. 2 Theoretical waveforms of HCRSC converter

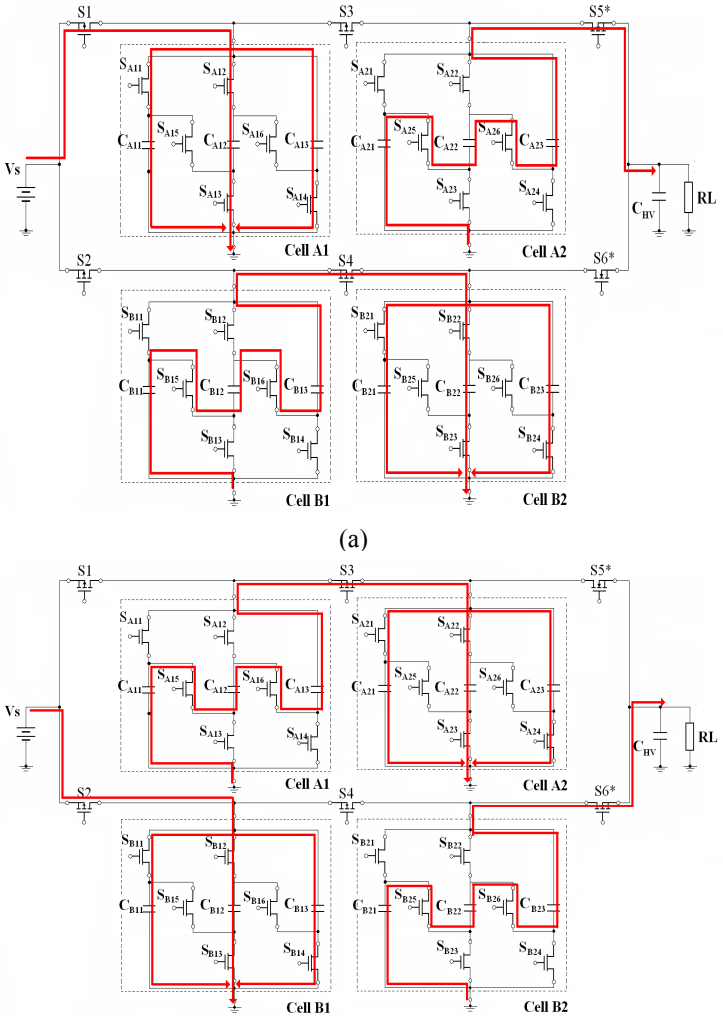


Fig. 3 (a) The first half-cycle topology
(b) The second half-cycle topology

paper, by using the PWM control, the regulation capability of HCRSC step-up DC-DC converter will be improved for different desired outputs, source or loading variations.

B. HCRSC operation:

For achieving step-up function, the converter needs two operations: charging into capacitors in parallel and discharging from capacitors in series.

(1). For the first half-cycle:
S1, S4: on, S5* : PWM on;
S2, S3 ,S6*: off.

C_{A11}~C_{A13} in Cell A1 are linearly charged in parallel by the Vs. C_{A21}~C_{A23} in Cell A2 are discharging in series to supply the load RL. At the same time, C_{B11}~C_{B13} in Cell B1 are discharging in series to Cell B2.

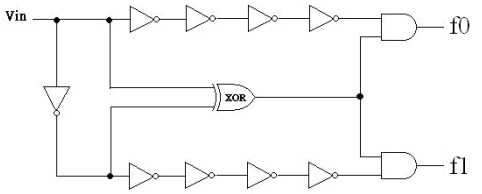


Fig.4 Latch in phase generator

(2). For the second half-cycle:
S2, S3 : on, S6* : PWM on;
S1, S4, S5* : off.

C_{B11}~C_{B13} in Cell B1 are linearly charged in parallel by the Vs. C_{B21}~C_{B23} in Cell B2 are discharging in series to supply

ISBN: 978-988-18210-4-1
ISSN: 2078-0958 (Print); ISSN: 2078-0966 (Online)

Table 1. all components of converter

Supply source	5V
Switch capacitor (C_{A11}~C_{A23}, C_{B11}~C_{B23})	100uF
Load of capacitor (C_{HV})	200uF
Resistance of capacitor (r)	0.01Ω
MOSFET of SC step-up (Cell A1~B2)	power MOSFET
Channel resistance	0.01Ω
Voltage ripple	0.008%
Frequency of φ0 and φ1	25kHz
MOSFET S5*, S6* W/L	30000u/0.18u
Load of resistance	300Ω

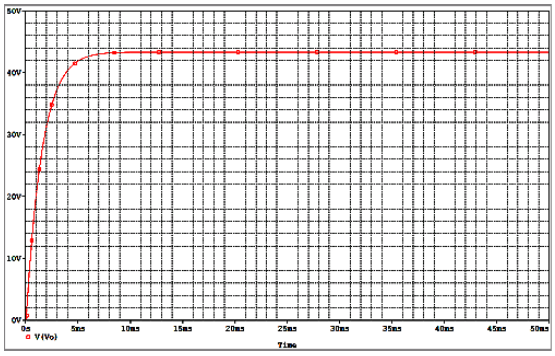
the load RL. At the same time, C_{A11}~C_{A13} in Cell A1 are discharging in series to Cell A2. By charging in parallel and discharging in series for capacitors cyclically, the basic step-up function can be realized to boost Vo up to 3×3 times of Vs at most.

III. EXAMPLE OF HCRSC CONVERTER

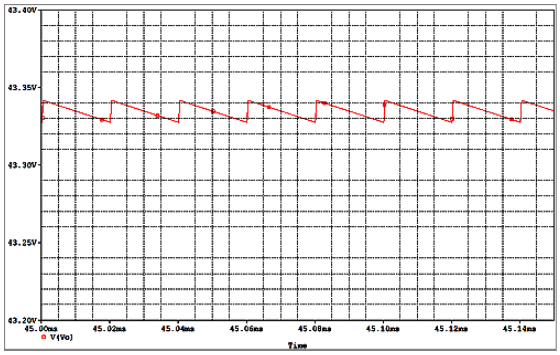
In this section, HCRSC step-up DC-DC converter with PWM control is made in circuit layout, and simulated by OrCAD tool. The results are illustrated to verify the efficacy of the proposed HCRSC converter. Here, all component parameters of the converter are listed in Table 1. This converter is preparing to supply the load RL=300Ω. For checking closed-loop performance, some topics will be simulated and discussed, including: (1) voltage conversion, output ripple percentage and power efficiency, (2) output robustness against source disturbance, and (3) regulation capability to loading variation.

Firstly, the HCR SCconverter is operated at a switching frequency of 25 kHz to convert source Vs=5V into output voltage Vo=44V (V_{ref}=44V) for supplying the load RL= 300Ω. The output voltage conversion, output voltage ripple and power efficiency versus time are simulated as shown in Fig. 5(a)-(c), respectively. In Fig. 5(a), it can be found that the settling time of the step-up converter is smaller than 10 ms, and the steady-state value of Vo is really reaching 44V. In Fig. 5(b), the output ripple percentage can be easily found as rp=Δvo/Vo=0.0332%. In Fig. 5(c), the steady-state power efficiency can be found at about 97.06%. These results show that the step-up converter has a pretty good transient and steady-state performance.

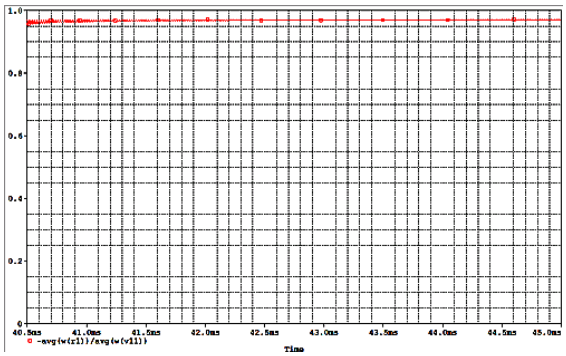
Secondly, the output robustness against source variation is simulated here. Since the source voltage is getting diminished naturally with running time of battery, or affected by the bad-quality one, the output robustness against source noises must be considered. While the source voltage is getting down exponentially from Vs=5V→4.5V



(a)



(b)



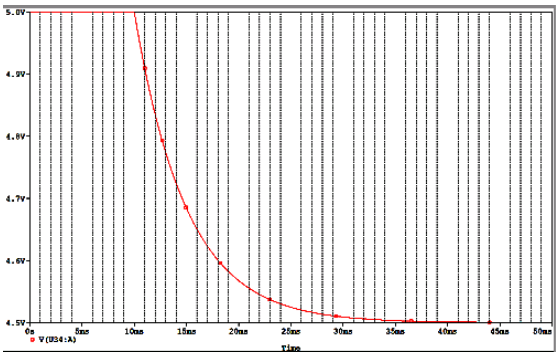
(c)

Fig.5 (a) Source voltage Vo = 44V.
(b) Output voltage ripple rp = 0.0332%.
(c) power efficiency η = 97.06%.

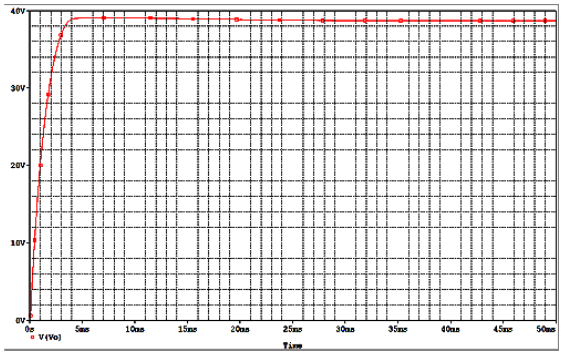
as Fig. 6(a), output voltage Vo is still following 39V (V_{ref} = 39V) as shown in Fig 6(b). While Vs has a ripple disturbance of 1V V_{P-P} around 4.5V as Fig. 7(a), output voltage Vo can hold on 32V (V_{ref}=32V) through the closed-loop compensation as shown in Fig. 7(b). From these results, it is obvious that the closed-loop HCR SC step-up converter has an excellent robustness against external source noises, e.g. natural voltage dropping or impurity DC source.

Finally, the regulation capability of the converter with

ISBN: 978-988-18210-4-1
ISSN: 2078-0958 (Print); ISSN: 2078-0966 (Online)

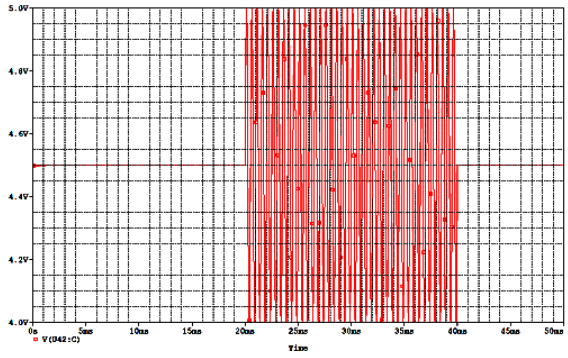


(a)

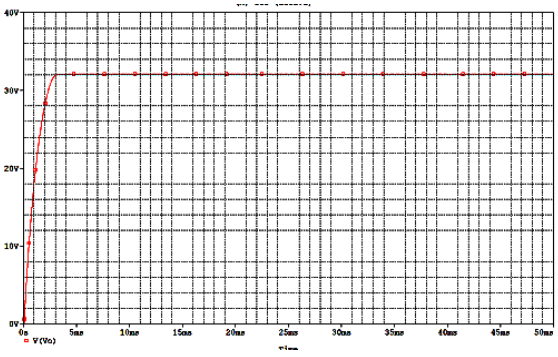


(b)

Fig.6 (a) Source voltage Vs:5V→4.5V.
(b) Output voltage Vo=39V (V_{ref} = 39V).

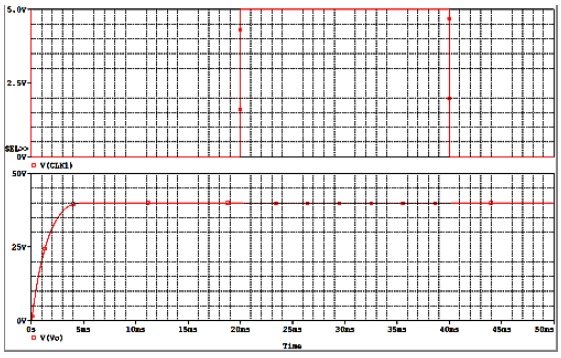


(a)

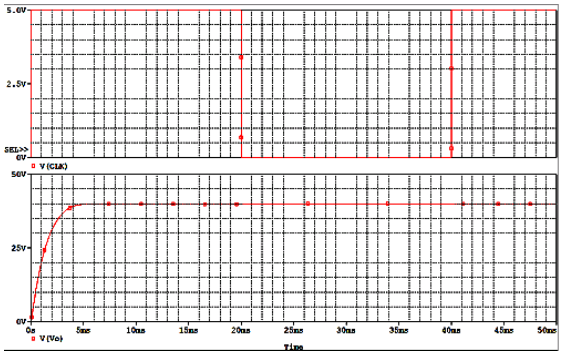


(b)

Fig.7 (a) Source voltage Vs: 4.5+0.5sin(1000t).
(b) Output voltage Vo=32V (V_{ref} = 32V).



(a)



(b)

Fig.8 (a) Waveform of Vo when RL: 300→150Ω.
(b) Waveform of Vo when RL: 150→300Ω.

loading variation is discussed. Fig. 8(a) shows the transient output waveform when the load is added in double, i.e. the same load is added and connected in parallel with the output terminals (RL=300Ω→150Ω). Fig. 8(b) shows the transient output waveform when the added load is removed away from the output terminals (RL=150Ω→300Ω). From Fig. 8(a)-(b), it is obvious that the output voltage can be still regulated to hold on about 40V (V_{ref}=40V) in spite of the extra loading variations. Of course, we can also find that the output ripple becomes larger during the time interval of supplying the heavier load (20~40ms). So, by using this PWM controller, this closed-loop HCRSC converter has a pretty good regulation capability.

IV. Conclusions

A HCRSC step-up DC-DC converter is proposed with PWM control here. The advantages of the proposed scheme are as: (1) The SC converter does not require use of inductive elements, so the I.C. fabrication is promising for realization. (2) This HCRSC needs just 6 capacitors (12 capacitors for the interleaved scheme) to boost Vo up to 3×3 times of Vs at most. (3) The PWM is adopted not only to enhance the output regulation for different desired outputs, but also to reinforce the robustness against source or loading variations. At present, we have implemented the hardware

ISBN: 978-988-18210-4-1
ISSN: 2078-0958 (Print); ISSN: 2078-0966 (Online)

of HCRSC converter as shown the photo of Fig. 9. Next, some more experimental results will be obtained and measured for the verification of our HCRSC step-up DC-DC converter.

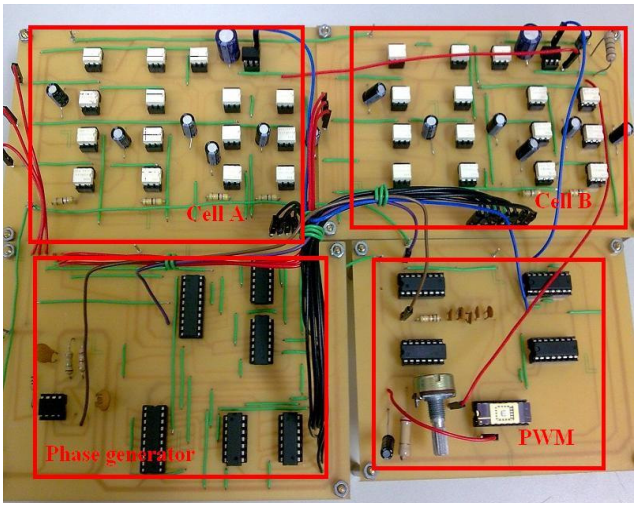


Fig. 9 .hardware implementation of HCRSC converter

REFERENCES

[1] T. Umeno, K. Takahashi, I. Oota, F. Ueno, and T. Inoue, "New switched-capacitor DC-DC converter with low input current ripple and its hybridization," *in Proc. 33rd IEEE Midwest Symposium on Circuits and Systems, Calgary, Canada*, pp.1091-1094, 1990.

[2] S. V. Cheong, S. H. Chung, and A. Ioinovici, "Duty-cycle control boosts dc-dc converters," *IEEE Circuits and Devices Mag.*, vol.9, no.2, pp.36-37, 1993.

[3] O. C. Mak, Y. C. Wong, and A. Ioinovici, "Step-up DC power supply based on a switched-capacitor circuit," *IEEE Trans. on Industrial Electronics*, vol.42, no.1, pp.90-97, 1995.

[4] K. D. T. Ngo and R. Webster, "Steady-state analysis and design of a switched-capacitor DC-DC converter," *IEEE Trans. Aerospace and Electronic Systems*, vol.30, pp.92-101, 1994.

[5] H. Chung and A. Ioinovici, "Switched-capacitor-based DC-to-DC converter with improved input current waveform," *in Proceedings IEEE Int. Symp. Circuits and Systems, Atlanta, USA*, pp.541-544, 1996.

[6] Y.-H. Chang, "Design and analysis of power-CMOS-gate-based switched-capacitor DC-DC converter with step-down and step-up modes," *Int. J. Circuit Theory and Appl.*, vol.31, pp.483-511, 2003.

[7] Y.-H. Chang, "Design and analysis of power-CMOS-gate-Based Switched-Capacitor Boost DC-AC Inverter," *IEEE Trans. Circuits Syst.-I: Fundamental Theory and Appl.*, vol.51, pp.1998-2016, 2004.

[8] Y.-H. Chang, "CPLD-based closed-loop implementation of switched-capacitor step-down DC-DC converter for multiple output choices," *IET Electric Power Applications*, vol.1, pp.926-935, 2007.

[9] B. Axelrod, Y. Berkovich, and A. Ioinovici, "Switched-capacitor/ switched-inductor structures for getting transformer-less hybrid DC-DC PWM converter," *IEEE Trans. Circuits Syst.-I: Regular Papers*, vol.55**,** pp.687-696, 2008.

ISBN: 978-988-18210-4-1
ISSN: 2078-0958 (Print); ISSN: 2078-0966 (Online)