A Low Power Audio Delta-Sigma Modulator with Opamp-Shared and Opamp-Switched Techniques

Hanqing Wang, Jian Xu, and Xiaobo Wu

***Abstract*— A high power efficient opamp-shared and opamp-switched delta-sigma modulator (DSM) has been presented. It employs a fourth-order single loop 17-level DSM with an input feed forward gain stage. It is shown that power consumption can be largely reduced by using half delay integrators and switched opamp, and sharing opamp between integrator stages. The proposed DSM, designed on 0.35μm TSMC process under 1.8V supply, achieves 121μW power dissipation with 20 kHz bandwidth and 111.9dB Signal-to-Quantization Noise Ratio (SQNR).**

Keywords: opamp shared technique, delta-sigma modulator (DSM), switched opamp technique, switch capacitor (SC) circuit

I. Introduction

With the ever-increasing demand for portable multimedia systems and continued long standby time, the improvement of low voltage low power dissipation systems is rapid. Analog to digital conversion (ADC) is widely used in these products. DSM based on switch-capacitor (SC) circuit is well suitable for high resolution low voltage ADC since the need for precision components or stringent matching between constituent elements is avoided [1]. Input feedforward structure [2] with multi-bit quantization is helpful for high precision under the constraints of low supply voltage and low power dissipation [3]. Because input feedforward demands less capacitors and switches compared with feedback structure and multi-bit quantization reduces greatly the output swing of integrator that relaxes the slew rate requirement of operational transconductance amplifier (OTA). However, in a multi-bit modulator, a dynamic element matching (DEM) circuit has to be utilized to remove tones and nonlinearities caused by capacitor mismatch of feedback digital to analog converter (DAC).

A SC integrator (Fig.1), the main component in DSM, has a sampling phase and integration phase. The OTA in a SC integrator is actually used during only integration phase. A way to reduce the power consumption of integrators is to turn off the OTA during sampling phase [4] or share OTA between integrator stages [5].

In this paper, a low power fourth-order 4-bit audio DSM is presented. Significant power saving has been achieved by employing opamp shared technique and switched opamp technique.

The rest of this paper is organized as follows: Section II describes the architecture of proposed DSM, and discusses the various design choices. In Section III, the implementation of system and various circuit blocks is discussed. In Section IV, the simulation results and the comparison with other works are presented. Finally, a brief conclusion is given in Section V.

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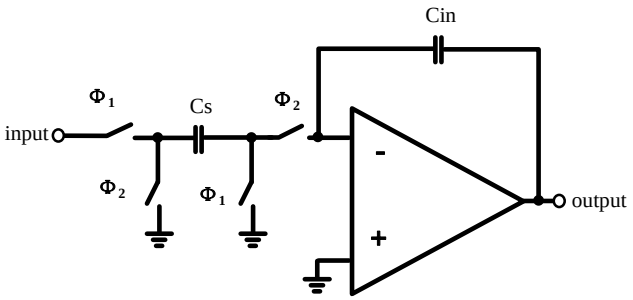

Fig.1 The general SC integrator

II. System Level Details

A. Delta-Sigma Modulator Topology

Fig.2 shows a traditional cascade of resonators with weighted feedforward summation (CRFF structure) [3]. This structure is suitable for half delay integrators because the total delay of two stages is one period. But it has an unacceptable problem, especially in high frequency multi-bit modulators. Because three processes of quantization, DWA and DAC are forced to be finished during the same phase. It deteriorates the stability of DSM. Fig.3 illustrates the block diagram of proposed DSM which has 4th order loop filter. Alternating delayed and non-delayed integrators are used, and two delay units are inserted after the second and fourth integrator to divide the quantization, DWA and DAC process into two phases. The reason will be discussed in detail in circuit implementation. Alternating delayed and non-delayed integrators means that four integrators are all half delayed in circuit implementation. And opamp shared technique and switched opamp technique can be used to reduce power dissipation.

Different with single bit DSM, multi-bit DSM needs an analog adder. If rang of input signal is near to power supply voltage, the output swing of analog adder is very large. The amplifier in the adder must have a very large slew rate, resulting in more power consumption. A two-step summation method can be used to solve the problem. Outputs of four integrators are summed at the first step by an amplifier. The output swing of the amplifier is only about 20% of full input signal swing (Fig.4). The second summation can be implemented by a SC adder, adding the output signal of the first adder and the input signal of DSM. The output signal of second adder is large as the input signal of DSM, but an amplifier is avoided here.

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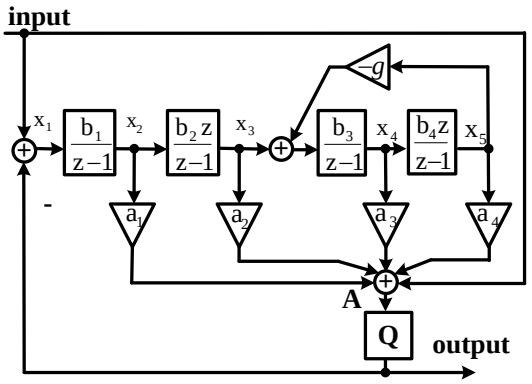

Fig.2 Traditional cascade of resonators with weighted feedforward summation (CRFF structure)

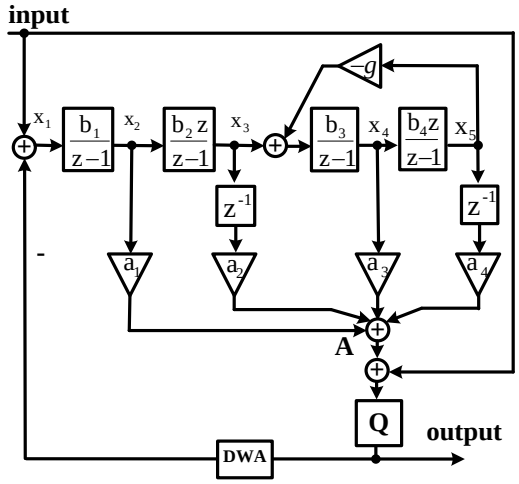

Fig. 3 Proposed CRFF modulator with feedforward delay

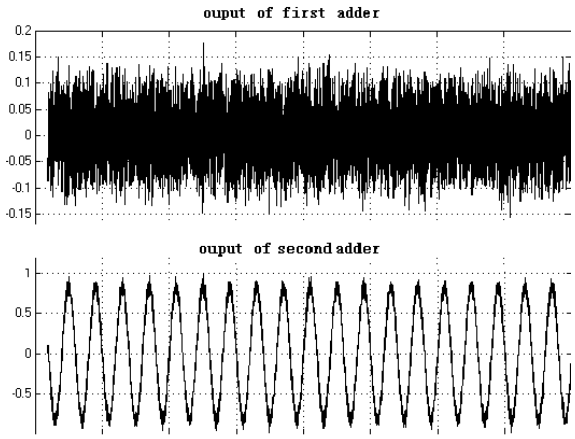

Fig. 4 Outputs of two-step summation

B. Choice of Sampling Capacitor and NTF

Another method to reduce power dissipation is to lower the oversampling ratio (OSR), thus the slowing down the sampling clock rate, meanwhile the sampling capacitor increases unfortunately. An OSR of 32 was chosen in this design. The calculated sampling capacitor of first stage is 4.5pF to achieve a noise floor of 100dB. Sampling capacitor of 6pF was used to provide adequate noise margin. Simulated result has a noise floor of 106dB.

The NTF influences several aspects of modulators performance. Multi-bit quantization enables NTFs with large out-of-band gains, which results in reduced in-band quantization noise. However, a large out-of-band gain may cause stability problem. Furthermore, discrete comparator was chosen to achieve low power. Effect of offset of discrete comparator is larger than comparator with preamplifier because CDS technique cannot be used to cancel it. Large out-of-band gain will aggravate the effect of offset. Based on these considerations, an out-of-band gain of 2.2 was adopted. And in MATLAB simulation, offsets generated randomly were added to comparators. It has been proved that the offset of comparators has a tiny deterioration of SQNR that can be negligible. Taking the offset into consideration, the peak SQNDR simulated in MATLAB is 116dB within the 20-kHz audio signal band.

C. Dynamic Element Matching

The main problem of multi-bit converters is the linearity requirement of the DAC. Since it is in the feedback loop, the nonlinearity error will enter into the first integrator without shaping and deteriorate the performance. Several dynamic element matching (DEM) techniques [3] provide a way to reduce the effect of nonlinearity of DAC. Data weighted averaging (DWA) is employed for its simple implementation and good performance.

III. Circuit Implementation

A. Opamp switched and shared technique

As mentioned above, alternating delayed and non-delayed integrators can use opamp shared technique and switched opamp technique. In a traditional CRFF structure (Fig2.), the quantization and DEM, together with DAC must be finished during the same phase. Taking the first and second integrator for example, the delays from the input of DSM to the quantizer through two paths of integrators are both one period. In circuit implementation, integrators are half delayed, and the analog adder needs a half period itself. So there is no extra half period left for quantization and DEM. Fortunately, this problem can be solved by proposed DSM structure. Two delay units are inserted after second and fourth stage that quantization and DWA are accomplished during phase 1, not disturbing the DAC process.

There are totally four integrators and two adders (Fig.3). The switched-capacitor circuit implementation of the proposed DSM is shown in Fig.5. The sampling capacitor of first stage is 6pF, which is greatly larger than anyone else. So the first OTA can be turned off directly during sampling phase to save half period power instead of sharing with other stages. The load of second stages approximates the third one, and one OTA can be shared between them. As the timing diagram of the modulator shows in Fig.6, the first OTA is turned off during phase 1, and the second OTA operates alternatively for second and third stage. The fourth integrator can share another OTA with the analog adder. There are only three OTAs needed in this DSM.

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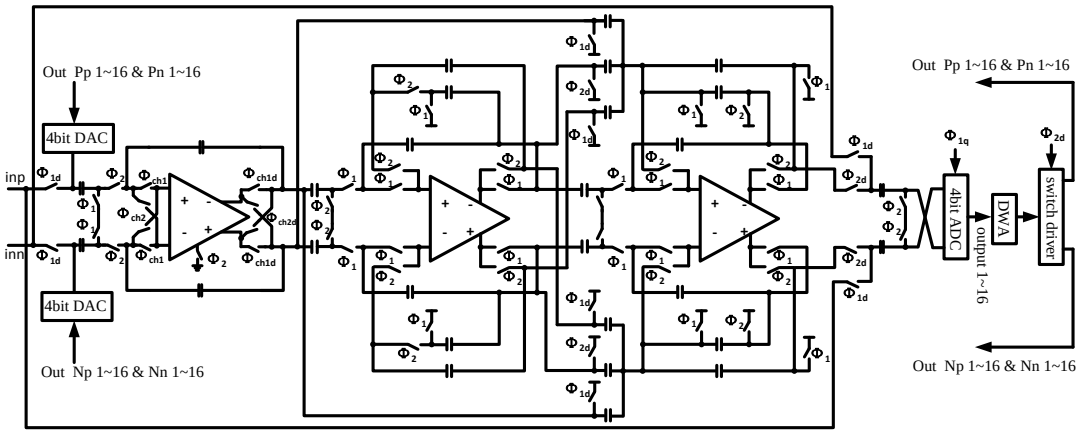


Fig5. Switched-capacitor implementation of the proposed modulator

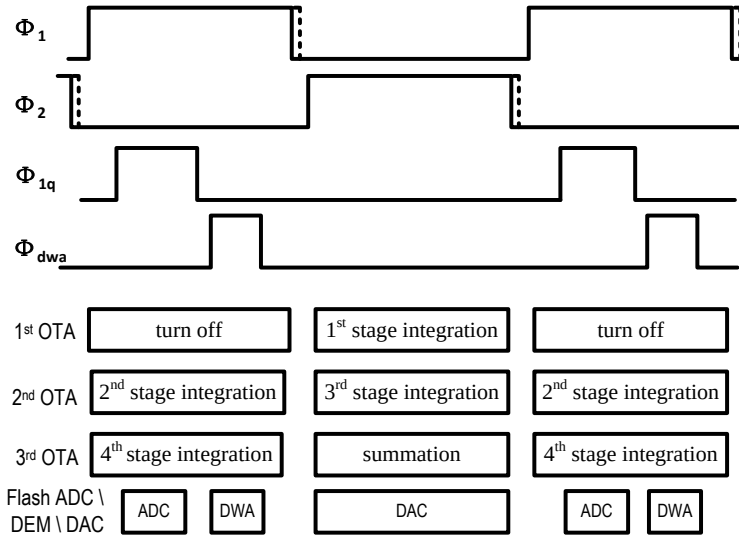
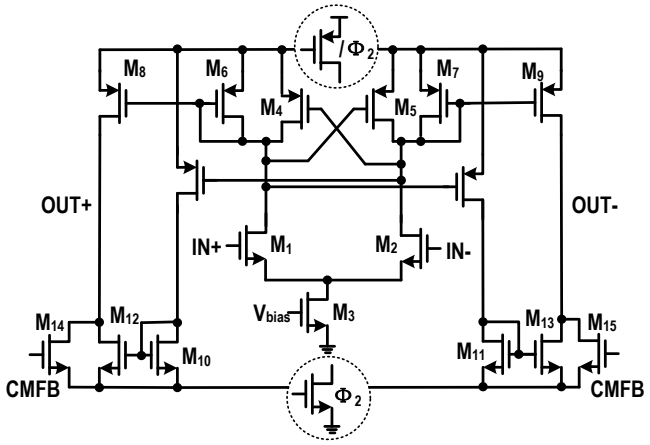
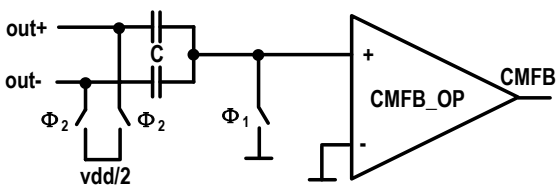


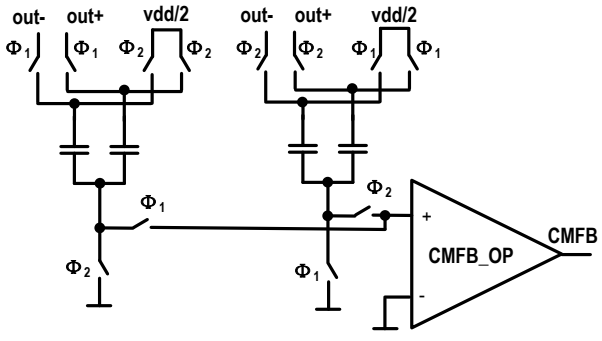
Fig6. Timing diagram of the proposed DSM



(a)



(b)



(c)

Fig7. OTA used in DSM (a) Main amplifier
(b) Common-mode feedback (CMFB) for switched opamp
(c) CMFB for shared opamp

B. OTA Design

The circuit schematic of the opamp used in the DSM is shown in Fig 7 (a). It is a current mirror OTA with class AB output. Cross couple structure (M_4~M_7) is used to increase the DC gain. The ratio of $(W/L)_4$ is set to be about half ratio of $(W/L)_6$. For differential input signals, polarities of transconductance of M_4 and M_6 are opposite, but would not cancel each other completely because of different sizes. And non-dominant pole generated at this node, the opamp can be

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regarded as single stage amplifier that compensation is unnecessary.

The first integrator determines the overall noise and linearity of modulator. A NMOS differential input pair is used to effectively attenuate the thermal noise because of its high transconductance. The high NMOS flicker noise will be concerned. In fact, the NMOS differential input pair is preferred even considering the flicker noise. Since sizes of four cross-coupled transistors cannot be large because of the constraint of phase margin. And the dc gain of first stage is low that flicker noise of load transistors is even larger than input pair. As the equation (1) shows, L_4 is smaller than L_1 and the second part can be dominant. Furthermore, mobility of hole is slower than that of electron. The ratio μ_p/μ_n can reduce the second part but enlarge if a PMOS differential input pair is used. So a NMOS input pair with PMOS load is recommended. The chopper stabilization technique is employed to remove the flicker noise and offset. The chopping frequency is half sampling clock frequency.

$$\begin{aligned}\overline{v_{in,1/f}^2} &\approx \frac{K}{C_{ox}f}\left(\frac{1}{(WL)_1}+\frac{1}{(WL)_4}\frac{g_{m4}^2}{g_{m1}^2}+\frac{1}{(WL)_6}\frac{g_{m6}^2}{g_{m1}^2}\right)\\ &= \frac{K}{C_{ox}f}\left(\frac{1}{(WL)_1}+\frac{1}{(WL)_4}\frac{u_p(W/L)_4 I_4}{u_n(W/L)_1 I_1}+\frac{1}{(WL)_6}\frac{u_p(W/L)_6 I_6}{u_n(W/L)_1 I_1}\right)\\ &= \frac{K}{C_{ox}f}\left[\frac{1}{(WL)_1}+\left(\frac{I_4}{L_4^2}+\frac{I_6}{L_6^2}\right)\frac{u_p}{u_n(W/L)_1 I_1}\right] \sim L_4 = L_6, I_4 + I_6 = I_1\\ &= \frac{K}{C_{ox}f}\frac{1}{W_1}\left(\frac{1}{L_1}+\frac{L_1 u_p}{L_4^2 u_n}\right)\end{aligned} \quad (1)$$

The OTA in first integrator is turned off during sampling phase to reduce power dissipation. Two switches in dash line circle are used to turn off the OTA. The performance of the OTA is shown in table I.

The common-mode feedback (CMFB) circuit is shown in Fig.5 (b). The capacitors are pre-charged to VDD/2 when OTA is turned off, unlike general switched opamp to VDD. This circuit works as follows: During the inactive clock phase of the opamp, the left plates of capacitors are pre-charged up to VDD/2 and the opposite plates are connected to common-mode input voltage V_{REF}. During the active one, the positive input of CMFB_OP is virtual V_{REF}. According to law of conservation of charge, the charge at positive input node between two clock phases is unchanged: $2C*VDD/2 - (CV_{out+} + CV_{out-}) = 0$, $(V_{out+} + V_{out-})/2 = VDD/2$ can be derived.

In opamp shared technique, the OTA (take away two switches in circles) has to be switched between two integration phases during which the common-mode output voltage must be both around VDD/2. Traditional discrete time CMFB circuit [6] is slow and not well to stabilize the common-mode output. A new CMFB circuit inspired from switched opamp technique is shown in Fig.5(c). Two pairs of capacitors are used to stabilize the common-mode output voltage alternatively.

C. Two-Step Summation

Fig.8 shows the circuit implementation. The capacitor samples the output of analog adder during phase 2, and during phase 1 the input feedforward signal shifts the voltage of capacitor. The charge in the right plate of capacitor is unchanged during two phases according to law of conservation of charge. The process of level shift in capacitor

TABLE I
SIMULATED PERFORMANCE OF THE OTA

DC gain	56dB
Unity gain frequency	12.6MHz
Phase margin	62°
Slew rate	4.9v/μs
Power dissipation	40μW

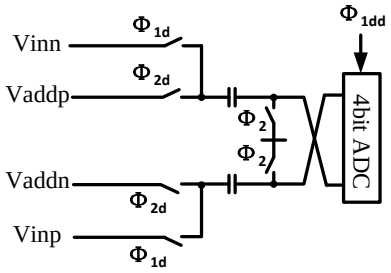

Fig8. Analog summation and quantizer

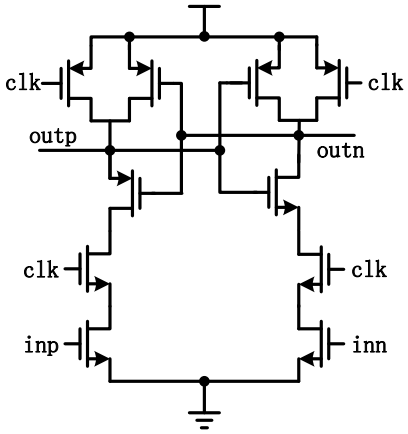

Fig9. Discrete time comparator

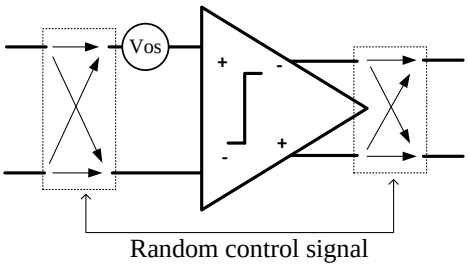

Fig10. Comparator offset DEM

is very fast, so the quantizer needs only a little delay to get the right voltage. There are no charge sharing here, so signal attenuation would not happen and signal compensation is avoided.

D. Flash ADC

The discrete time comparator used in this study is shown in Fig9, without quiescent dissipation. Assuming the comparator has a high offset of about 0.2 LSB, the SQNR decreases about 3 dB which is acceptable. However, the comparator DEM technique can be used to eliminate the little deterioration, shown in Fig.10. Distortion caused by comparator offsets is mitigated by using random signal to chop the offset [7].

In a fully differential quantization, symmetry is a helpful

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characteristic. Only nine comparators are needed to realize 4-bit quantization. One comparator is used to determine the polarity of input signal to either pass the input through or its inverted waveform to the other eight comparators [8]. The power consumption and chip size are reduced.

IV. SIMULATION RESULTS

According to the discussions of the previous sections, a fourth-order 4-bit DSM is designed with TSMC 0.35μm CMOS process for audio applications. Fig.11 shows the output spectrum of Cadence simulation result with a -1dBFS sine-wave input and achieved SQNDR is 111.9dB. Table II lists the performance summary.

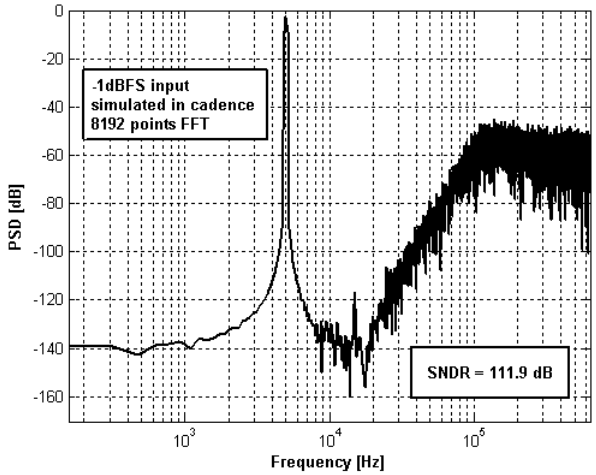

Fig.11 simulation result in cadence

TABLE II
PERFORMANCE SUMMARY OF PROPOSED DSM

Specifications		Value
Sampling rate		1.28MHz
OSR		32
Signal bandwidth		20kHz
Peak SQNDR		112dB
Power	Analog	97μW
	Digital	24μW
Process		TSMC 0.35μm

V. CONCLUSION

In this paper, a low power DSM is designed for audio applications. Combination of Opamp-shared and opamp-switched techniques is used in the DSM, which saves about 40% of total power consumption. The power consumption is only 121 μW and the PSQDNR is 112 dB.

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