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# Design and Implementation of Full Adder Cell with the GDI Technique Based on 0.18µm CMOS Technology

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*Abstract*— **In this paper, The low power and high performance 1-bit full adder cell is proposed. The Gate Diffusion Input (GDI) technique has been used for the simultaneous generation of XOR and XNOR functions. Fourteen states of the arts 1-bit full adders and one proposed full adder are simulated with HSPICE using 0.18µm CMOS Technology at 1.8v supply voltage. The resulting full adder circuit is realized using of the 24 transistors, while having full voltage-swing in all circuit nodes. By optimizing the transistor size in each stage the power and delay are minimized. The results of post-layout simulation compared to similar reported ones illustrate significant improvement. Simulation results show great improvement in terms of Power-Delay-Product (PDP). The power consumption of this adder is 0.78µw.**

*Index Terms*— **Full Adder, GDI Technique, Low Power, Power-Delay-Product (PDP).**

## I. INTRODUCTION

Historically, VLSI designers have used speed as the performance metric. High gains, in terms of performance and silicon area, have been made for digital processors, microprocessors, DSPs (Digital Signal Processors), ASICs (Application Specific ICs), etc. In general, small area and high performance are two conflicting constraints [1]. The power consumed for any given function in CMOS circuit must be reduced for either of the two different reasons: One of these reasons is to reduce heat dissipation in order to allow a large density of functions to be incorporated on an IC chip. Any amount of power dissipation is worthwhile as long as it doesn't degrade overall circuit performance. The other reason is to save energy in battery operated instruments same as electronic watches where average power is in microwatts

In CMOS circuits, the power consumption is proportional to switching activity, capacitive loading and the square of the supply voltage [2].

Full Adder is one of the most important parts of each processor, which is used in floating-point, in the arithmetic logic unit (ALU), digital signal processing, image, video processing, microprocessors and in all the arithmetic operations such as division, multiplication, subtraction. Increasing the performance of a 1-bit Full Adder cell is very effective in increasing the Performance of the whole system[3].

The structure of the rest of this paper is organized as follows: Section II reviews fourteen states of the full adder cells. In section III the Implementation of full adder with the GDI Technique is described. The simulation results are shown in section IV. Finally, section V contains the conclusion.

## II. REVIEW OF FOURTEEN STATE OF THE ART FULL ADDER CELLS

There are different types of CMOS full adder. this section reviewed the fourteen states of the arts 1-bit full adders. This proposed cell is compared with them.

Fourteen state of the art full adder cells are: 10T, 14T, CPL, TFA, TG CMOS, $C^2$MOS, Hybrid, Bridge, FA24T, N-Cell, DPL, Mod2f, HPSC and TSAC.

The first full adder structure in this section is 10T. It has only 10 transistors. The number of transistors is the advantage of this cell which leads to better performance and less silicon area. However poor driving capability and non full swing nodes are the serious problems of this full adder cell. The power consumption of this structure is 1.13µw.It is shown in figure 1(a).

The 14T adder with 14 transistors consumes considerably less power in the order of microwatts and has higher speed. The 14T adder reduces threshold loss problem compared to the previous different types of transistor adders. In future, this kind of low power and high speed adder cell will be used in designing the digital FIR filter and its applications in various fields. The power consumption of this structure is 6.4µw. It is shown in figure 1(b) [4].

The Complementary Pass-transistor Logic (CPL) full adder is shown in figure 1(c). This is contains the 18 transistors that based on NMOS pass-transistor network. This causes low input capacitance and high speed operation. Due to less output voltage swing that is the result of one Vt loss in the output, CPL consumes less power than standard static CMOS circuits. The power consumption of this structure is 2.5µw [4].

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A Transmission Function Full Adder (TFA) based on the transmission function theory is shown in figure 1(d). It has 16 transistors. The power consumption of this structure is 12µw.

A Transmission- Gate Adder (TGA) is shown in figure 1(e). Transmission gate logic circuit is a special kind of pass-transistor logic circuit. It is built by connecting a PMOS transistor and an NMOS transistor in parallel, which are controlled by complementary control signals. Both the PMOS and NMOS transistors will provide the path to the input logic "1" or "0", respectively when they are turned on simultaneously. Thus, there is no voltage drop problem whether the "1" or "0" is passed through it. It contains the 20 transistors [5].

The Complementary CMOS full adder ($C^2$MOS) is shown in figure 1(f) .The advantage of complementary CMOS style is its robustness against voltage scaling and transistor sizing which are essential to provide reliable operation at low voltage and arbitrary transistor. It contains the 28 transistors[5].

Hybrid Full Adder cell, which contains the 26 transistors, utilizes a modified low-power XOR/XNOR circuit. In this circuit worst case delay problems of transitions from 01 to 00 and from 10 to 11 are solved by adding two series PMOS and two series NMOS transistors respectively. The power consumption of this structure is 2.22µw. it is shown in figure 1(g) [4].

The Bridge circuit has 26 transistors which is shown in figure 1(h). This design creates a conditional conjunction between two circuit nodes. Since one of the important parameters in circuit design is the chip area, the proposed style might reduce the area or increase density of transistors in this unit of area. The power consumption of this structure is 1.66µw [6].

The FA24T structure is shown in figure 1(i). This full Adder is based on Bridge style. FA24T has 24 transistors. The body of FA24T has two transistors less than Bridge and has better power consumption. However, in FA24T the Sum generator should wait to receive the Cout signal from the Cout generator; therefore, the delay of FA24T is more than Bridge. The power consumption of this structure is 1.66µw[4].

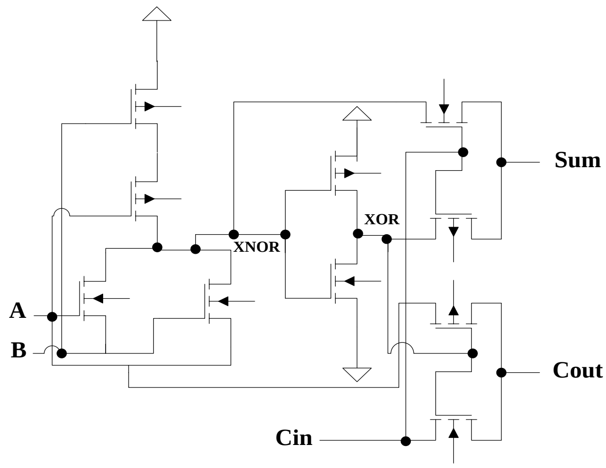
N-CELL contains the 14 transistors and utilizes the low power XOR/XNOR circuit. There is a pass transistors network to produce a non full swing Sum signal and uses four transistors to generate a full swing Cout signal. However, NCELL Full Adder cell has 12 transistors less and better performance in comparison with Hybrid Full Adder cell. The power consumption of this structure is 1.62µw. It is shown in figure 1(j) [4].

The Double Pass-transistor Logic (DPL) Full Adder of the figure 1(k) is a modified version of CPL and contains the 24 transistors. Full swing operation is obtained by simply adding PMOS transistors in parallel with the NMOS transistors in DPL circuits. Therefore, the problems of little noise margin and performance degradation at low supply voltages, which occur in CPL circuits because of the output voltage drop, are avoided. However, the addition of PMOS transistors bring about increased input capacitances. The power consumption of this structure is 2.35µw [4].

Mod2f Full Adder cell of Figure 1(l), which contains the 14 transistors, generates full swing XOR and XNOR signals by utilizing a pass transistor based DCVS circuit. As mentioned in, this leads to higher speed and better performance in comparison with the circuit proposed. The power consumption of this structure is 2.23µw [4].

The HPSC is based on feedback logic, as shown in Figure 1(m). HPSC has a feedback connection between XOR and XNOR function eliminating the non-full- swing operation. The existence of VDD and GND connections give good driving capability to the circuit and the elimination of direct connections between them and avoid the short circuit currents component. There is a delay in switching the feedback transistors. This occurs because of one of the feedback transistors which is switched ON by a weak signal and the other signal is at high impedance state. it contains the 22 transistors and the power consumption of this structure is 0.25µw [7].

The TSAC full adder of Figure 1(n) is based on the $c^2$mos logic style. This circuit has inherited the advantages of $c^2$mos logic style, which has been proved in to be superior in performance to all pass transistor logic style for all logic gates except XOR at high supply voltage. It contains the 26 transistors [7].

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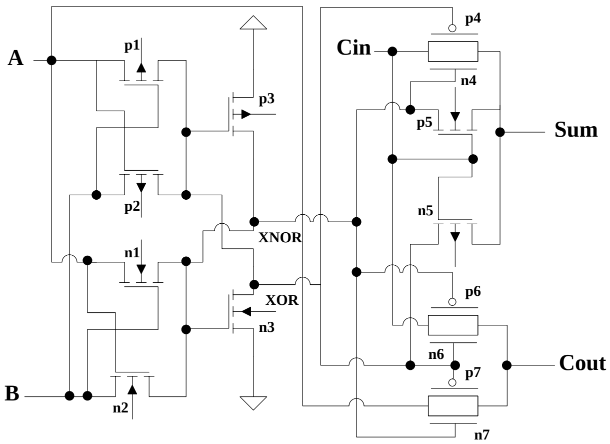


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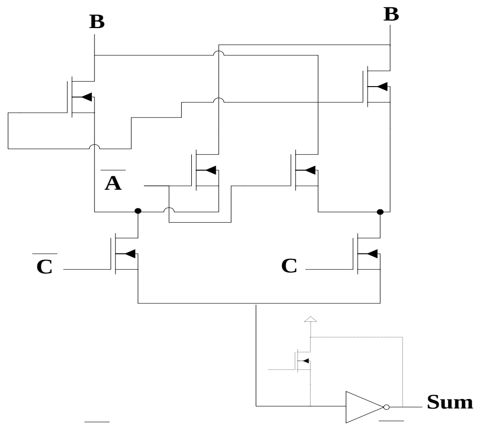


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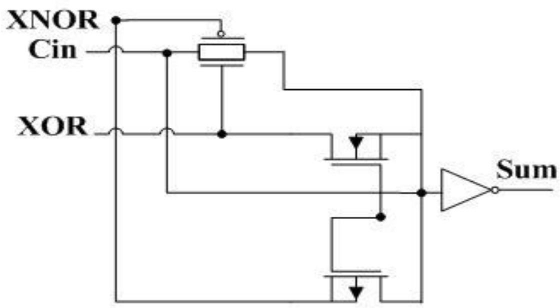


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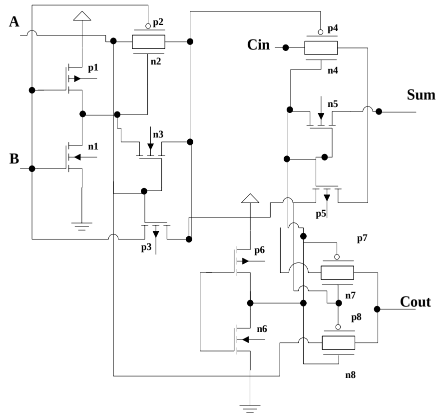


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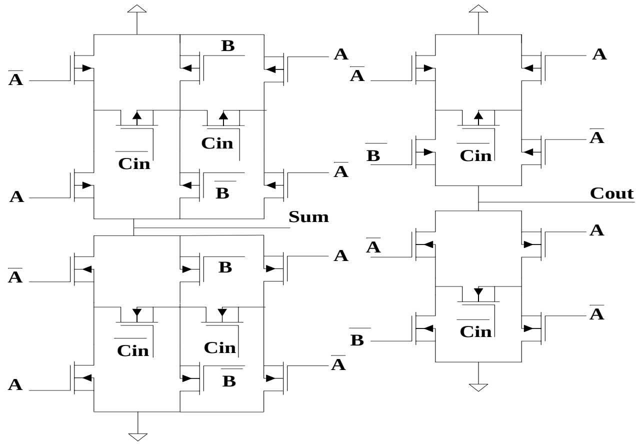


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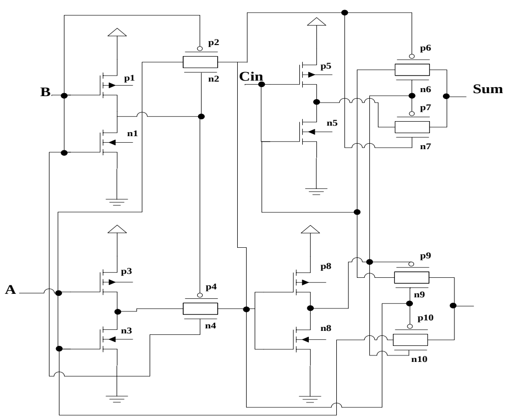


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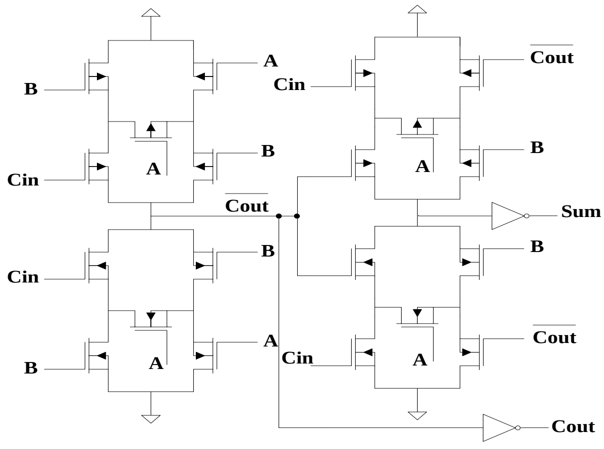


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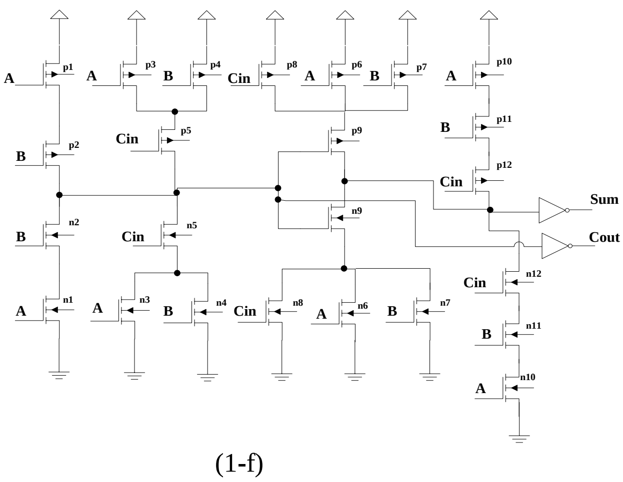


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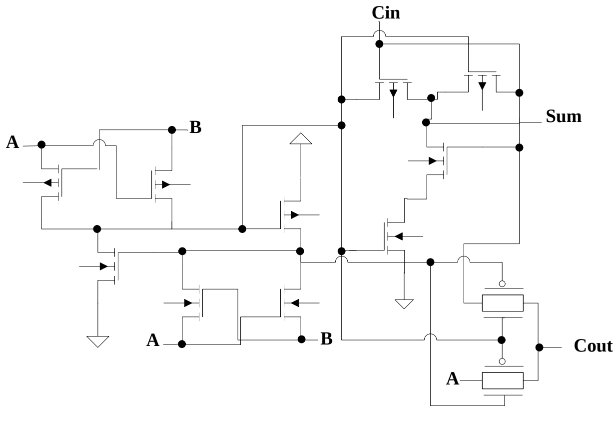


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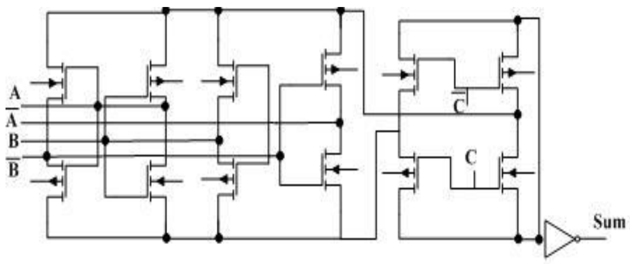


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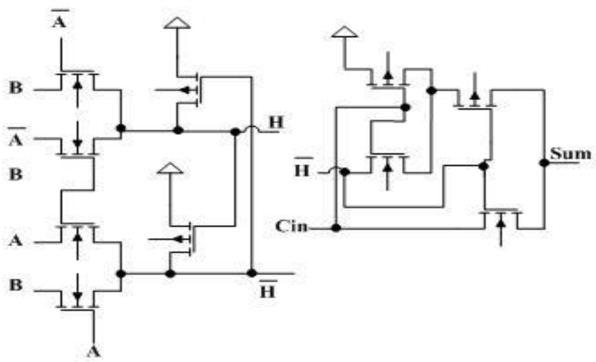


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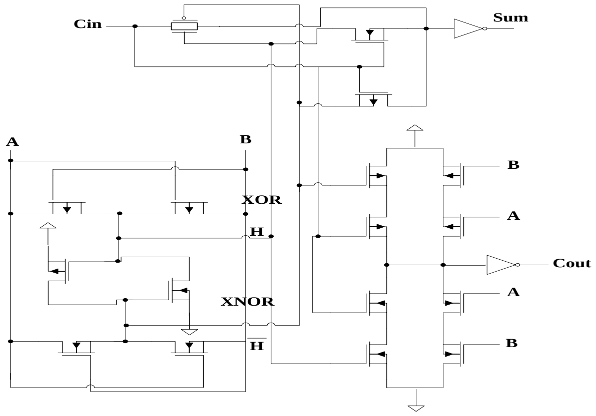


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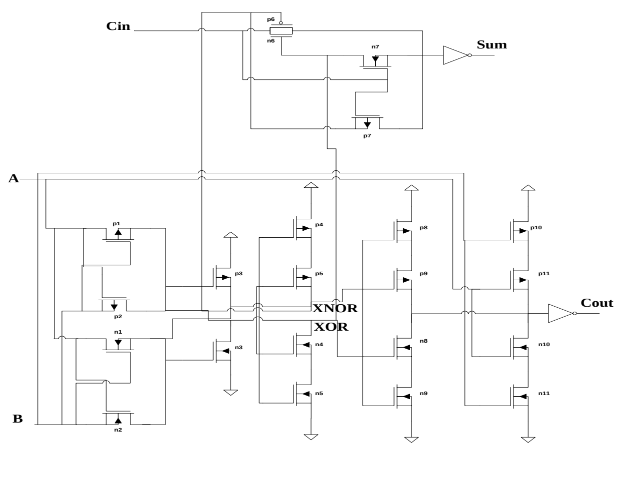


(1-n)

Fig.1- Fourteen state of the art full adder cells .(a)10T, (b)14T, (c)CPL, (d)TFA, (e)TG-Cmos, (f)$C^2$mos, (g)Hybrid, (h)Bridge, (i)FA24T, (j)N-Cell, (k)DPL, (l)Mod2f, (m)HPSC, (n)TSAC.

## III. THE GDI TECHNIQUE AND IMPLEMENTING OF FULL ADDER CELLS

Gate-Diffusion-Input (GDI) method is based on the use of a simple cell as shown in figure .2. At a first glance the basic cell reminds the standard CMOS inverter, but there are some important differences:

1) GDI cell contains three inputs – G (common gate input of NMOS and PMOS), P (input to the source/drain of PMOS), and N (input to the source/drain of NMOS).

2) Bulks of both NMOS and PMOS are connected to N or P respectively, so it can be arbitrarily biased at contrast with CMOS inverter. It must be remarked, that not all the functions are possible in standard P-Well CMOS process, but can be successfully implemented in Twin-Well CMOS or SOI technologies [8].

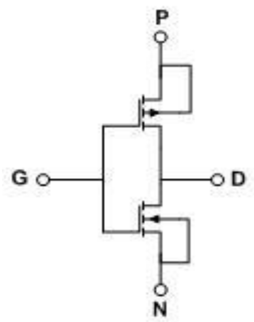


Fig. 2- GDI basic cell

Table I shows how a simple change of the input configuration of the simple GDI cell corresponds to very different Boolean functions. Most of these functions are complex (6-12 transistors) in CMOS, as well as in standard PTL implementations, but very simple (only 2 transistors per function) in GDI design method.

Table I: Some logic functions that can be implemented with a single GDI cell

| N | P | G | D |
|---|---|---|---|
| '0' | B | A | A'B |
| B | '1' | A | A'+B |
| '1' | B | A | A+B |
| B | '0' | A | AB |
| C | B | A | A'B+AC |
| '0' | '1' | A | A' |

XOR and XNOR functions are the key variables in adder equations. If the generation of them is optimized, this could greatly enhance the performance of the full adder cell. In this new cell has used the GDI technique for generating of XOR and XNOR functions. It uses only eight transistors to generate the balanced XOR and XNOR functions, as shown in figure 3.

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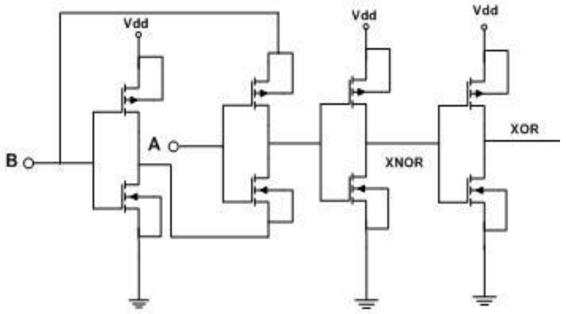


Fig. 3- XOR/XNOR cell with the GDI technique

A one-bit binary full adder takes three one-bit inputs: A, B and Cin and generate sum and carry.

Sum=( A ⊕ B) ⊕ Cin)
Carry= A. B + Cin ( A ⊕ B)

The goal of this paper is to design a high performance and low power full adder cell with the GDI technique.

The full adder cell has the 24 transistors that is shown in figure.5. In the first stage of this cell, the GDI technique is used for generating of XOR and XNOR functions. This stage shows full swing with low voltage. These complementary outputs, together with other inputs, will be fed to the second stage. The Sum and Carry outputs are generated from the second stage. Since adder cells are normally cascaded to form a usual arithmetic circuit and their capabilities must be ensured.

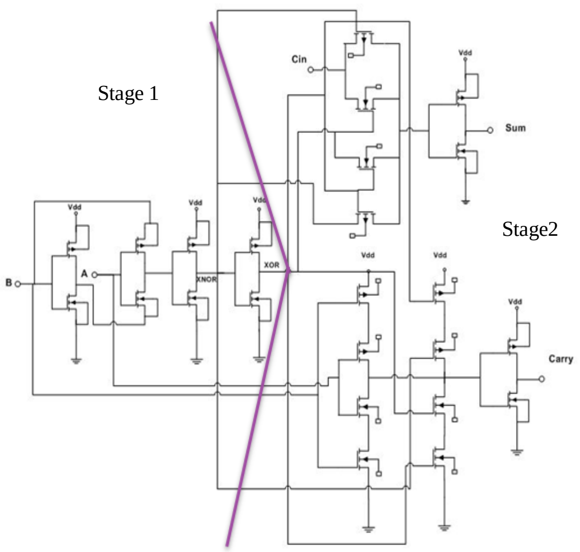


Fig. 4- The proposed full adder cell with GDI technique

## IV. SIMULATION RESULTS

The full adder operates in 100 MHz range. In fact, in addition to normal transistors, circuits are tested in corner cases with fast and slow transistors and their combinations too. In each stage one of the components FF, SS, FS, SF is replaced instead of normal transistors in circuit and is perused in each circuit function. The difference in this stage is in consumption power and falling and rising times so this subject looks simple due to the difference in NMOS and PMOS transistors speed .After the simulation, the layout of circuit is drawn. By the post simulation result along with a few corrections have achieved in sizes that the circuit has an accurate operation. Simulation results are performed by HSPISE based on 0.18µm CMOS technology. The power supply is 1.8v. The 5% variation of power supply is tested. This design is also compatible with transistor size 10% variation. In the table II, comparison of similar works and their results have been there. The snapshot of the waveforms at 1.8v is shown in figure 5.

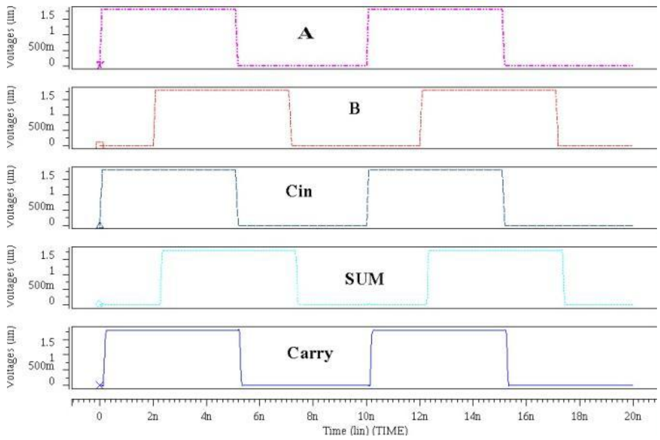


Fig.5- Snapshots of waveforms at 1.8v and 100MHZ

Table.2 comparison of similar works (Power, Delay and Power-Delay-Product)

| Structure | No. Transistors | Power (µw) | Delay (ns) | PDP (aj) |
|---|---|---|---|---|
| 10T | 10 | 1.13 | 73.5 | 83.05 |
| 14T | 14 | 6.4 | - | - |
| CPL | 18 | 2.5 | 141.1 | 352.7 |
| TFA | 16 | 12 | - | - |
| TGA | 20 | - | 342 | - |
| $C^2$MOS | 28 | - | 364 | - |
| HYBRID | 26 | 2.22 | 80.6 | 178.9 |
| FA24T | 24 | 1.66 | 137.9 | 228.91 |
| BRIDGE | 26 | 1.66 | 104.2 | 172.97 |
| N-CELL | 14 | 1.62 | 63.2 | 102.3 |
| DPL | 24 | 2.35 | 75.3 | 176.95 |
| MOD2F | 26 | 2.23 | 87.7 | 195.57 |
| HPSC | 22 | 0.25 | 141 | 35.25 |
| TSAC | 26 | - | 128 | - |
| This Work | 24 | 0.78 | 50 | 39 |

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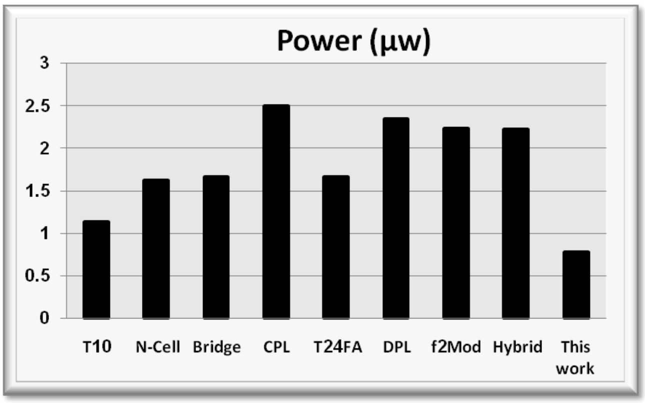


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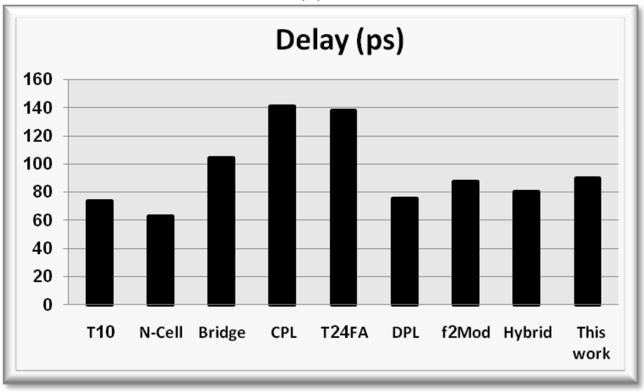


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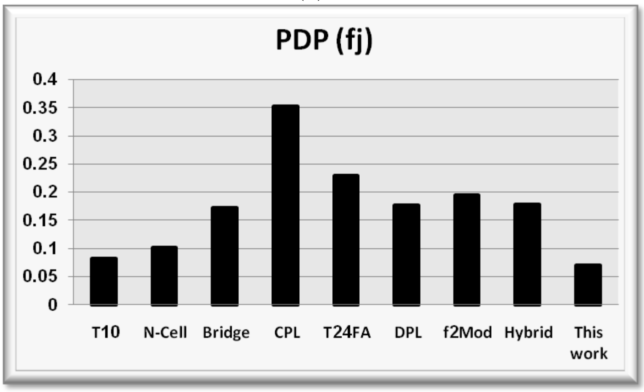


(c)

Fig. 6- comparison of (a) power, (b) delay and (c) PDP

## V. CONCLUSION

The aim of this work is two have been power reduction and speed increase in the full adder. In this operation the GDI technique was introduced. By using techniques such as size optimizing in full adder could reduce the power consumption. As a result, the full adder works at the 100 MHz speed with 0.78 $\mu$w power consumption. These results were obtained with spice simulation from the extracted net list of the layouts for normal parameters, room temperature and power supply at 1.8v.

The power was improved by 30% comparing to the 10T, by 65% to the Hybrid, by 53% to the Bridge, by 52% to the N-Cell and by 65% to the Mod2f.

The power delay product was improved by 53% comparing to the 10T, by 78% to the Hybrid, by 77% to the Bridge, by 61% to the N-Cell and by 80% to the Mod2f.

The power, delay and power product delay and PDP were improved. The result of this work and others are shown in figure 6.

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