A Tool Independent Improvement of IBIS Simulation on SSN

Boyuan Zhou, Lixin Yu, Junjian Chu

***Abstract*—The IBIS (Input/output Buffer Information Specification) is widely adopted in signal integrity (SI) analysis of high speed PCB system. This paper presents a novel approach to improving the accuracy of IBIS simulation by taking a feedback circuit that is usually absent in normal IBIS simulation into consideration. The improved simulation results compared with transistor-level simulation validate the efficiency of the proposed approach.**

***Index terms*—SI(Signal Integrity), behavior simulation, IBIS model, SSN (Simultaneous Switching Noise)**

I. INTRODUCTION:

With various advantages in fast, accuracy simulation and IP protection, IBIS (Input/output Buffer Information Specification) is qualified as the industry standard[2] (EIA standard 656-A) in modeling all kinds of I/O buffers, which is applied to modeling an entire IC device in behavior, as well as in board level simulation. With the ever growing popularity of IBIS, more thorough and detailed analysis and research [1] [3] are required to improve the simulation accuracy and to explore more available applications of the tool.

The IBIS model describes the buffer's behavior with curves such as pull-up and pull-down in terms of V-I, V-T tables as shown in figure 1. Since the simulation is independent of any specific circuit and does not reveal any circuit information, speediness and accuracy in simulation are guaranteed. As it's known the IBIS is lack in necessary information for SSN (Simultaneous Switching Noise), that limit the capability of IBIS using in the PI (Power Integrity) analyzing. Though the high version IBIS[4] contain SSN information is identified recently, it's take time to be capable in simulation tools. In this paper, a tool independent improvement of IBIS simulation is proposed, that enhance the accuracy of the IBIS simulation in SSN.

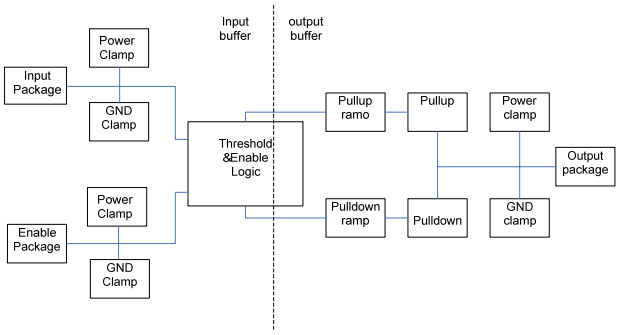

Figure 1. The IBIS structure. The left part express a typical input buffer structure, and a typical output buffer to the right

The remainder of this paper is organized as follows. The background of simulation approaches is presented in section 2. And Section 3 investigates how well the current IBIS can model the noise on nodes through an output buffer simulation. And then an approach to improving the simulation with results compared to transistor-level model and plain IBIS is introduced in detail in section 4. Finally in section 5 conclusions are drawn from the above sections and future work is discussed.

II. APPROACHES:

In this paper, all simulations are carried out on an embedded micro-processor core and an output buffer of the device is taken as an example.

In the very first step, the IBIS model of the entire device is transformed from the transistor-level model (SPICE) using S2IBIS tool[5]. High version of IBIS is not used, for it is not available in most common IBIS simulators.

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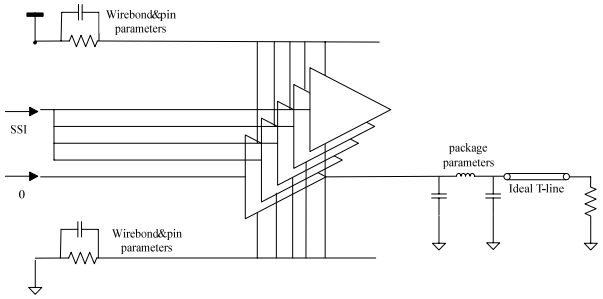

Figure 2. The SSN test net. The buffer could simulate with either SPICE model or IBIS model. RC nets are added as package parameters to the GND and POWER plane

The specific output buffer is picked out from the pin list because it is located in high speed data bus, and thereby most frequently used in the device.

And then the netlist is setup with the equivalent construct in Hspice to make simulation by transistor-level model and IBIS model-which is quoted as B-element in Hspice[6]. The construction is discussed and analyzed in the following section.

III. Comparing SPICE and IBIS:

The circuit in figure 2 is setup with 5 cascaded non-inverting voltage mode drivers. These 5 drivers share the same power-ground plane through RLC circuits that models the power-ground plane parasitics as well as pin-package parasitics. The drivers are connected to 50 ohm ideal transmission line and terminated with 50 ohms resistors. Simultaneous switching inputs are applied on 4 of the drivers and the other driver is grounded to act as a quiet line. After the circuit is built, the 5 drivers can then be simulated with transistor-level model or IBIS model.

The Hspice guidance[6] advises to distribute the C_comp (silicon die capacitance) into each node of the model, to get more accuracy of SSN simulation in power and ground. But the feature is not implemented in this paper for universality, since this feature is tool dependant, and not available in all IBIS simulators.

Simulate with the aforementioned setup, a significant noise is observed on the quiet line both in the SPICE and IBIS simulation. And IBIS simulation result demonstrates even higher noises than transistor-level model simulation in power, ground.

As it's shown from the simulation results, IBIS overestimates the SSN as it does not model the parasitic circuit known as 'feedback circuit'. The overestimation

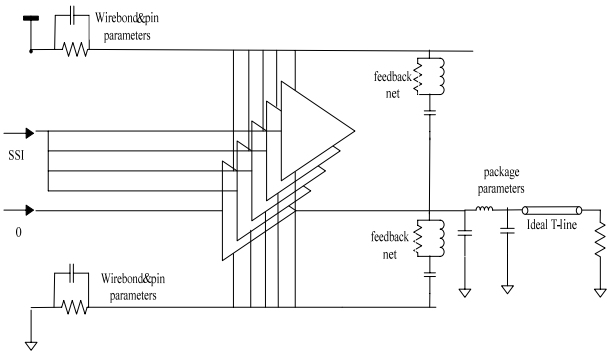

Figure 3. Add the feedback circuit into the SSN test net, feedback parameters calculated by simulation tool.

would shrink the designer's available options and limit the flexibility of design with IBIS[7].

To alleviate the noise problem, 'feedback' parts are introduced into the simulate circuit. Details are discussed in the following section.

IV. Improved Simulation with 'Feedback Effect' and Results Comparison:

Since the absence of 'feedback' circuit in simulation would result in the overestimation of the SSN. Measures to add equivalent RLC networks between POWER, GND and the output nodes as 'feedback' are taken as shown in figure 3.

The RLC parameters among GND, output node and POWER could be figured out simply, then the feed back circuit based on the parameters can be built. It should be noticed that in this paper, an optimum C parameter is selected from values are swept between 0.05 and 5uf.

All the simulation curves are shown in figure 4 to figure 9.

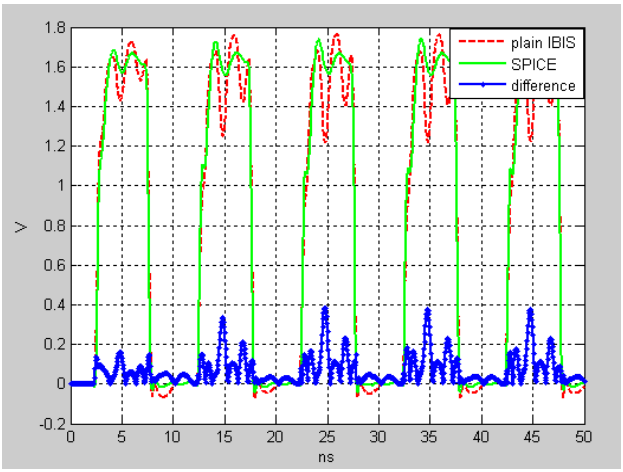

Figure 4. The output curves of SPICE model (solid) and plain IBIS model (dashed), and the difference between the two curves.

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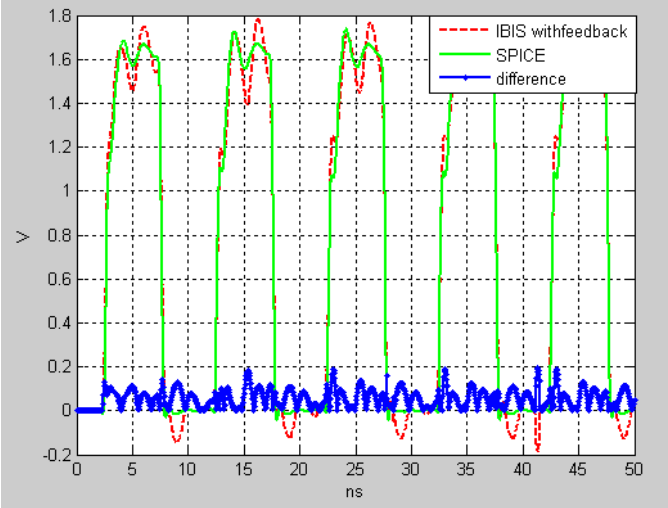


Figure 5. The output curves of SPICE model (solid) and IBIS model with feedback (dashed), and the difference between the two curves.

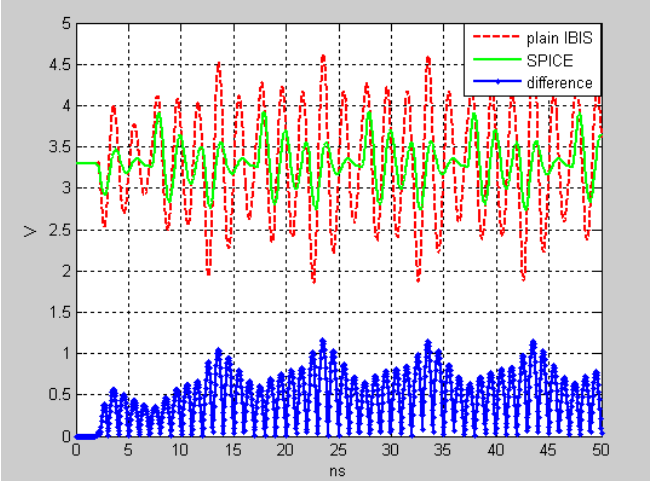


Figure 6. The noise curves in POWER of SPICE model (solid) and plain IBIS model (dashed), and the difference between.

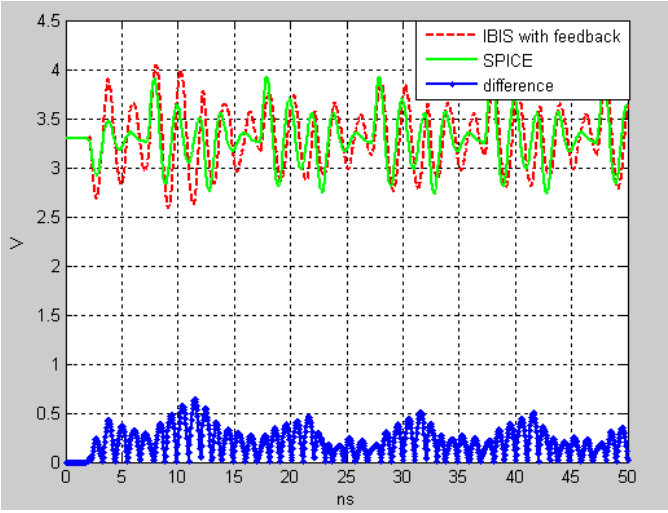
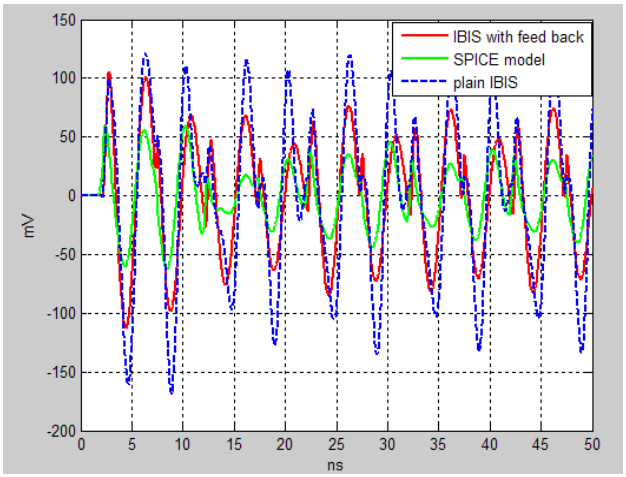


Figure 7. The noise curves in POWER of SPICE model (solid) and IBIS model with feedback (dashed), and the difference between.



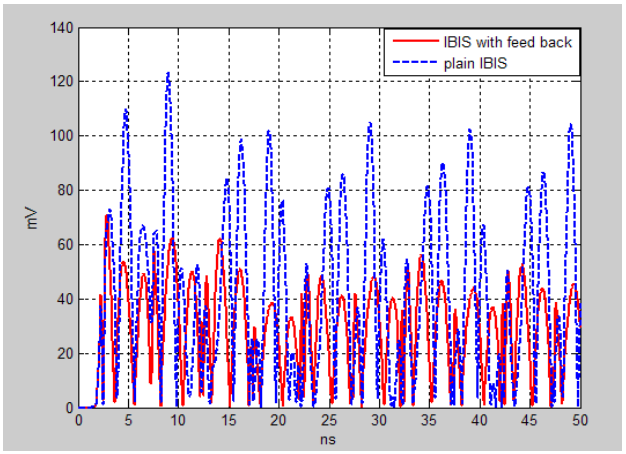


Figure 10. The noise in ground (up), the dashed blue curve is plain IBIS, and the solid red curve is enhanced IBIS with feedback, both compared with SPICE model. And the difference of the two IBIS curve compared to SPICE is below.

Matlab is used to analyze and compare the results. The improvement is estimated using mean square error in the formula (1) below.

$$MeanSquareError = \frac{1}{n}\sum_{i=1}^{n}\left(Y_{IBIS}(i) - Y_{tran}(i)\right)^2 \quad (1)$$

The comparison is listed in a table 1 for legibility. The result shows that the circuit with feedback has a lower mean square error than the circuit without it.

Table 1.simulate result comparison

Simulation result		Mean error	Percentage improvement in mean square error
Power	IBIS	46.63mV	42.14%
	enhanced	20.29mV	
GND	IBIS	41.05mV	37.95%
	enhanced	28.91mV	
Output	IBIS	69.45mV	48.07%
	enhanced	56.62mV	

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V. CONCLUSION AND FUTURE WORK:

As shown in this paper, more accurate results can be achieved by complementing the IBIS model with feedback information. With the noise on POWER plane of circuits compared to SPICE, circuit with feedback has a lower mean square error than circuit without it. And refer to the ground, a lower mean square error of 37.95%is achieved with feedback taken into account. And a lower mean square error of 42.14% in power. The decrease in output node error is 48.07%. The average improvement is close to 40-45%.

To obtain more accurate simulation result, various solutions have been proposed to improve simultaneous switching noise simulations with IBIS models [8]. A number of potential solutions are under investigation. Still, more effort needs to be made in the future. The research work in this paper is dedicated to resolve the problems encountered that are beyond the capability of the current tools. Measures have to be taken to alleviate the problems that IBIS tool lags behind the development of IBIS version. Hopefully we look forward to seeing the unified IBIS using and the options of adjusting detailed parameters in future IBIS tools.

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