A Precise Power Supply Noise Detector with High-Linearity

I-Chyn Wey, Chien-Chang Peng, Yu-Jiang Liao, and Yu-Sheng Yang

Abstract

In this paper, we proposed a noise detector with high linearity in CMOS 0.18um process. By removing the precharging capacitor, we can provide a stable charging voltage source to enhance power supply noise detection linearity from 0.9291 to 0.9986. By using separated supply voltage sources, we set the detection path with a higher supply voltage of 2.5V to turn on the detection circuitry immediately when supply voltage drops. In this way, the noise detection range can be enlarged and the noise detection accuracy is improved by 4.94 times.

Key Words: Precise, Power Supply Noise, Noise Detector, High Linearity.

I. Introduction

In recent years, due to the progress of CMOS technology, not only the transistor size is scaled down, the supply voltage is also lowered as well as threshold voltage. Lowering power supply voltage leads to lower power consumption; however, noise does not decrease while the supply voltage is downward. To solve the noise issues in VLSI designs, we must first detect the behavior, distribution, and size of noise to build the understanding of noise interference. The type of noise can be classified as switching impulse noise, power supply noise (PSN), and substrate noise [1], [2]. For different noise sources, we must apply different techniques to detect them [1]-[10]. In this paper, we focus our attention on PSN detection.

Nowadays there are some built-in noise detection circuits [3]-[6] that have been proposed to measure the distribution of noise signals in a VLSI chip. High linearity and high precision are two design goals in PSN detection circuits design. The built-in self noise detection circuits in [3], [4] are constructed by a source follower and a transconductance amplifier. These designs can detect the noise in real time.

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However, the detection results translated from transconductance amplifier are non-linear. As for the concurrent power supply noise detection technique [5], it can provide an output error message upon the occurrence of power supply noise. However, it only shows the noise is detected or not detected, we cannot get the detail noise information. For the power supply noise monitoring circuit [6], the detected signals are analog signals, which can reveal the detected noise voltage peak values. Nevertheless, the noise detection range is limited because the noise amplitude peak value cannot be detected before the charging transistor is turned on. In addition, the detected PSN signal is affected by the variance of charging voltage, which leads to non-linear PSN detection results.

To remove the unstable charging voltage source in [6], we remove the precharging capacitor Cr and charge the capacitor Cx by using an independent power supply with higher supply voltage of 2.5V. By this way, the output dynamic range is enlarged to 4.04 times and the detection accuracy can be enhanced by 4.94 times.

II. The Existing PSN Detection Circuits

Built-in power supply noise detecting circuit [3]-[4], consists of a source follower (SF) that senses power supply noise voltage and a transconductance amplifier (Gm) that converts the SF's output voltage to current signal Iout. The detected PSN can be directly observed through Iout. The benefit of built-in detecting circuit lies in its small size, real-time output and the detected noise voltage or current value that can be observed directly. However, the detection results translated from transconductance amplifier and source follower are non-linear.

Concurrent power supply noise detection technique [5] is designed based on a self-checking scheme which concurrently monitors a signal of the system clock distribution network. It can provide an output error message upon the occurrence of power supply noise. The benefit of concurrent detecting method lies in its digital output, which is hardly interfered by noise. But we can only know the scope of noise rather than its accurate value.

The power supply monitoring circuit [6] is to measure the power supply noise through its effect on the propagation delay of an inverter chain. The total charge flow to Cx is proportional to the propagation delay of the inverter chain. While the propagation delay of the inverter chain is proportional to the supply voltage, and the supply voltage is

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affected by the PSN. In other words, the larger voltage peak of PSN, the longer delay time in the inverter chain; therefore, the charging time of Cx is longer, and the output of Vx is higher and vice versa.

In the previous noise detection circuit designs, the detection results in the built-in detecting circuits are non-linear. The concurrent power supply noise detection technique can only reveal digital output instead of the peak value of noise. The monitoring circuit can provide analog outputs, which can be measured in different sizes of Vx, so that it can identify the peak value of noise. Alternatively, our proposed precise power supply noise detection circuit design is based on monitoring circuit but with higher linearity and higher precision.

III. The Proposed PSN Detection Circuit

Maintaining the relationship between the PSN detector output and the input PSN as linear is a direct and effective way to precise detect the noise amplitude. However, the noise detection range is limited in the power supply monitoring circuit [6]. Moreover, the PSN detection precision is restricted in [6] because the graduation in the delta Vx is small. Therefore, we must enlarge the voltage difference of delta Vx to enhance PSN detection accuracy.

As mentioned above, the charging voltage of Cx in the power supply monitoring circuit is determined by the charging voltage across the capacitor of Cr. Once PSN occurs, the voltage across Cr will change along with various noise amplitudes, as illustrated in Fig. 1. In the PSN monitoring circuit [6], the variance of Vr results from the power supply noise dropping. Such voltage variance on Vr results in non-linearity on the variance of Vx. In order to provide a stable voltage source for charging Cx, we remove the capacitor by directly connecting to the separated supply voltage to achieve higher linearity in the detection output. To enlarge the linear detection range, we apply a higher voltage of 2.5V to this separated supply voltage to let the transistor MP3 can be turned on immediately once PSN occurs. In this way, the detected △Vx can be enlarged and the PSN detection linearity can be improved.

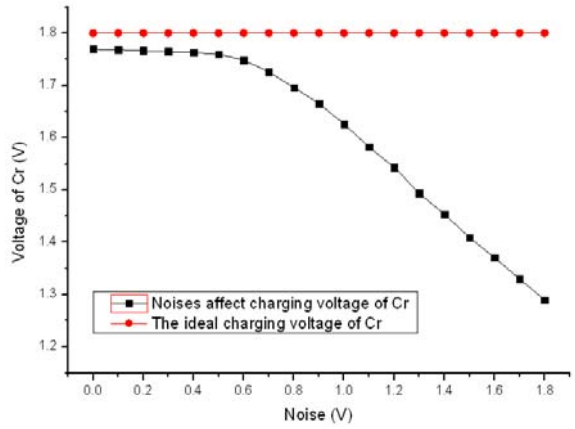

Fig. 1 The analysis of charging voltage variation of Cr along with various PSN amplitudes

For the proposed PSN detection circuit as shown in Fig. 2, MP1 and Cr are removed and replaced by an independent power supply directly to the charging capacitor Cx. The proposed circuit operates in the following way: as the CTRL/CLK is logic low, the transistor MN1 is turned on, the capacitor Cx is discharging, and the transistor MP3 is turned off. While CLK is logic high as 1.8V, MN1 is open and Cx stops discharging. Due to the inverter delay line, MP2 and MP3 will both be turned on with a short period of time. Meanwhile, the Cx is recharged by VDDH, and the period of time is up to the delay time of the inverter chain.

In our proposed PSN detection circuit, VDDH is independent from original power supply VDD. In this way, we can provide a stable voltage source for charging Cx, which can enhance the detection linearity. We can also separately adjust the value of VDDH and the capacitance value of Cx to enhance the linearity of detected output. Moreover, VDDH is set to be higher than VDD to turn on the transistor MP2 and MP3 once the supply voltage drops. Moreover, the PSN detected output dynamic range, delta Vx, can be also greatly enlarged. Therefore, the noise detection accuracy can be improved.

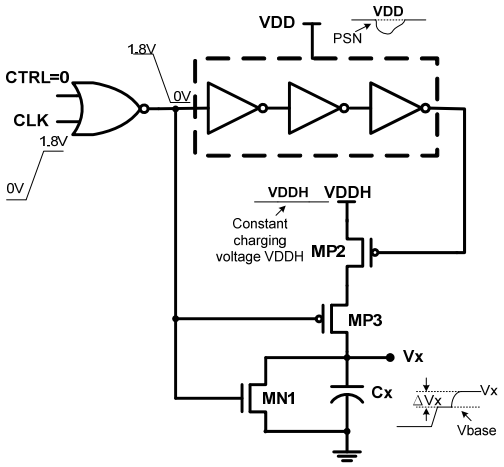

Fig. 2 The proposed power supply noise detection circuit

IV. Simulation Comparison Results

In this paper, the proposed precise and high linearity PSN detector is accomplished by a stable and independent charging voltage source. Connecting the transistor MP2 to a separated charging path even with the same supply voltage as 1.8V, we can also improve the detection range with wider Vx variation range as illustrated in Fig. 3. It is mainly because that we can overcome the charging voltage instability issue existing in [6]. As illustrated in Fig. 3, the slope of curve in the proposed PSN detector is steeper than that of conventional one. The average output value can be enlarged to 30.55mV, which is about 2 times larger as compared with the conventional design.

In order to further detect the noise below 0.5V, we raise the supply voltage value of VDDH to improve the output dynamic range. It is illustrated in Fig. 4 that the higher VDDH can result in the more linear PSN detection.

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However, when the charging voltage increases, the delta Vx will reach saturation and the linearity of PSN detection can no more be held. To find out the highest PSN detection linearity, we compare the PSN detection linearity among different charging supply voltages. To evaluate the detection linearity of PSN detector, we define the relevance between the ideal expected PSN value and the real detected PSN value as PSN detection linearity, which is defined as

$$\text{Relevance (r)} = \frac{\sum_{i=1}^{n}\left(x_i-\bar{x}\right)\cdot\left(y_i-\bar{y}\right)}{\sqrt{\sum_{i=1}^{n}\left(x_i-\bar{x}\right)^2\cdot\sum_{i=1}^{n}\left(y_i-\bar{y}\right)^2}} \quad (1)$$

As illustrated in Fig. 4, we can achieve a higher PSN detection linearity of 0.9986 by selecting the maximum charging voltage of 2.5V. As a result, the VDDH value is set as 2.5V to acquire the higher PSN detection linearity. The size of output capacitor also affects the PSN detection linearity. Based on the analytical results, we select the capacitance of 0.4pF as the output capacitor with the PSN detection linearity of 0.9986. As a result, the PSN can be read clearly with 4.04 times larger average detected PSN voltage difference as compared with the conventional design in [6], as shown in Fig. 5. The linearity can also be enhanced from 0.9291 to 0.9986.

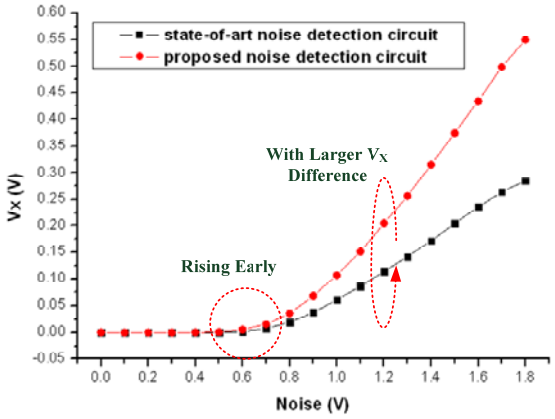

Fig. 3 Comparison of Vx variation under various power supply noise pulse amplitude in the proposed PSN detection circuit versus the state-of-art PSN detector in [6]

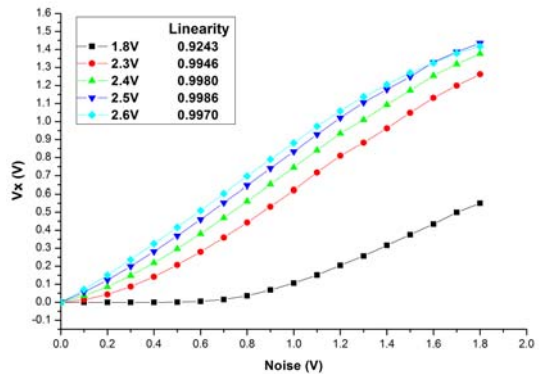

Fig. 4 Analysis of various charging supply voltage for higher PSN detection linearity

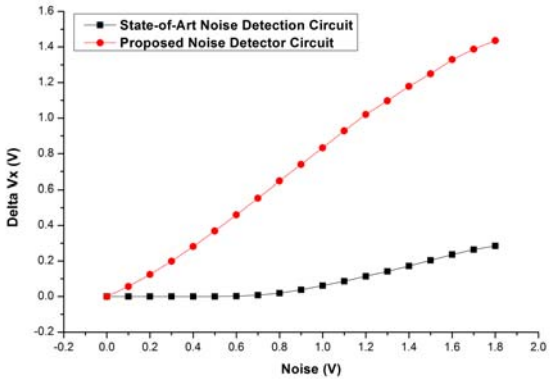

Fig. 5 Comparison of detected output voltage difference in the state-of-art PSN detector in [6] and the proposed PSN detector

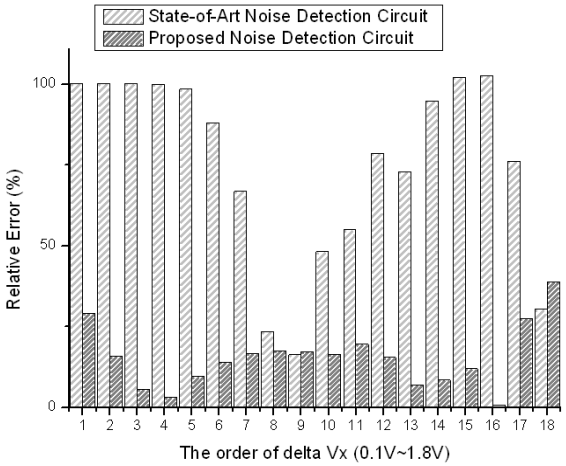

Fig. 6 Comparison of PSN detection error in the state-of-art PSN detector in [6] and the proposed PSN detector

To evaluate the PSN detection accuracy, we define the PSN detection error as:

$$\text{Detection Error} = \left|\frac{V_X-\overline{V_X}}{\overline{V_x}}\right|\times 100\% \quad (2)$$

As illustrated in Fig. 6, the PSN detection resolution in [6] is limited to around 100mV and the average PSN detection error is 75.265%. Under the case with 100mV PSN detection resolution, the PSN detection error can be lowered to 15.246 % in our proposed PSN detection circuit. The reason that makes our improvement effective is that we successfully raise the charging voltage to enhance the PSN detection range and provide an independent stable charging path to improve PSN detection linearity.

To evaluate the PSN detection performance, we summarize the comparison results in Table 1. In the proposed PSN detector, the PSN detection linearity can be improved from 0.9291 to 0.9986 in terms of relevance. The detected output variance can be enlarged from 15.82mV to 79.75mV. Therefore, the output dynamic range can be enlarged to 4.04 times. Moreover, the PSN detection error can also be reduced from 75.27% to 15.25%. As a result, the noise detection accuracy can be improved by 4.94 times.

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In order to verify the function and performance in silicon, we layout the proposed design in TSMC 0.18μm process as shown in Fig. 7. The silicon area of PSN detector circuit is 15.93μm*45.93μm, which is dominated by the capacitor. By removing one capacitor, Cr, we can save about 40% silicon area. The PSN detection performance is nearly the same before and after the silicon layout.

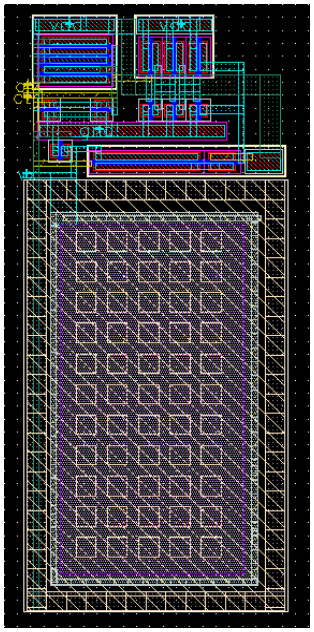

Fig. 7 Chip layout of the proposed PSN detector

Table1 Comparison of PSN detection performance

	State-of-Art PSN Detector in [6]	Proposed PSN Detector
Transistor Count	**14**	**13**
Capacitor	**2**	**1**
Linearity (Relevance)	**0.9291**	**0.9986**
Detected Variance (per 100 mV PSN)	**15.82mV**	**79.75mV**
Detection Error	**75.27%**	**15.25%**

V. Conclusion

In this paper, we proposed a noise detector with high PSN detection precision and high linearity in CMOS 0.18μm process. The silicon area of the proposed PSN detector circuit is 15.93μm*45.93μm, which saves 40% as compared with the PSN detector in [6]. By replacing the precharging capacitor with a independent 2.5V supply voltage, the PSN detection linearity can be enhanced from 0.9291 to 0.9986, the output dynamic range can be enlarged to 4.04 times, and the noise detection accuracy can be improved by 4.94 times.

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