Active-Harmonic-Elimination-Based Switched-Capacitor Boost DC-AC Inverter

Yuen-Haw Chang and Shin-Cheng Chen

***Abstract*—A closed-loop scheme of 9-level switched-capacitor (SC) boost DC-AC inverter is proposed by combining active-harmonic-elimination (AHE) approach for a staircase DC-AC conversion and regulation. In this 9-level SC inverter, there are 3 pumping capacitors between supply source and output terminals in order to realize the maximum boosting gain of 4 at most, and also to obtain the inverted gain of 4 with the help of bidirectional switches employed here. For achieving a staircase AC output, these bidirectional switches are controlled with the driver signals from the clock generator so as to boost/invert the output up to 1x, 2x, 3x, or 4x voltage of supply source. In this paper, an AHE approach is suggested and used for the consideration of the 3rd, 5th, 7th harmonic elimination not only to control the time intervals of the different output levels of 1x, 2x, 3x, 4x, but also to enhance the output regulation capability for the different desired outputs. Finally, this 9-level SC boost inverter is designed and simulated by OrCAD, and all the results are illustrated to show the efficacy of the proposed scheme.**

***Index Terms*—switched-capacitor, boost DC-AC inverter, bidirectional switches, active-harmonic-elimination**

I. Introduction

With the popularity of portable electronic equipments (e.g. notebook, digital camera, PDA), people always ask for the power modules of these products possessing the merits of smaller volume, lighter weight, higher efficiency, and better regulation capability. General speaking, the traditional power converters (e.g. DC-DC or DC-AC) have a big volume and a heavy weight because of magnetic devices. So, more manufactures and researchers pay much attention to this topic, and ultimately, requiring DC-DC or DC-AC converters realized on a compact chip by mixed-mode VLSI technology.

The SC-based power converter, based on charge pump scheme, is one of good solutions to power conversion because it contains capacitors and semi-conductor switches only. Unlike traditional converters, SC converters require no inductive element, so they are suitable for many applications, e.g. drivers of electromagnetic luminescent (EL) lamp, white light emitting diode (WLED). In 1990, the first SC step-down converters were proposed by Japan researchers [1], and their idea is to switch MOSFETS cyclically according to 4 periods of capacitors charging/discharging for step-down conversion. In 1993, Cheong et al. suggested a modified SC converter with two symmetry SC cells working in the two periods [2]. Then, combining with pulse-width-modulation (PWM) technique, they proposed a new step-up DC-DC converter by using duty-cycle control [3]. In 1994, Ngo et al. first proposed a current control of SC converters by using a saturated transistor as a controllable current source [4]. In 1996, Chung and Ioinovici suggested a current-mode SC for improving current waveforms [5]. Following this idea, Chang proposed an integrated SC step-up/down DC-DC/DC-AC converter [6-7].

In this paper, by using the AHE control, a closed-loop boost DC-AC inverter is realized not only to reduce total harmonic distortion (THD), but also enhance output regulation for different desired output.

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II. Configuration Boost DC-AC Inverter

Fig.1 shows the configuration of 9-level SC boost DC-AC inverter, and it has two main parts: power part and control part. The discussions are as follows.

A. Power Part — 9-Level SC Boost Inverter

The 9-level SC boost inverter as in the upper of Fig.1 is composed of 14 bidirectional switches devices (S1-S14), 3 pumping capacitor (C1-C3) and output capacitor Co between supply sources Vs1, Vs2 (Vs1=Vs2=Vs), and output Vout, where each capacitor has the same capacitance C (C1=C2=C3=C). The main function of this power part is to boost Vout up to 1x, 2x, 3x, 4x of Vs1 in positive half-wave, or to 1x, 2x, 3x, 4x of Vs2 in negative half-wave. Thus, this part can provide 9-level output values of Vout for realizing a staircase AC output. These 9-level operations are explained as follows.

1) Positive Half-Wave (PHW):
   a) Phase I:
      S1, S2, S3, S4, S9, S10, S11 turn on, and S5, S6, S7, S8, S12, S13, S14 turn off. The relevant topology is shown Fig.2 (a). Capacitors C1, C2, C3 are charged to Vs1.
   b) Phase II:
      In order to obtain the different voltage gains (1x, 2x, 3x, 4x), the different phase II operations (switches and topologies) are considered below.
      (1) 1x:
         S1, S5, S6, S7, S13 turn on, and S2, S3, S4, S8, S9, S10, S11, S12, S14 turn off. The current flow is passing from Vs1 through S1, S13 to output

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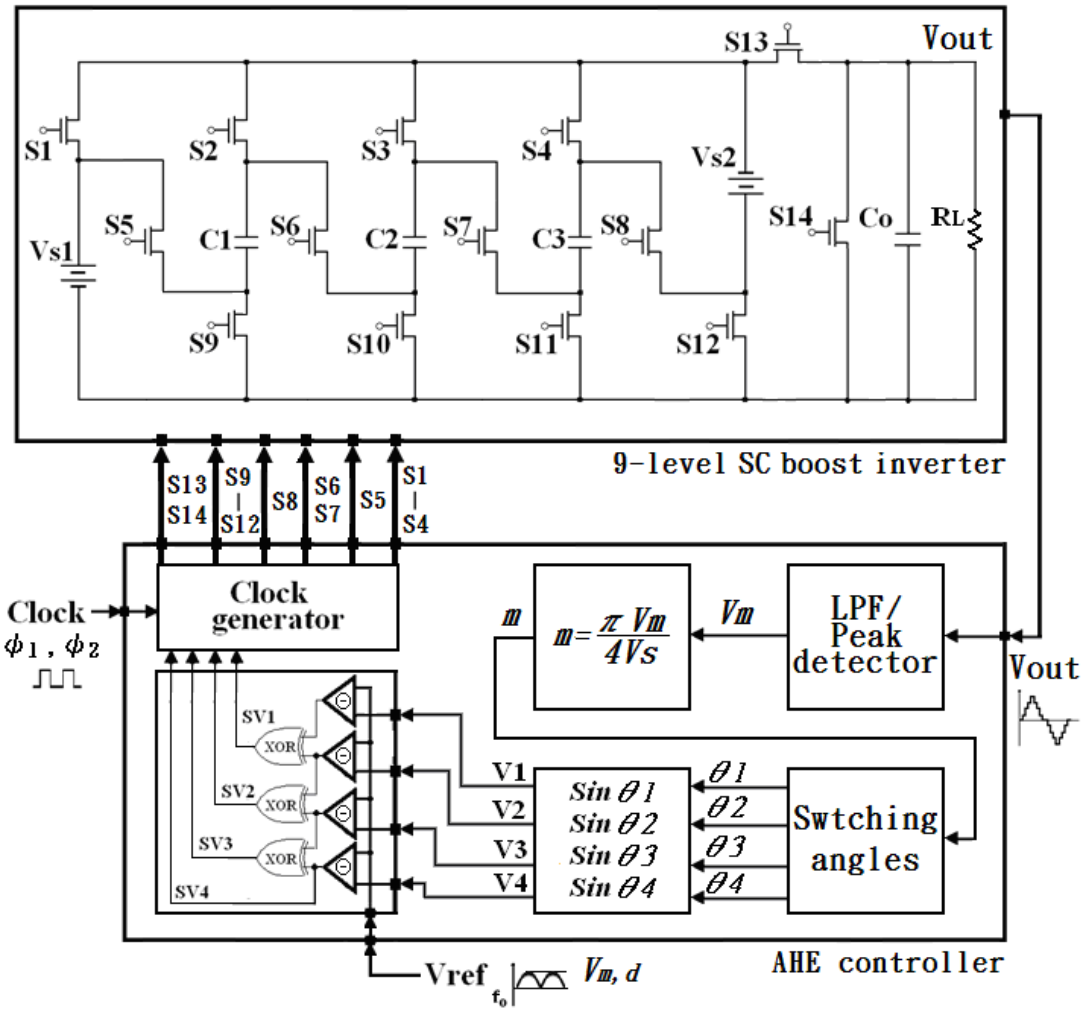

Fig.1. Configuration of SC boost DC-AC inverter.

terminal as symbol "— — — — " in Fig.2 (b).

(2) 2x:

S2, S5, S6, S7, S13 turn on, and S1, S3, S4, S8, S9, S10, S11, S12, S14 turn off. The current flow is passing via Vs1 and C1 in series connection through S2, S5, S13 to output terminal as shown symbol "— • — • —" in Fig.2 (b). So, the 2x function can be obtained with the help of Vs1 and C1 in series.

(3) 3x:

S3, S5, S6, S7, S13 turn on, and S1, S2, S4, S8, S9, S10, S11, S12, S14 turn off. The current flow is passing via Vs1, C1 and C2 in series connection through S3, S5, S6, S13 to output terminal as shown symbol "—x—x—" in Fig.2 (b). So, the 3x function can be obtained with the help of Vs1, C1 and C2 in series.

(4) 4x:

S4, S5, S6, S7, S13 turn on, and S1, S2, S3, S8, S9, S10, S11, S12, S14 turn off. The current flow is passing via Vs1, C1, C2 and C3 in series connection through S4, S5, S6, S7, S13 to output terminal as shown symbol "———" in Fig.2 (b). So, the 4x function can be obtained with the help of Vs1, C1, C2 and C3 in series.

2) Negative Half-Wave (NHW):

a) Phase I:

S2, S3, S4, S9, S10, S11, S12 turn on, and S1, S5, S6, S7, S8, S13, S14 turn off. The relevant topology is shown Fig.2 (c), Capacitors C1, C2, C3 are charged to Vs2.

b) Phase II:

In order to obtain the different voltage gains (1x, 2x, 3x, 4x), the different phase II operations (switches and topologies) are considered below.

(1) 1x:

S6, S7, S8, S12, S13 turn on, and S1, S2, S3, S4, S5, S9, S10, S11, S14 turn off. The current flow is passing from Vs2 through S12, S13 to output terminal as shown symbol "— — — — " in Fig.2 (d).

(2) 2x:

S6, S7, S8, S11, S13 turn on, and S1, S2, S3, S4, S5, S9, S10, S12, S14 turn off. The current flow is passing via Vs2 and C3 in series connection through S8, S11, S13 to output terminal as shown symbol "— • — • —" in Fig.2 (d). So, the 2x function can be obtained with the help of Vs2 and C3 in series.

(3) 3x:

S6, S7, S8, S10, S13 turn on, and S1, S2, S3, S4, S5, S9, S11, S12, S14 turn off. The current flow is passing via Vs2, C2 and C3 in series connection through S7, S8, S10, S13 to output terminal as shown symbol "—x—x—" in Fig.2

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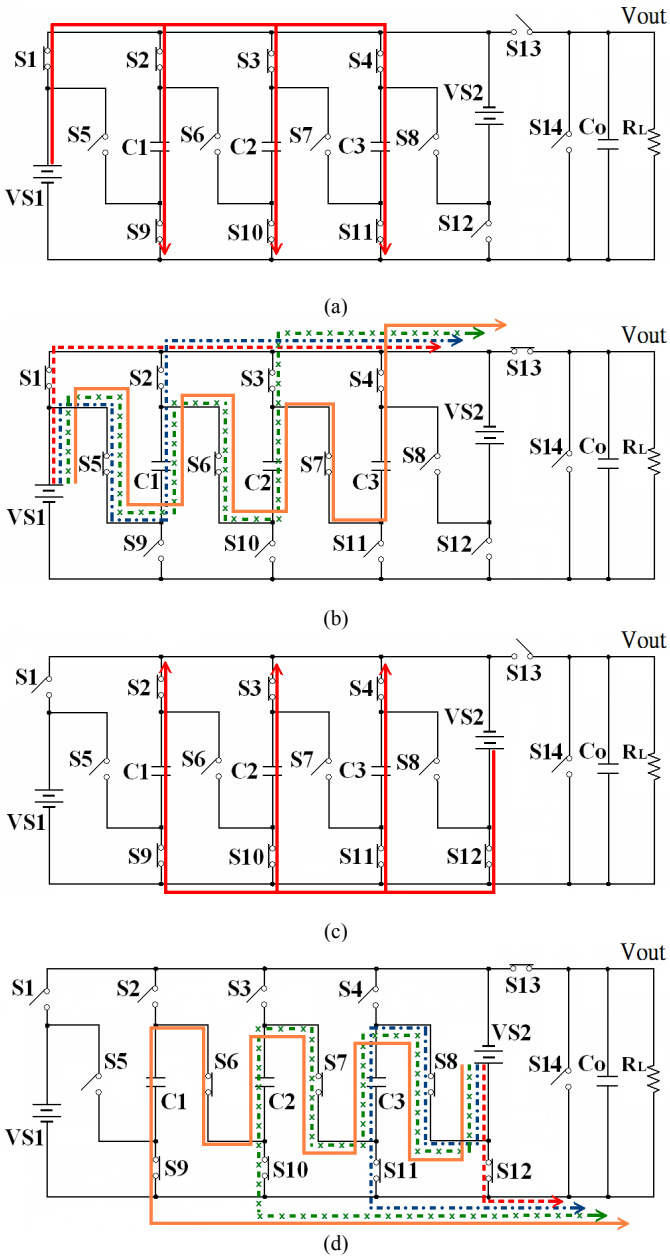

Fig. 2. (a) Phase I topology in PHW (b) Phase II topology in PHW (c) Phase I topology in NHW (d) Phase II topology in NHW.

(d). So, the 3x function can be obtained with the help of Vs2, C2 and C3 in series.

(4) 4x:

S6, S7, S8, S9, S13 turn on, and S1, S2, S3, S4, S5, S10, S11, S12, S14 turn off. The current flow is passing via Vs2, C1, C2 and C3 in series connection through S6, S7, S8, S9, S13 to output terminal as shown symbol "———" in Fig.2 (d). So, the 4x function can be obtained with the help of Vs2, C1, C2 and C3 in series.

3) Zero crossing:

In phase I and II, S1-S13 torn off, and only S14 turn on for a zero output.

According to the above descriptions, the theoretical waveforms of these switches and AC output are shown in Fig.3. As S1 shown in Fig.3, the output value of 1Vs in PHW/NHW is running within the interval of S1 turned on both in phase I and II, as denoted by T_1. The output value of 2Vs in PHW/NHW is within the interval of S2 on both in

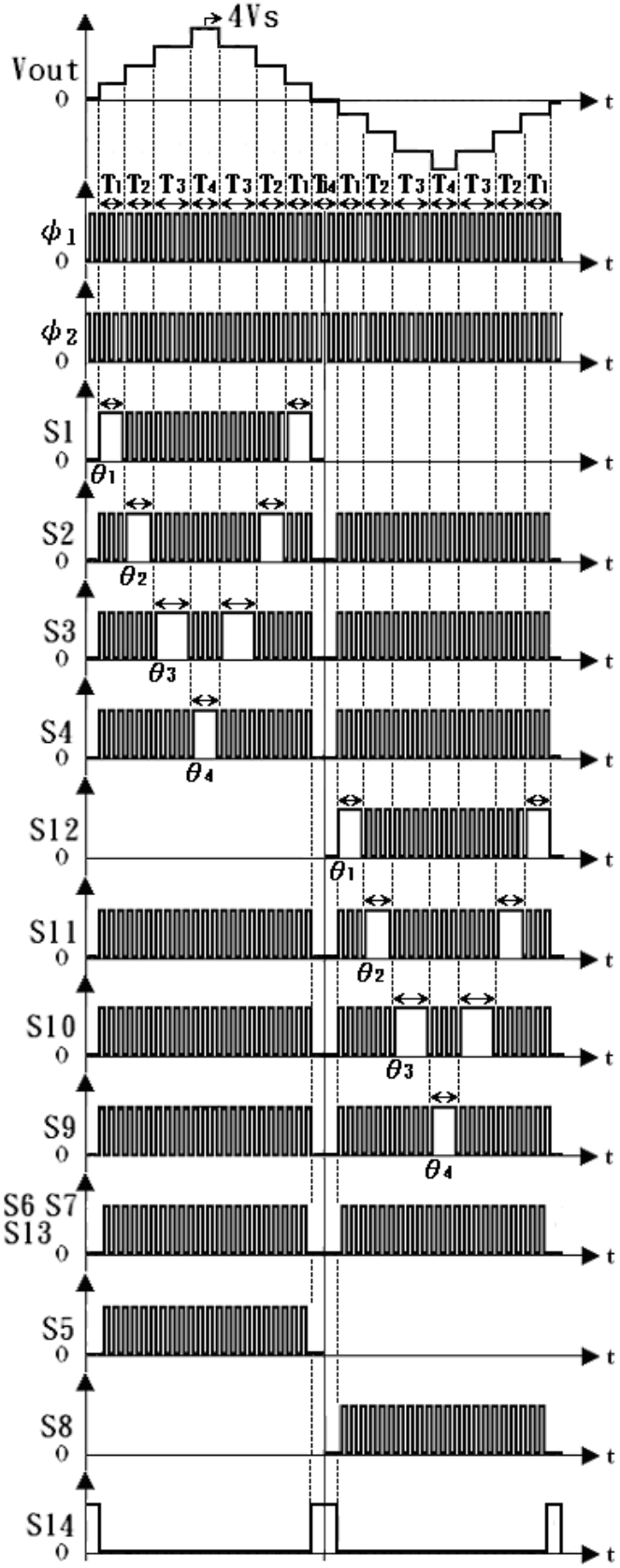

Fig.3. Theoretical waveforms of DC-AC booster.

phase I and II as T_2. Similarly, the output value of 0Vs is controlled for zero-crossing by S14 as interval T_{14}. So, the values of T_1, T_2, T_3, T_4, and T_{14} determine/control how long the time interval of 1Vs, 2Vs, 3Vs, 4Vs and 0Vs are. In this paper, we use the AHE approach to form a controller for a set of suitable values of T_1, T_2, T_3, T_4 and T_{14}. The main goal is to obtain a staircase AC output waveform for a better THD.

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B. Controller Part — AHE Controller

As the controller shown in Fig.1, first, Vout is sent into the low-pass filter (LPF) for high frequency noise reduction, and is detected to obtain its amplitude *Vm*. Based on this *Vm*, the modulation index *m* is computed via $m=\pi Vm/4Vs$ [8]. Next, by using this index *m*, the angles θ_1, θ_2, θ_3 and θ_4, are determined through the rule table of switching angles, where θ_1, θ_2, θ_3, θ_4, are the exciting angles of S1, S2, S3, S4 respectively. This rule table is designed for the elimination of the 3rd, 5th, 7th harmonics, and the relevant harmonic-elimination equations are shown as follow [8]:

$$\begin{cases} \cos(\theta_1)+\cos(\theta_2)+\cos(\theta_3)+\cos(\theta_4)=m, \\ \cos(3\theta_1)+\cos(3\theta_2)+\cos(3\theta_3)+\cos(3\theta_4)=0, \\ \cos(5\theta_1)+\cos(5\theta_2)+\cos(5\theta_3)+\cos(5\theta_4)=0, \\ \cos(7\theta_1)+\cos(7\theta_2)+\cos(7\theta_3)+\cos(7\theta_4)=0. \end{cases} \quad (1)$$

Next, the exciting levels: V1, V2, V3, V4 can be computed based on $V1=\sin\theta_1$, $V2=\sin\theta_2$, $V3=\sin\theta_3$, $V4=\sin\theta_4$ as in Fig.4. Then V1, V2, V3, V4 are compared with full-wave rectified sinusoidal V_{ref}, and through exclusive operation (XOR gates), the basic control signals SV1, SV2, SV3, SV4 can be obtained for the control of T_1, T_2, T_3, T_4. Equation (2) shows the detailed computations of SV1, SV2, SV3, SV4.

$$\begin{aligned} SV1 &= (V1 \ominus V_{ref}) \oplus (V2 \ominus V_{ref}), \\ SV2 &= (V2 \ominus V_{ref}) \oplus (V3 \ominus V_{ref}), \\ SV3 &= (V3 \ominus V_{ref}) \oplus (V4 \ominus V_{ref}), \\ SV4 &= (V4 \ominus V_{ref}), \end{aligned} \quad (2)$$

$$\text{where } a \ominus b = \begin{cases} 0, a \ge b, \\ b-a, a < b. \end{cases}$$

In Fig.4, it is obvious that SV1 has 4 time slots with the interval T_1, SV2 has 4 time slots of T_2, SV3 also has 4 slots of T_3, and SV4 has 2 slots of T_4. According to SV1, SV2, SV3, SV4, ϕ_1 and ϕ_2, all the truing-control signals S1-S14 are generated via the clock generator with the detailed Boolean relationships as follows: ("•": logic AND, "+": logic OR, "′": logic NOT).

$$\begin{aligned} S1 &= ((SV1+\phi_1)\cdot S^+)\cdot(V1 \ominus V_{ref}), \\ S12 &= ((SV1+\phi_1)\cdot S^-)\cdot(V1 \ominus V_{ref}), \\ S2 &= ((SV2\cdot S^+)+\phi_1)\cdot(V1 \ominus V_{ref}), \\ S11 &= ((SV2\cdot S^-)+\phi_1)\cdot(V1 \ominus V_{ref}), \\ S3 &= ((SV3\cdot S^+)+\phi_1)\cdot(V1 \ominus V_{ref}), \\ S10 &= ((SV3\cdot S^-)+\phi_1)\cdot(V1 \ominus V_{ref}), \\ S4 &= ((SV4\cdot S^+)+\phi_1)\cdot(V1 \ominus V_{ref}), \\ S9 &= ((SV4\cdot S^-)+\phi_1)\cdot(V1 \ominus V_{ref}), \\ S5 &= (\phi_2\cdot S^+)\cdot(V1 \ominus V_{ref}), \\ S8 &= (\phi_2\cdot S^-)\cdot(V1 \ominus V_{ref}), \\ S6 &= (V1 \ominus V_{ref})\cdot\phi_2, \\ S7 &= (V1 \ominus V_{ref})\cdot\phi_2, \\ S13 &= (V1 \ominus V_{ref})\cdot\phi_2, \\ S14 &= (V1 \ominus V_{ref})'. \end{aligned} \quad (3)$$

The main goal of (3) is to generate these control signals S1-S14 just like the theoretical waveforms in Fig.2 in order to realize the AHE control.

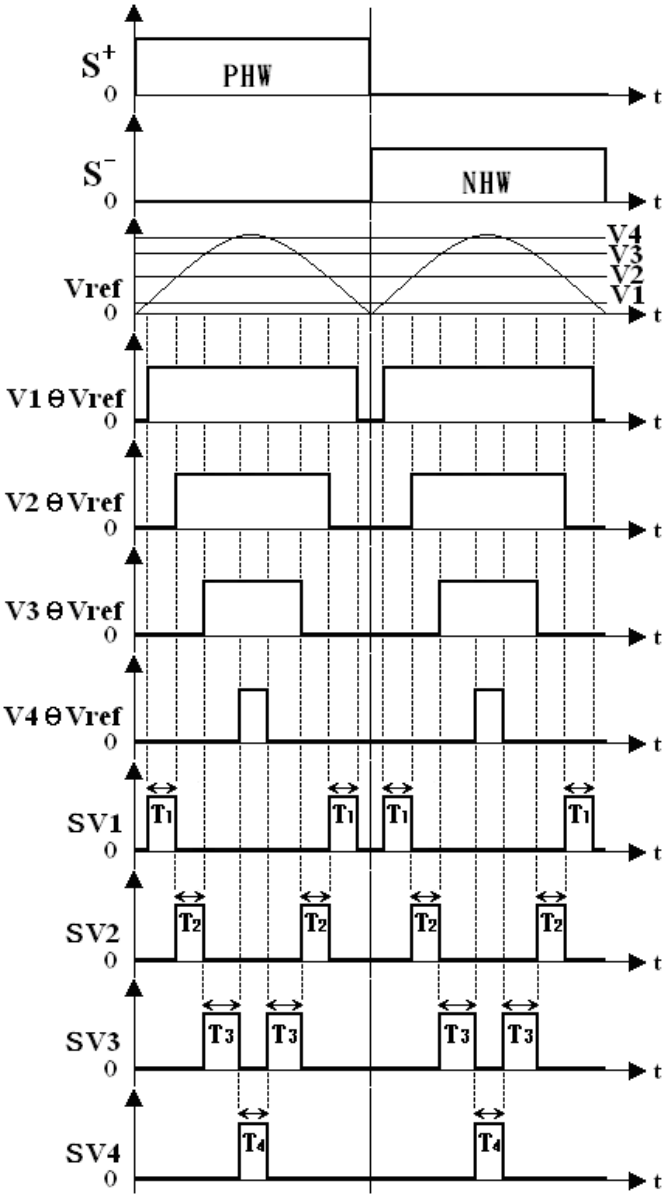

Fig.4. Theoretical waveforms of AHE control.

III. Example of Boost DC-AC Inverter

In this section, a closed-loop DC-AC inverter with AHE control is simulated by OrCAD, and then the results are illustrated to verify the efficacy of the proposed inverter scheme. All the parameters are listed in Table I. We have three cases to discuss as follows.

1) Case1:different frequencies
   a) Frequency=1.1k:
      Let the DC-AC booster source Vs1 and Vs2 be 5V, load R_L be 1kΩ, and the peak value and output frequency of V_{ref} are $V_{m,d}$=1V, fo=1.1kHz. And then, as shown in Fig.5, Vout has the peak value of 19.1V, and the practical output frequency is about 1.1kHz. The efficiency is 72.59%, and THD is 12.57%.
   b) Frequency=0.9k:
      Let the DC-AC booster source Vs1 and Vs2 be 5V, load R_L be 1kΩ, and the peak value and output frequency of V_{ref} are $V_{m,d}$=1V, fo=0.9kHz. And then,

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TABLE I
COMPONENTS OF DC-AC BOOST INVERTER

Supply source	5V*2
Switch capacitor (C1~C3)	0.3uF
Load capacitor (Co)	0.1uF
Load resistance (RCo)	1Ω
Resistance of capacitor (r)	2Ω
MOSFET of SC booster	Transmission Gate
Switch on Resistance	0.01Ω
Peak value of Vout	19.2V
Frequency of SC boost	200kHz
MOSFET W/L	20m/1u, 40m/1u
Diode	Dbreak
Output impedance	1kΩ, 1.2kΩ
Output voltage	13.02 V_{rms}
Output frequency	900Hz, 1kHz , 1.1kHz

as shown in Fig.6, Vout has the peak value of 19.1V, and the practical output frequency is about 0.9kHz. The efficiency is 78.2%, and THD is 12.75%.

2) Case2:different loads
   a) Load=1.2k:
      Let the DC-AC booster source Vs1 and Vs2 be 5V, load R_L be 1.2kΩ, and the peak value and output frequency of V_{ref} are $V_{m,d}$=1V, fo=1kHz, respectively. And then, as shown in Fig.7, Vout has the peak value of 19.2V, and the practical output frequency is about 1kHz. The efficiency is 70.27%, and THD is 12.53%.
   b) Load=1k:
      Let the DC-AC booster source Vs1 and Vs2 be 5V, load R_L be 1kΩ, and the peak value and output frequency of V_{ref} are $V_{m,d}$=1V, fo=1kHz, respectively. And then, as shown in Fig.8, Vout has the peak value of 19.1V, and the practical output frequency is about 1kHz. The efficiency is 76.11%, and THD is 12.82%.
3) Case3:different peaks
   a) Load=1k, Frequency=1k, $V_{m,d}$=1V:
      Let the DC-AC booster source Vs1 and Vs2 be 5V, load R_L be 1kΩ, and the peak value and output frequency of V_{ref} are $V_{m,d}$=1V, fo=1kHz, respectively. And then, Vout has the peak value of 19.1V, and the practical output frequency is about 1kHz, and the steady-state root-mean-square value (V_{rms}) of Vout is 13.02V as shown in Fig.9. The efficiency is 76.11%, and THD is 12.82%.
   b) Load=1k, Frequency=1k, $V_{m,d}$=0.974V:
      Let the DC-AC booster source Vs1 and Vs2 be 5V, load R_L be 1kΩ, and the peak value and output frequency of V_{ref} are $V_{m,d}$=0.974V, fo=1kHz. And then, Vout has the peak value of 19.05V, and the practical output frequency is about 1kHz, and the steady-state root-mean-square value (V_{rms}) of Vout is 12.32V as shown in Fig.10. The efficiency is 72.86%, and THD is 13.63%.

According to the above results, it is obvious that Vout is following V_{ref} for the different frequencies, loads and peaks. These results show that this AHE-based inverter has a good steady-state performance.

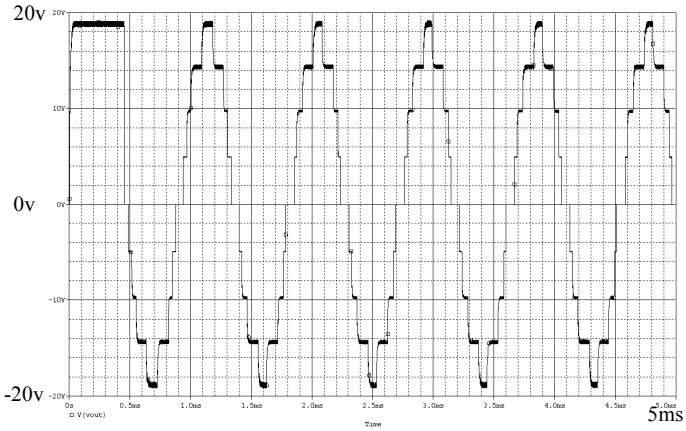

Fig.5. Output Vout when fo=1.1kHz, R_L=1kΩ.

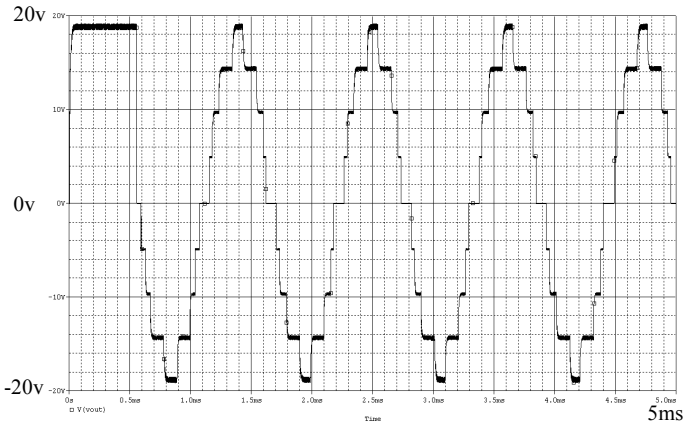

Fig.6. Output Vout when fo=0.9kHz, R_L=1kΩ.

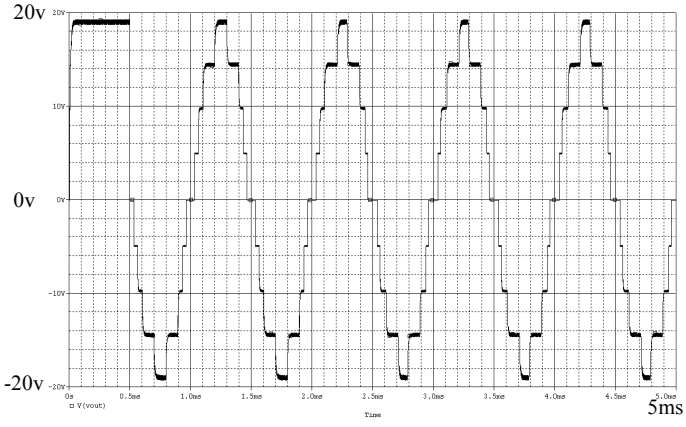

Fig.7. Output Vout when fo=1kHz, R_L=1.2kΩ.

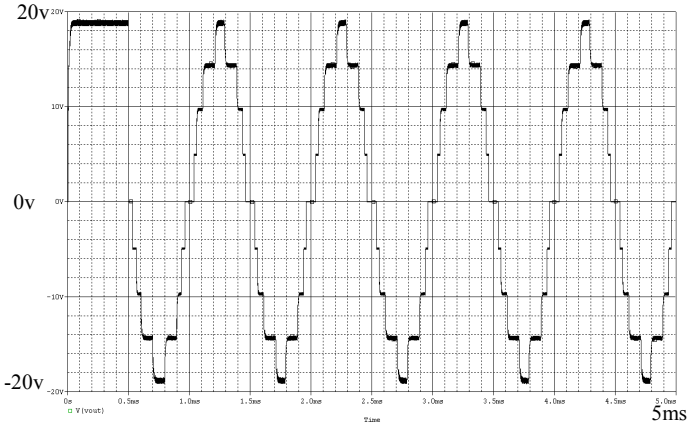

Fig.8. Output Vout when fo=1kHz, R_L=1kΩ.

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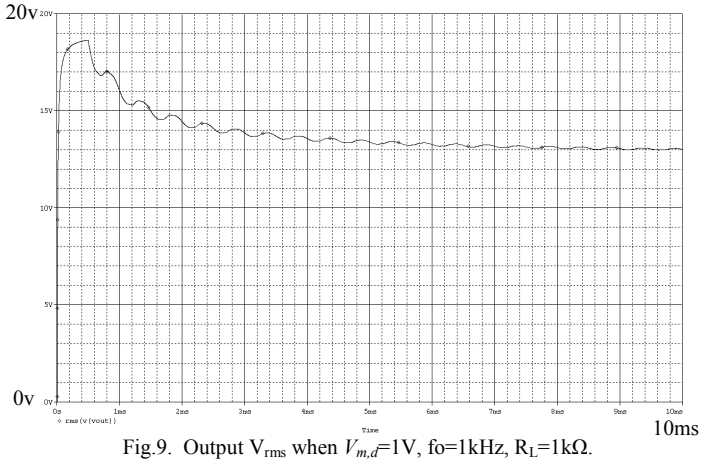

Fig.9. Output V_{rms} when $V_{m,d}$=1V, fo=1kHz, R_L=1kΩ.

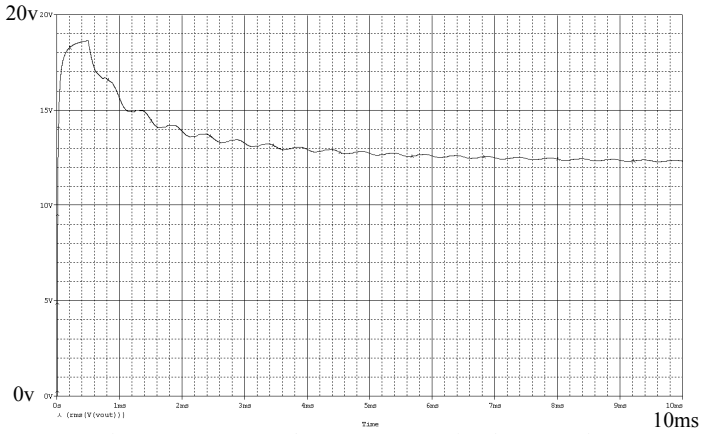

Fig.10. Output V_{rms} when $V_{m,d}$=0.974V, fo=1kHz, R_L=1kΩ.

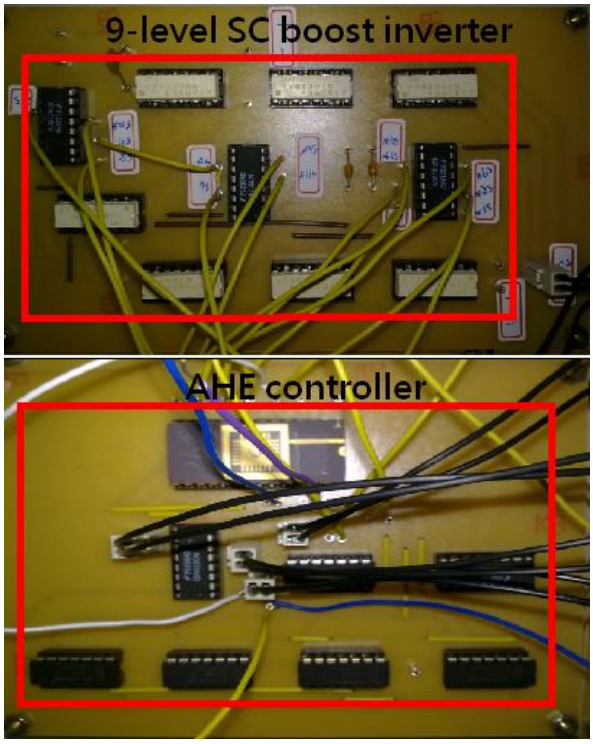

Fig.11. hardware implementation of AHE-based inverter.

IV. Conclusion

A closed-loop scheme of 9-level SC boost DC-AC inverter is proposed by combining AHE approach for a staircase DC-AC conversion and regulation. Here, the AHE approach is suggested and used for the consideration of the 3rd, 5th, 7th harmonic elimination not only to control the time intervals of the different output levels of 1x, 2x, 3x, 4x, but also to enhance the output regulation capability for the different desired outputs attitude and frequency. By using AHE control, it is realized that output Vout is following the reference V_{ref}, so as to make the output easier for the better THD. Here, this AHE-based inverter is simulated by OrCAD, and the results are illustrated to show the efficacy of the proposed scheme. Here, the efficiency is about 72.5%-78.2% and the THD is 12%-13%. At present, we have implemented the hardware of this AHE-based inverter circuit as the photo in Fig.11. Next, some more experimental results will be measured for the verification of this scheme.

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