Frequency Divider Design Using CMOS-NDR-Based Chaos Circuit

Kwang-Jow Gan*, Ping-Feng Wu, Din-Yuen Chan, Cher-Shiung Tsai,
Zhen-Kai Kao, and Jian-Syong Huang

***Abstract*—We present a frequency divider circuit using a negative-differential-resistance (NDR) circuit, which is composed of Si-based metal-oxide-semiconductor field-effect transistor (MOS) and bipolar junction transistor (BJT) devices. This circuit monolithically integrates a MOS-BJT-NDR circuit, an inductor, a capacitor, and a buffer. The operation is based on the long-period behavior of the NDR-based chaos circuit, which can show the variable frequency-dividing-ratio signal. We demonstrate the high-frequency characteristics of this frequency divider. The results show that the dividing ratio can be selected by modulating the input signal frequency. This frequency divider is fabricated using a 0.18 μm CMOS process.**

***Keywords*:—frequency divider, negative-differential-resistance circuit, chaos circuit, variable frequency-dividing-ratio signal, CMOS process.**

I. Introduction

In the past few years, the negative-differential-resistance (NDR) devices have attracted much attention as practical devices because of their potential for highly functional analog and digital circuits [1]-[4]. The NDR device has specially folded current-voltage (I-V) curve. A circuit consisting of such nonlinear I-V characteristic often shows the chaos phenomenon [5]. When an external periodic signal is used, such circuit shows an increased variety of bifurcation sequences. Then we can observe the long-period behavior which demonstrates the frequency divider characteristic.

For the previous circuit design, they often use the resonant tunneling diode (RTD) as a core device. The RTD is fabricated based on the III-V compound technique including the molecular-beam-epitaxy (MBE) and metal-organic chemical vapor deposition (MOCVD) system. Compared to silicon-based applications, the cost of MBE or MOCVD is more expensive and the process is not easy to be compatible with mainstream ULSI technology including the CMOS or BiCMOS process. Therefore, the applications based on the RTD devices suffer the problem of convenience.

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In this paper, we firstly demonstrate a NDR circuit made of Si-based metal-oxide-semiconductor field-effect-transistor (MOS) and bipolar junction transistor (BJT) devices. Then a NDR-based frequency divider circuit is designed based on this MOS-BJT-NDR circuit. The results show that we can obtain the variable frequency-dividing-ratio signal by inputting a sinusoidal signal. The fabrication of this NDR chaos-based frequency divider is based on the standard CMOS process provided by the Taiwan Semiconductor Manufacturing Company (TSMC) foundry.

II. NDR-Based Frequency Divider Circuit

The MOS-BJT-NDR circuit used in this work is made of five Si-based n-channel MOS and one BJT devices, as shown in Fig. 1. By suitably designing the MOS width/length (W/L) parameters, we can obtain the N-type I-V curve with NDR characteristic. The combined current of this MOS-BJT-NDR circuit is the sum of the collector current of the NPN BJT device and the drain current of MN3 device.

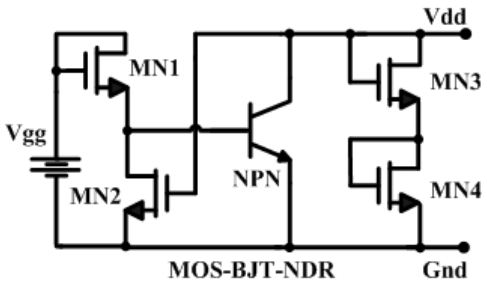

Fig. 1 Configuration of a MOS-BJT-NDR circuit.

The Vgg value must be large enough to turn on both MN1 and BJT devices. When we apply a fixed Vgg voltage and increase the bias Vdd gradually, the operating condition for the first positiv-differential-resistance (PDR) region can be described as the MN1 and the BJT device are saturated, and the MN2 device is turned off. When the bias Vdd is high enough to turn on the MN2 device, then the base voltage of the BJT device will be decreased gradually. It results in the decrease of the collector current of the BJT device. It is demonstrated as the NDR region of the combined I-V curve. Finally, both the MN1 and the MN2 devices are saturated, and the BJT device is turned off. The combined current of the MN1, MN2, and BJT devices is shown as a Λ-type I-V characteristic, as shown in Fig. 2. As for the operation of the MN3 and MN4 devices, the bias Vdd should be larger than the sum of the threshold voltage of two devices. The MN3 and MN4 devices are act as two series-connected dynamic resistors. The combined I-V characteristics are presented as an exponential curve, as shown in Fig. 2, which establish the second PDR region of the combined I-V curve. Therefore, we

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can obtain an N-type I-V curve in the combined I-V curve of the MOS-BJT-NDR circuit by increasing the bias Vdd gradually.

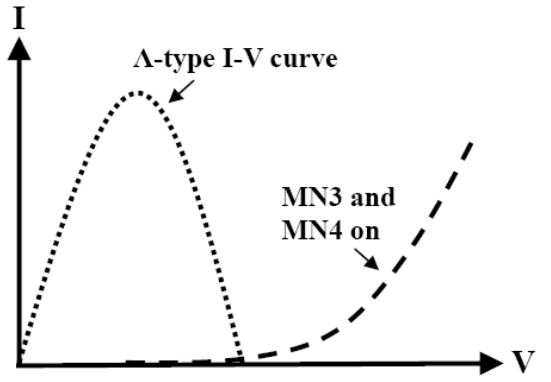

Fig. 2 The I-V characteristics of the MOS-HBT-NDR circuit.

In particular, this NDR circuit possesses the ability to control the peak current by the external voltage terminal Vgg. Figure 3 shows the measured three I-V curves with the Vgg values 1.4 V, 1.45V, and 1.5 V, respectively. When the Vgg is biased at 1.45 V, the peak voltage is 0.3 V, valley voltage is 0.9 V, peak current is 0.42 mA, and valley current is 0.026 mA. The peak-to-valley current is about 16.1 at room temperature.

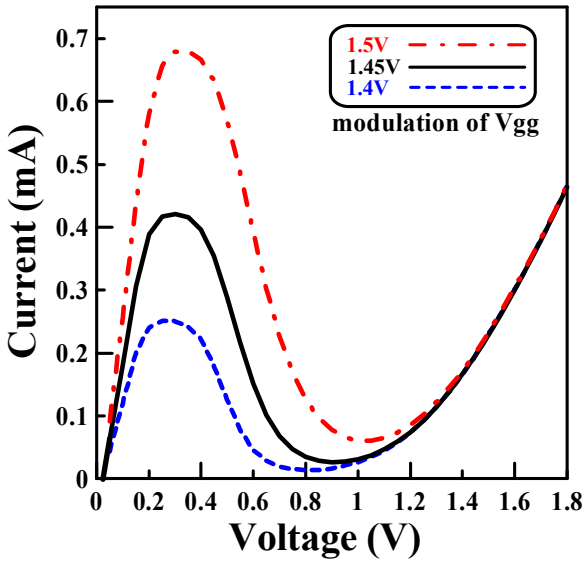

Fig. 3 The measured I-V curves of the MOS-HBT-NDR circuit by modulating the Vgg values.

Compared to the resonant tunneling diode (RTD) device, this MOS-BJT-NDR circuit is much easier to combine with other Si-based devices and circuits to accomplish the NDR-based applications. Referring to the folded I-V characteristic, the NDR circuit is a strong nonlinear element. The nonlinear system can generate the chaos phenomena, and also observed the long-period behavior in some parameter regions [6]-[8]. This is called the bifurcation phenomenon. We can observe the period-adding phenomena and the alternating periodic chaotic transition sequence. That means the output signal period of the nonlinear system will be the integer-multiple of the input signal period.

Fig. 4 shows the circuit topology of the frequency divider. This circuit monolithically integrates a MOS-BJT-NDR circuit, an inductor, a capacitor, and a buffer. This circuit is a kind of van der Pol oscillator. It outputs various types of signal patterns including subharmonic oscillations and chaos, when it is driven by an external periodic signal $Vsin=V_{DC}+Asin(2\pi ft)$, where V_{DC} is a DC bias, A is the amplitude, and f is the frequency. The subharmonic signals can be used for designing a dynamic frequency divider with variable frequency-dividing-ratio. However, applications of chaos have attracted much attention in the field of information processing and communication systems [9].

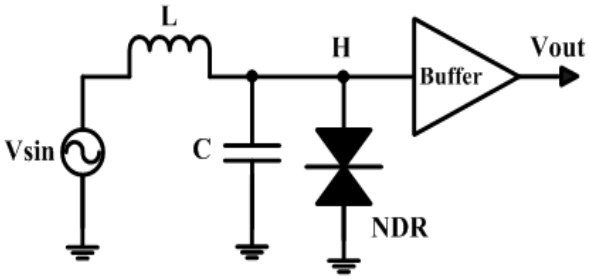

Fig. 4 Circuit configuration of a frequency divider.

The inductor and capacitor are designed as 30 μH and 1 pF, respectively, so that the characteristic frequency f_{LC} is about 29 MHz. In order to obtain the high-frequency operation in measurement, a buffer design is required in this circuit. The buffer is composed by two cascaded NMOS-based inverters here.

III. Measured Results

This circuit outputs various signal patterns, including subharmonic oscillations and quasi-periodic or chaotic waveforms, depending on the circuit parameters and the operating conditions. The bias V_{DC} is designed at 0.6 V, which is located at the NDR region of the MOS-BJT-NDR circuit, and the amplitude A is fixed at 0.3 V. Chaos is often shown as a random and uncontrollable phenomenon. In sampling oscilloscopes, chaos signals turn into blurred band-like signals [8]. Figure 5 shows one kind of the chaos signals observed in this circuit.

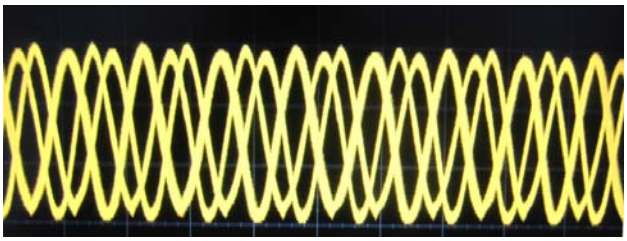

Fig. 5 Chaos waveform of this circuit.

The operation of the frequency divider can be described as follows. The current passing through the inductor (I_L) is the combined currents of MOS-BJT-NDR circuit (I_{NDR}) and capacitor (I_C); $I_L(t)=I_{NDR}(t)+I_C(t)$. The impedance of the inductor is proportional to the input signal frequency. When the input signal is at low frequency, the charges in capacitor are sufficient to switch the NDR circuit during a cycle of the input signal. Figure 6 shows the output waveforms for the 6.3 MHz sinusoidal inputs. The upper part is the input signal Vsin, and the lower part is the output signal Vout. As shown, the period of the output signal is the same as that of the input

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signal.

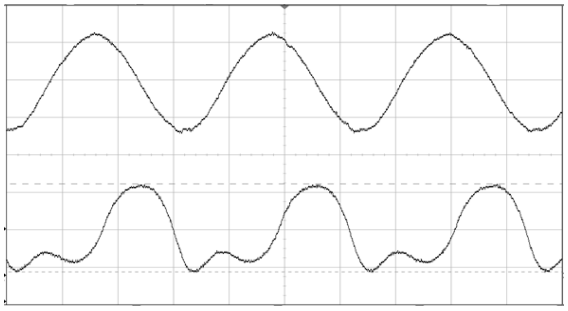
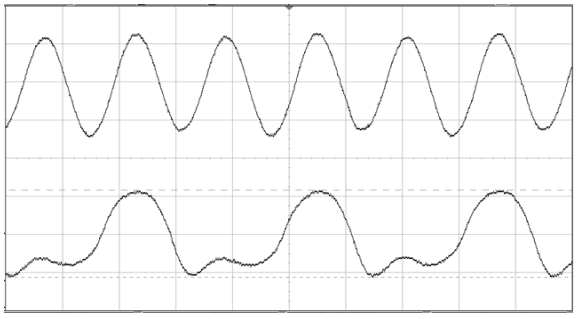
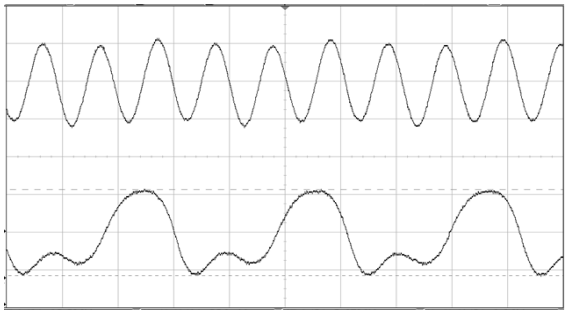


Fig. 6 The period of the output signal is the same as that of the input signal.

When the input frequency increases, the impedance of the inductor is increased. The charges supplied to the capacitance are not sufficient to switch the NDR circuit. Therefore, it requires two or more cycles of period to switch the NDR circuit. It will results in the frequency dividing operation with 1/2, 1/3, and so on. Therefore, we can obtain a dynamic frequency divider with variable frequency-dividing-ratio. Figures 7 (a) and (b) show the output waveforms for the 12.3 MHz and 19.6 MHz sinusoidal inputs, respectively. Clear 1/2 and 1/3 frequency dividing operation was observed.



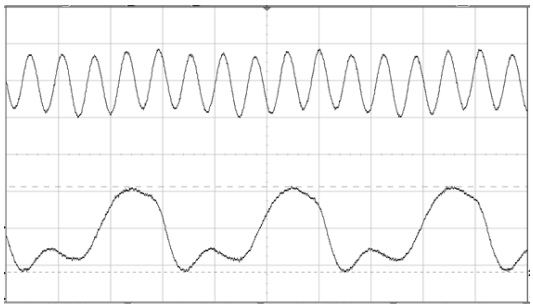
(a)



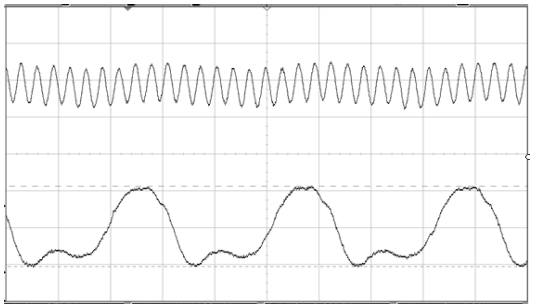
(b)

Fig. 7 Clear frequency divider operations of (a) 1/2 and (b) 1/3 are shown in the figure.

By further increasing the input frequency, we can obtain the higher stable 1/5 and 1/10 dividing-ratio operations as shown in Figs. 8 (a) and 8 (b), respectively. The modulation ranges for various dividing ratios corresponding to frequencies are shown in Table I. The results show that the dividing ratio can be selected by adjusting the input signal frequency. We also emphasize here that the dividing ratio can be chosen by adjusting the other parameters including bias voltage, capacitance, and inductance. The output period increases discontinuously with increasing frequency. This discontinuous region between dividing ratios indicate chaos phenomenon or quasi-periodic signal.



(a)



(b)

Fig. 8 Clear frequency divider operations of (a) 1/5 and (b) 1/10 are shown in the figure.

Table I Modulation ranges of dividing ratios.

Dividing ratio	Modulation Range (MHz)	Dividing ratio	Modulation Range (MHz)
1	5.78~6.65	7	45.8~46.65
2	12.46~12.63	8	51.18~52.45
3	18.5~19.37	9	56.83~57.23
4	24.82~25.58	10	63.03~64.25
5	31.28~32.45	11	69.93~70.16
6	40.3~40.8	12	76.03~76.72

The operating frequency is not only limited by the characteristic frequency f_{LC} but also is determined by the cutoff frequency of MOS-BJT-NDR circuit. Therefore, a higher operating frequency is expected, if these frequency dividers are implemented by further advanced CMOS or BiCMOS process.

IV. Conclusions

We have demonstrated a frequency divider using an MOS-BJT-NDR chaos circuit. This circuit design is based on the strong nonlinearity of its NDR characteristic. The operation of this frequency dividing is based on the bifurcation phenomenon which appears in the waveforms of subharmonic oscillation. The results show that we can obtain the variable frequency-dividing-ratio signal by modulating the frequency of a sinusoidal signal.

Because this MOS-BJT-NDR circuit is made of the Si-based MOS and BJT devices, it is convenient to integrate with the other active or passive devices to achieve the system-on-a-chip. We implemented this circuit using the standard CMOS process provided by the TSMC foundry.

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These characteristics might provide some useful ideas to design the NDR-based applications in the future.

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