Low Power Decimator Design Using Bit-Serial Architecture for Biomedical Applications

Kristin Scholfield and Tom Chen

Abstract—**Due to limited battery capacity, electronics in biomedical devices require low power consumption. On the other hand, biomedical devices that integrate multiple functions like sensing, amplification, signal conditioning, signal processing, data storage, etc. have put a greater constraint on power consumption for each functional unit. This paper presents a low power design of a decimator for a sigma-delta ADC for biomedical applications in a commercial 0.18µm CMOS process. Two features help make the design low power: use of bit-serial architecture and use of an ultra-low supply voltage of 0.9V in a 0.18 µm CMOS design. The design interfaces with a sigma-delta modulator with a clock rate of 1MHz.**

Keywords: Low Power Circuits, Biomedical Devices, Analog-to-Digital Converter, and Decimator.

I. Introduction

Bioelectronics has opened a new frontier for high quality, high availability and low cost patient care. Commercially available glucose testing devices are a good example of improved testing and diagnosis made possible by advances in biomedical devices and the associated bioelectronics. More recent advances in bioelectronics focus on integration of a variety of functions on a single biomedical device [1] [2]. This trend helps improve the overall functionality of biomedical devices. However, it put a greater constraint on power consumption of each functional circuit being integrated on to the same chip.

One of the important functions of bioelectronics is to convert the analog signals from various sensors to their digital format. Using sigma-delta ADCs, such conversion takes place in two steps. One is sigma-delta modulation [3] and the other is decimation filtering [4]. This paper focuses on the design of a decimation filter using some of the low power design techniques. Architecturally, the design uses bit-serial arithmetic circuits for lower complexity and lower power consumption. At the circuit level, transistors are optimized for the lower supply voltage of 0.9V for lower power consumption. 0.9V is half of the standard rail supply voltage for the 0.18µm CMOS process. The resulting decimator is 0.029mm^2 in size and consumes 225µW of power while running at 1MHz clock rate.

II. Bit-Serial v. Bit-Parallel Systems

There are two options for the design of the decimation filter: a bit-parallel or bit-serial design. Since bit-parallel systems compute the data simultaneously, they are often used in systems requiring high speeds at the cost of chip space and power [5]. However, for biomedical applications, low power is greatly desirable, since the chip may be used in applications where a small power source is used and available power is limited. In addition, high speed is not needed since the time scale for biomedical applications usually ranges from milliseconds to seconds [6].

The most common architecture used for decimation filters is the bit-parallel configuration. In this architecture, if the word length is 10 bits, all 10 bits are processed in parallel by 10 bit-slice units, plus any additional logic for dealing with carry signals, etc. This means that the data can be processed quickly, although wide buses are required for routing.

Another, less complex architecture that can be used is the bit-serial implementation. In this implementation, one bit of the word is processed each clock cycle. This means that wide buses are no longer needed. In addition, only one bit-slice processing unit is needed for the entire word-length of data, significantly reducing the overall hardware complexity.

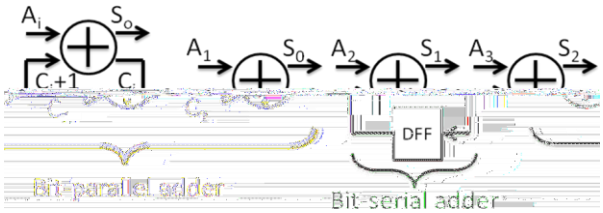

Figure 1. Comparison of bit-parallel adder to a bit-serial adder

Fig. 1 illustrates the difference between the bit-serial and bit-parallel architectures in the form of an adder. For the bit-serial architecture, each bit is fed through a single full-adder slice one by one, using N clock cycles where N is the data word length. For the bit-parallel architecture, all bits are processed simultaneously, but each bit requires a separate adder slice.

The bit-serial architecture does have some disadvantages, however. The bit-serial configuration will be slower, since only one bit gets processed at a time. In addition, large registers may be needed, which can potentially increase the amount of power consumed [7]. However, these large registers will most likely take up less area than the overall bit-parallel design, so an increase in power is unlikely.

III. Previous Work

The sigma-delta analog-to-digital converter (ADC) consists of two parts, a modulator and decimator [8] [9]. The modulator will take an incoming analog signal and convert it into a digital bit stream whose average corresponds to the input analog signal. The decimator will then take that bit stream and convert it to a digital output of N bits, where N is the required wordlength. Cascaded integrator comb (CIC)

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filters are often used for the decimator side of the ADC for its simplicity. The basic first-order CIC structure includes one integrator stage and one comb stage as shown in Fig. 2.

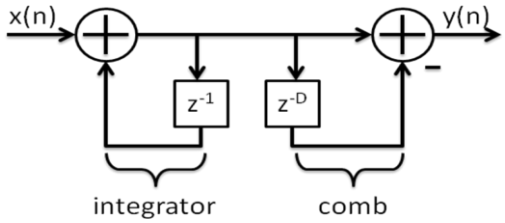

Figure 2. Basic first order CIC structure

The integrator takes in the input sample and recursively adds the delayed signal to the incoming signal at each clock cycle. Subsequently, the comb stage subtracts the differentially delayed output of the integrator from the original output. The amount of differential delay, D, will determine the amount of ripple seen at the output. In order to choose the best D, one must observe the frequency response of the filter at different values of D. The frequency response has the shape of a sinc function as shown in Fig. 3. Different values of D will make the first lobe of the sinc function closer or farther away from the DC. The higher the value of D, the better the low pass filter.

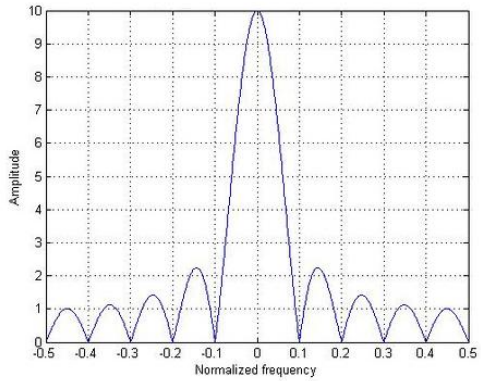

Figure 3. The shape of the frequency response of the decimator, similar to a sinc function

In order to improve anti-aliasing, the order of the CIC filter can be increased. We use a third order CIC to improve anti-aliasing and the sharpness of the cut-off frequency for the CIC filter, while not making the filter prohibitively expense to implement.

For many decimator applications, noise and speed, rather than power, are the primary goals. Therefore bit-parallel designs will often be implemented to improve speed. In addition, since these designs were not targeted for low power, they can operate at supply voltages of up to 5V [10]. [10] directly compares a bit-parallel to a bit-serial design for a 5V supply. For the bit-parallel design, the power consumption was 33.28mW. With the implementation of bit-serial, they are able to reduce the power consumption by half. For our proposed design, the power consumption is further reduced by operating the filter at a 900mV supply, instead of the nominal 1.8V supply. Reducing power supply is a powerful tool to quadratically reduce power consumption. But it requires care balance of gate designs to maintain drive strength to meet the overall performance goal of operating at 1MHz clock rate.

In [7], several bit-serial architectures are proposed. The basic block diagram for the decimator in [7], as seen in Fig. 4, is an adder with a 25-bit shift register for the integrator section and another 25-bit shift register with a subtractor for the comb section. In this implementation, the clock frequency for the bit-serial circuit is 25 times that of the bit-parallel, for the same fifth order CIC filter. Because of this, [7] saw a reduction in chip area from the bit-parallel implementation of 0.045mm^2 in size to the bit-serial implementation of 0.033mm^2 in size, with an increase in power consumption at 6.144MHz data rate (315µW bit-parallel, 6399µW bit-serial). This indicates that the bit-serial architecture may not be suitable for all applications where high performance is required.

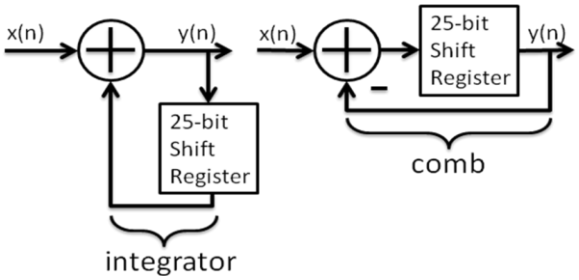

Figure 4. Bit serial architecture for an integrator and a comb for a 5th order CIC filter [7]

TABLE I. POWER CONSUMPTION

Serial/ Parallel	***Total Power***	***Total Area per bit***	***Clock Frequency***	***Process Used***
Serial [7]	6399µW	0.0013 mm^2/bit	6.144MHz	0.18µm CMOS
Parallel [10]	85mW	0.2mm^2/bit	10MHz	0.8 µm CMOS
Parallel [11]	33.28mW	312 gates/ bit	200MHz	0.6 µm CMOS
Serial [11]	15.12mW	267 gates/ bit	200MHz	0.6 µm CMOS

Several decimators that have been designed and tested are summarized in Table 1. The bit-parallel architectures that are displayed show a wide range of power consumption from 85mW to 315µW. The work done in [11] is one example of the improvement which can be gained by changing from bit-parallel to bit-serial. In this design, 15.16mW of power was saved by switching to bit-serial.

IV. PROPOSED BIT-SERIAL CIC DESIGN

The proposed decimator design is a part of an integrated sensor chip. Details of other components on the integrated sensor chip can be found [12] and [13]. In biomedical applications, the main design goal for the sensor chip is low power. Bandwidth of biomedical signals is typically low. With a 1MHz clock frequency, the proposed decimator, and the accompanying sigma-delta modulator has a 512 oversampling ratio. 0.18µm CMOS process being selected is more than sufficient for the required performance. In order to reduce the number of delay elements, and thus the power consumption, we used a bit-serial architecture. In the proposed bit-serial configuration, a word length of 10 bits is used. In order to avoid overflow, this word length is sign extended to 15 bits. The architecture is similar to [7] except that at the comb stage, the size of the shift register has been increased, as seen in Fig. 5.

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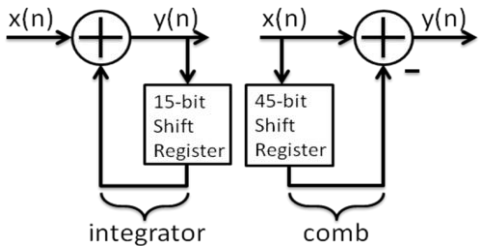

Figure 5. New bit serial architecture for an integrator and a comb for a 3rd order CIC filter

The purpose of the increased shift register size is to achieve the desired differential delay. The 45-bit shift register makes sure that the 15-bit word is delayed by 3x for the comb section. In addition, the bit-serial will run at the same frequency as the bit-parallel, and will be sampled at a slower frequency. This means that we should not see the large increase in power consumption observed in [7].

A few extra elements are needed for this design. One such element is a counter for the incoming signal. This counter will count the number of ones for every ten bits coming in from the modulator. After it has seen ten bits, it will reset and then count the next ten bits. The counter has a parallel output, so a parallel in, serial out (PISO) shift register is included to send a serial line of bits to the bit-serial CIC.

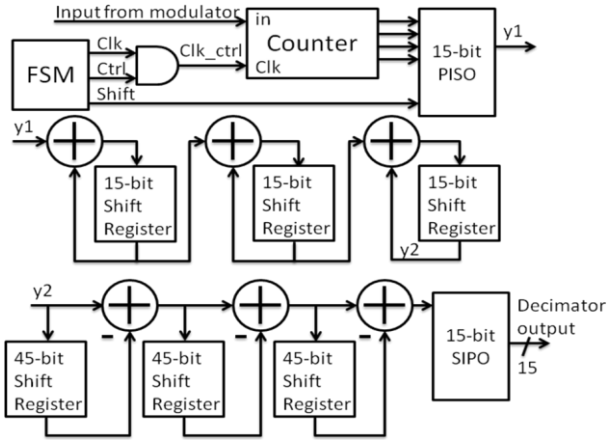

Figure 6. The top level diagram for the proposed bit-serial decimator design

Fig. 6 shows the top level block diagram for the proposed bit-serial decimator design. The FSM generates a control signal for the counter and the first integrator block. As was mentioned previously, the first section operates with 10 bits, but to avoid overflow, all subsequent blocks operate with 15 bits. In order for the first section to operate correctly, it needs to be stalled for five clock cycles while the rest of the blocks finish their computations. In order to accomplish this, we need a control signal that is high for ten clock cycles and low for five clock cycles. This control signal is then ANDed with the clock and the subsequent signal is used as the clock for the counter and the first integrator section while all other sections run on the normal clock. The FSM also produces another signal called shift that is used for the PISO shift register to change from parallel to serial.

The FSM itself is made up of a counter that counts from zero to thirteen. NANDs and inverters are used to produce the shift and control signals at the correct times. In addition, the shift is also used as a reset signal for the FSM counter so that it only goes from zero to thirteen instead of zero to fifteen. The Boolean equation for the control signal is

$$\text{Control signal} = [!Q4 + (!Q3 * !Q2)]*\text{shift}. \quad (1)$$

In (1), Q4 is the MSB of the counter and Q1 is the LSB. Because the shift is also the reset, the control signal needed to be ANDed with the shift so that it stayed low for the proper amount of time. The shift goes low on count 13 and control needs to be low until 14, so the AND sets the control signal low during reset to accomplish this goal. The shift Boolean equation is

$$\text{Shift} = !(Q1 * !Q2) + !(Q3 * Q4). \quad (2)$$

In (2) we see that the shift signal is high until the count equals 1101, or 13, at which point shift goes low for one clock cycle. This shift signal will also be used for any subsequent electronics following the decimator, as the output will be valid only every 15th clock cycle. If the shift signal is inverted, its rising edge can be used as a clock to achieve this goal.

For the final design, 250 DFFs, 124 NANDs, 16 inverters and 10 multiplexers were needed. This gives us a total of 40 gates/bit. When compared to [11], this is a reduction of 227 gates/bit.

V. Simulation Results and Layout

The overall design was simulated at the schematic level as well as the extracted layout level. Ideally, the decimator would receive its input from a modulator, which would output a string of ones and zeros. A sample string to represent a sine wave from a modulator was used to simulate the decimator. This output was then compared to a behavior model of the decimator in MATLAB.

Fig. 7 shows the final results from the extracted layout simulation. A bit stream input was created from a 1kHz sine wave fed into a modulator. The outputs S_out through S_out3 are the final outputs from the integrator stages of decimator. S_out4, S_out5, and y15 are the outputs from the comb stages of the decimator. The final output is 15 bits long and is valid every fifteenth clock cycle, with a clock cycle of 1MHz.

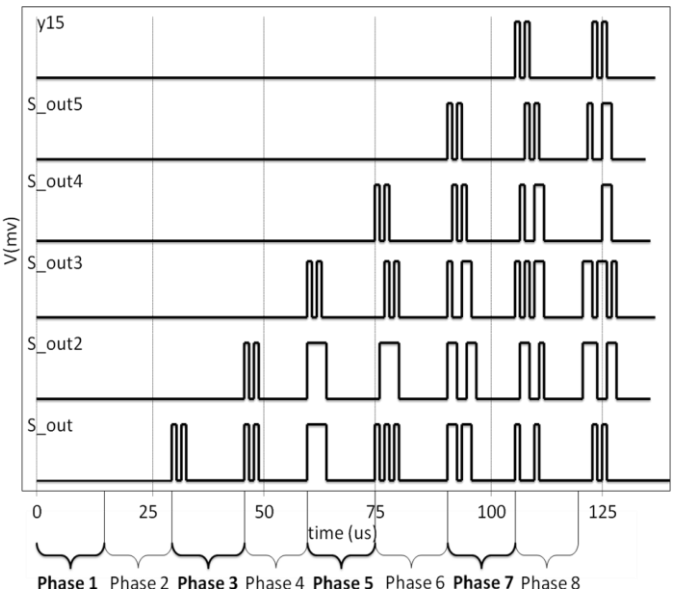

Figure 7. Raw Cadence results with phases separated into 15µs sections

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Phase 1 of the simulation is the 1st 15 clock cycles and is used as a reset period. During phase 2, the data is being stored in the 1st fifteen bit shift register. At phase 3 you can see the first output from the first integrator. During phases 4 and 5, the data begins to appear at the outputs of the second and third integrators. During phases 6 and 7, the data is being processed through the first two comb filters. Finally, at phase 8, we begin to see the final output from the final comb stage, represented by y15, which is the LSB of the final output. As the graph clearly indicates, it takes from phase 2 to the beginning of phase 8, or 90 clock cycles, before data appear at the output.

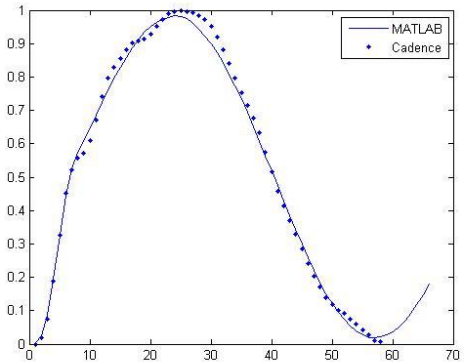

Figure 8. Final normalized sine wave output of the decimator

Fig. 8 shows the ideal input sine wave and the decimator output sine wave. A small amount of distortion can be seen on the Cadence graph that occurs when there is a low amount of differential delay. This distortion would increase if D were lowered to 30 or 15, as seen in Fig. 9.

The final result that we see at the output is the digital representation of the sine wave originally fed into the sigma-delta modulator with a frequency decimated by 15 clock cycles. Thus, instead of a 1kHz wave on the output, we see approximately a 66Hz sine wave normalized to 1V peak.

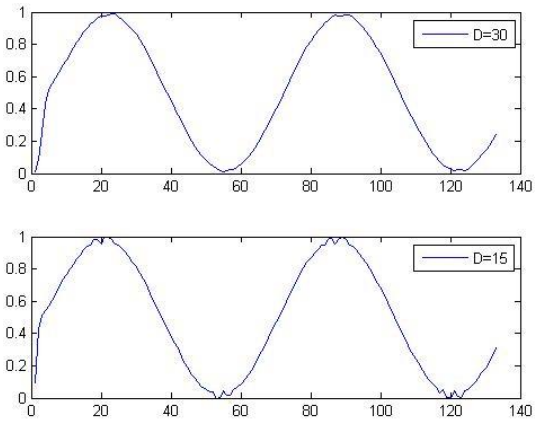

Figure 9. Output comparison showing distortion at lower delay values

In order to define the amount of distortion seen in the final output, a Gaussian distribution was taken of the difference between the Cadence output and the ideal simulations in MATLAB. This curve can be seen in Fig. 10. The integrated biosensor chip is designed to have a 400mV peak-topeak at the input of the on-chip ADC with a 10-bit resolution, the LSB is 400µV. The error distribution from the proposed design has a sigma value of 16.8µV and a mean error of 10 µV. The worst case error of mean plus 3sigma in this case is 60.4 µV which is well below LSB.

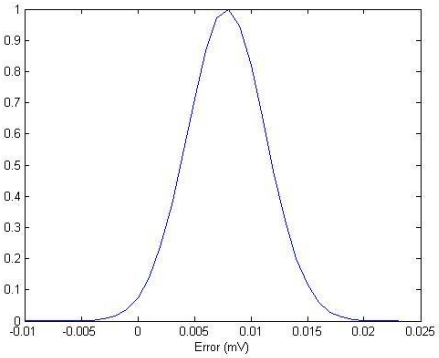

Figure 10. Gaussian distribution of the Cadence error from the ideal

The final layout shown in Fig. 11 was implemented in a commercial 0.18um CMOS process with 174.8µm by 166.2µm in size for a total area of 0.029mm^2. The entire chip area for the integrated sensor is approximately 1mm by 1mm so the decimator takes up about 3% of the available space.

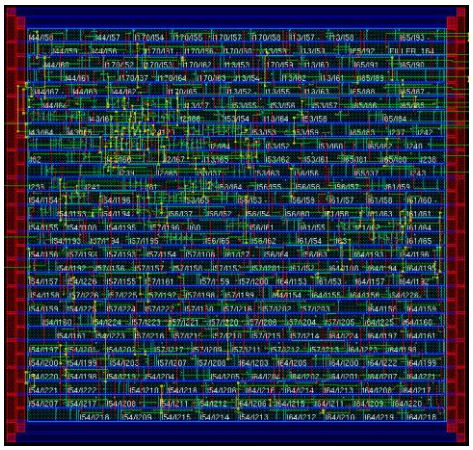

Figure 11. Final layout of the decimator

VI. CONCLUSION

The bit-serial configuration offers a promising solution to reduce the size of the decimator on chip, as well as a way to reduce the amount of power consumption. This configuration does have the drawback of running slower compared to bit-parallel designs. However, this drawback is far outweighed by the reduction in size and power consumption, and the reduction in performance poses no problem for biomedical applications. Table II shows the final comparison between our work and the previous work. Compared to bit-parallel designs, the proposed decimator design is significantly smaller and consumes a significant less amount of power. The bit-parallel designs work well for high-precision and high-speed applications. However, the bit-serial configuration is ideal for biomedical applications because of the low power and small size that it offers. The proposed decimator design is slightly larger than the similar bit-serial design reported in [7]. However, it is important to note that the power and area calculated in [7] does not include routing or parasitics in the final calculation. Our size and power consumption data was obtained using the final routed layout shown in Figure 11, and the power consumption data is from

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the extracted netlist from the layout. The layout includes power grid and a clock tree, making it larger if you only consider logic gates. Our total power consumption is significantly lower than that reported in [7]. This can be attributed to the fact that the design in [7] has a higher clock rate and significantly more latches and flip-flops. In addition, the clock frequency data from [7] may not reflect the actual clock frequency when parasitic capacitance and resistance are included.

TABLE II. FINAL RESULTS

Serial/ Parallel	***Total Power***	***Total Area per bit***	***Clock Frequency***	***Process Used***
Serial (this work)	225 µW	0.00193 mm^2/bit	1MHz	0.18µm CMOS
Serial [7]	6399µW	0.0013 mm^2/bit	6.144MHz	0.18µm CMOS
Parallel [10]	85mW	0.2mm^2/bit	10MHz	0.8 µm CMOS
Parallel [11]	33.28mW	312 gates/ bit	200MHz	0.6 µm CMOS
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REFERENCES

[1] A. Hassibi and T. Lee, "A programmable 0.18-um CMOS electrochemical sensor microarry for biomolecular detection," IEEE Sensors Journal, vol. 6, no. 6, December 2006

[2] S. Martin, et al., "A fully differential potentiostat," IEEE Sensors Journal, vol. 9, no. 2, 2009

[3] B. E. Boser and B. A. Wooley, "The design of sigma-delta modulation analog-to-digital converters," IEEE Journal of Solid-State Circuits, vol. 23, no. 6 December 1988

[4] P. M. Aziz, H. V. Sorensen, and J. Van der Spiegel, "An overview of sigma-delta converters," Signal Processing Magazine, IEEE, vol. 13, pp. 61-84, January 1996

[5] O. Vainio, H. Tenhunen and J. Nurmi, "Architecture and circuit design for DSP-ASIC," Euro ASIC '90, pp. 56-61, June 1990

[6] M. Stanaćević, K. Murari, A. Rege, G. Cauwnberghs, and N. V. Thakor, "VLSI potentiostat array with oversampling gain modulation for wide-range neurotransmitter sensing," IEEE Transactions on Biomedical Circuits and Systems, vol. 1, no. 1, pp. 63-72, March 2007

[7] S. M. Zanjani, S. R. Omam, S. M. Fakhraie, and O. Shoaei, "Experimental evaluation of different realizations of recursive CIC filters," CCECE '06, pp. 1056-1059, May 2006

[8] Y. Park, S. Karthikeyan, W. M. Koe, Z. Jiang and T. Tan, "A 16-bit, 5MHz multi-bit sigma-delta ADC using adaptively randomized DWA," Custom Integrated Circuits Conference, pp. 115-118, September 2003

[9] S. Lee and C. Cheng, "A low-voltage and low-power adaptive switched-current sigma-delta ADC for bio-acquisition microsystems," Circuitss and Systems I: Regular Papers, vol. 53, pp. 2628-2636, December 2006

[10] K. Nakamura, M. Hotta, R. Carley and D. Allstot, "A 85-mW, 10-bit 40-Ms/s ADC with decimated parallel architecture," Custom Integrated Circuits Conference, pp. 495-498, May 1994

[11] C. Lei, Z. Yuanfu, G. Deyuan, W. Wu, W. Zongmin, Z. Xiaofei, and P. Heping, "A decimation filter design and implementation for oversampled sigma delta A/D converters," VLSI Design and Video Technology, pp. 55-58, May 2005

[12] M. Duwe, T. Chen, "Low power integrated potentiostat design for µelectrodes with improved accuracy," Circuits and Systems (MWSCAS, pp1-4, August 2011

[13] W. Pettine, M. Jibson, T. Chen, S. Tobet an C. Henry, "Charaterization of novel microelectrode geometries for detection of neurotransmitters," Sensors Journal, IEEE, in press

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