High-Gain Serial-Parallel Switched-Capacitor Step-Up DC-DC Converter

Yuen-Haw Chang and Song-Ying Kuo

***Abstract*—A closed-loop scheme of high-gain serial-parallel switched-capacitor step-up converter (SPSCC) is proposed by combining a phase generator and pulse-width-modulation (PWM) controller for step-up DC-DC conversion and regulation. The SC-based converter needs no magnetic element, e.g. inductor and transformer. In this SPSCC, there are two 3-stage SC cells in cascade between source V_S and output V_O, where each cell has 3 pumping capacitors. By using these capacitors charging in parallel and discharging in series, plus the front-stage voltage connected in series, each SC cell can be treated as a small step-up converter with a 4× voltage gain. Thus, this SPSCC is able to boost V_O to 4×4 times voltage of V_S at most just with the fewer number of pumping capacitors (6 totally). Further, the PWM technique is adopted not only to enhance the output regulation for the compensation of the dynamic error between the practical and desired outputs, but also to reinforce output robustness against source or loading variation. Finally, the closed-loop SPSCC is designed by OrCAD SPICE, and simulated for some cases as: (1) steady-state response, (2) dynamic response (source/loading variation).**

***Index Terms*—high-gain; serial-parallel; step-up; pulse-width-modulation; switched-capacitor (SC).**

I. Introduction

Recently, the demand for portable electronic devices has been increasing fast. With their light weight, small volume, multiple functionality and stand-alone power supply, these devices have found their way into many applications, such as PDA, E-book, cellular phone, etc. General speaking, this kind of portable equipments needs a small and compact power converter for converting battery voltage into the desired voltage value. However, the traditional converters have a larger volume and a heavier weight due to inductive elements, e.g. inductors and transformers. The SC-based power converter, possessing the power stage based on charge pump structure, is one of the good solutions to low-power DC-DC conversion because it has only semi-conductor switches and capacitors. Unlike traditional ones, inductor-less SC converters have light weight and small volume. Up to now, many SC types have been suggested and the well-known topologies are described as follows. In 1976, Dickson charge pump was proposed with two-phase clock connected with a diode chain via pumping capacitors [1]. But, its drawbacks included the fixed gain and larger device area. In 1997, Ioinovici and Zhu proposed SC circuit based on two symmetrical SC cells, and PWM was used for the output regulation enhancement [2-3]. In 2001, Starzyk presented a multiphase voltage double (MPVD) by multiphase operation. An n-stage Starzyk MPVD can boost voltage gain up to 2^n at most [4], i.e. the capacitor count in Starzyk is fewer for the same gain. Following the idea, Chang proposed many SC step-up/down DC-DC/DC-AC converters [5-7]. Nevertheless, some improved spaces still exist as follows:(i) Starzyk MPVD has the merits of fewer capacitor count and high gain, but it needs a complicated multiphase control circuit. Dickson charge pump or Ioinovici SC has a simple two-phase control circuit, but the gain is proportional to capacitor count. In this paper, the SPSCC scheme is presented for a compromise between capacitor count, voltage gain, and phase number of control circuit. Here, we use just 6 pumping capacitors to boost V_O up to 4×4 times voltage of V_S at most. (ii) Many SC circuits suffer from a limited regulation capability. For example, Starzyk MPVD circuit is fixed, the output voltage is also fixed. In this paper, we adopt PWM technique to compensate the error between the practical and desired outputs so as to enhance the output regulation as well as robustness against source/loading variation.

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II. Configuration of SPSCC

A. SPSCC scheme

Fig. 1 shows the overall circuit configuration of SPSCC, and it contians two major parts: "power part" and "control part" for achieving the closed-loop step-up DC-DC conversion and regulation.

Firstly, the power part of SPSCC is shown in the upper half of Fig. 1, and it is mainly composed of two SC cells (cell A1 and cellA2) in cascade between source V_S and output V_O. For more details, it includes 6 pumping capacitors (C_{A11}~C_{A13}, C_{A21}~C_{A23}), one output capacitor C_L and 8 switches (S1~S4, S5~S8*), where each capacitor has the same capacitance C (C_{A11}~C_{A13}=C_{A21}~C_{A23}=C). Fig. 2 shows the theoretical waveforms of 4×4 SPSCC in a switching cycle T_S. Each T_S contains four small phases (Phase I, II, III and IV), and each phase has the same phase cycle T ($T = T_S/4$).

Secondly, the control part of SPSCC is shown in the lower half of Fig.1, and it is composed of low-pass filter (LPF), PWM block, and phase generator. From the view of controller signal flow, the feedback signal V_O is sent into the OP-amp LPF for high-frequency noise rejection. Next the

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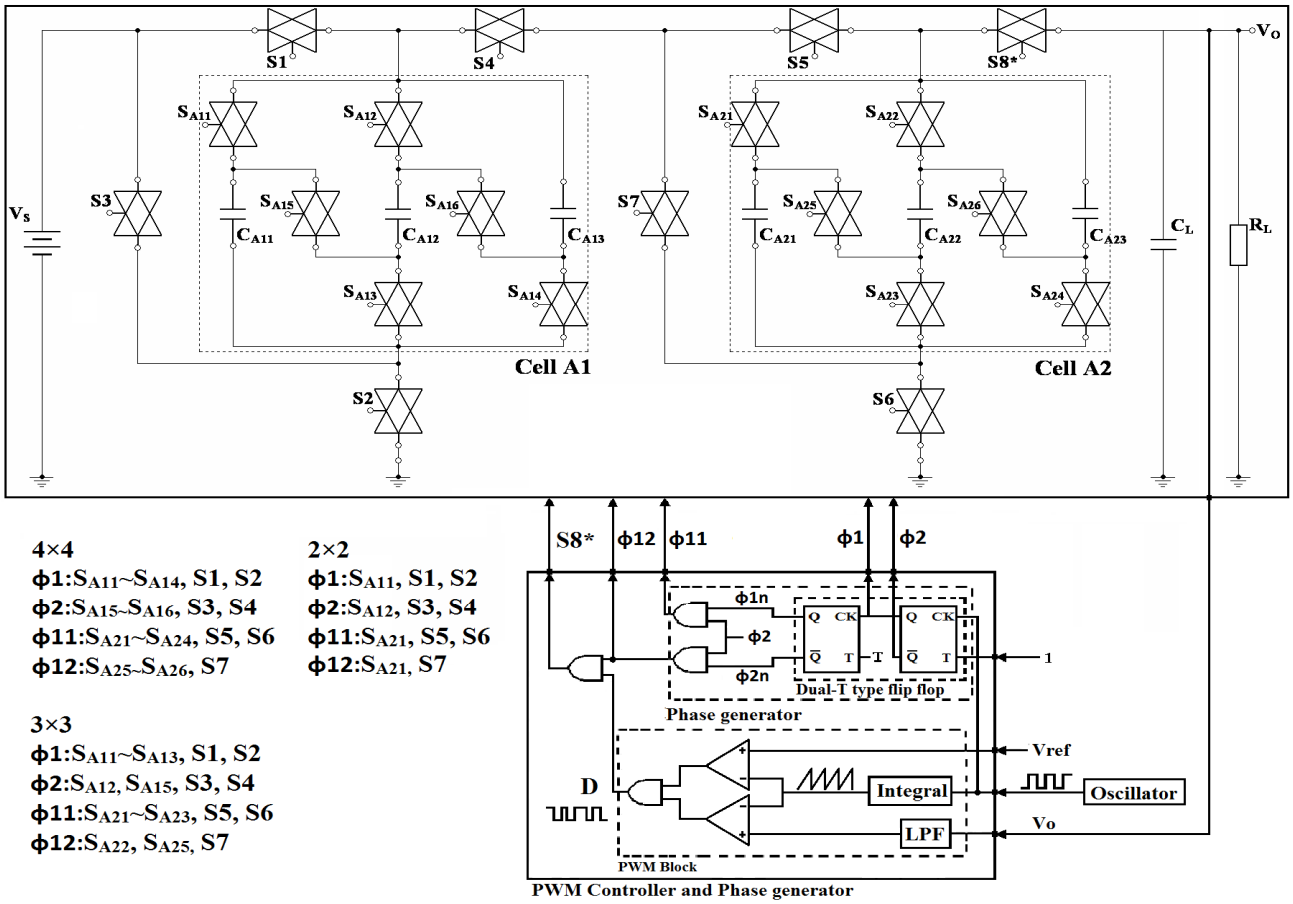

Fig. 1. Configuration of SPSCC.

filtered signal V_O is compared with the desired output reference Vref so as to produce the duty-cycle D via the PWM block. The main goal is to keep V_O on following Vref by closed-loop duty-cycle adjustment. At the same time, the phase generator can be realized by digital logic gates to generate the switch driver signals (S1~S4, S5~S8*, S_{A11}~S_{A16}, and S_{A21}~S_{A26}). In addition, the PWM switch S8* is controlled by using logic-AND combination between S7 and duty-cycle D. In this paper, by using the PWM control, the regulation capability of SPSCC will be improved for different desired output.

B. Operation of SPSCC

In order to achieving step-up function, this converter needs two basic ways: charging into capacitors in parallel and discharging from capacitors in series. Next, we explain the detailed running steps of SPSCC for boosting the voltage gain of 4×4, 3×3, 2×2, respectively.

Operation of 4×4 SPSCC

(Please see the symbol "————" of Fig. 3.)

(i) Phase I:
S1, S2, S_{A11}~S_{A14}: turn on. Then, the Phase I topology is shown in Fig. 3(a). C_{A11}~C_{A13} (Cell A1) are charged in parallel by the V_S.

(ii) Phase II:
S3, S4, S5, S6, S_{A15}~S_{A16}, S_{A21}~S_{A24}: turn on. The Phase II topology is shown in Fig. 3(b). C_{A11}~C_{A13} (Cell A1) are discharged in series with the V_S to transfer the power to C_{A21}~C_{A23} (Cell A2) in parallel.

(iii) Phase III:
It repeats Phase I operation as in Fig. 3(c). C_{A11}~C_{A13} (Cell A1) are charged in parallel by the V_S.

(iv) Phase IV:
S3, S4, S7, S8* (PWM), S_{A15}~S_{A16}, S_{A25}~S_{A26}: turn on. The Phase IV topology is shown in Fig. 3(d). C_{A11}~C_{A13} (Cell A1), C_{A21}~C_{A23} (Cell A2) are discharged in series with the V_S to supply load R_L via PWM control of S8*.

Operation of 3×3 SPSCC

(Please see the symbol "— — — —" of Fig. 3.)

(i) Phase I:
S1, S2, S_{A11}~S_{A13}: turn on. Then, the Phase I topology is shown in Fig. 3(a). C_{A11}~C_{A12} (Cells A1) are charged in parallel by the V_S.

(ii) Phase II:
S3, S4, S5, S6, S_{A12}, S_{A15}, S_{A21}~S_{A23}: turn on. The Phase II topology is shown in Fig. 3(b). C_{A11}~C_{A12} (Cell A1) are discharged in series with the V_S to transfer the power to C_{A21}~C_{A22} (Cell A2) in parallel.

(iii) Phase III:
It repeats Phase I operation as in Fig. 3(c). C_{A11}~C_{A12} (Cell A1) are charged in parallel by the V_S.

(iv) Phase IV:
S3, S4, S7, S8* (PWM), S_{A12}, S_{A15}, S_{A22}, S_{A25}: turn on. The Phase IV topology is shown in Fig. 3(d). C_{A11}~C_{A12} (Cell A1), C_{A21}~C_{A22} (Cell A2) are discharged in series with the V_S to supply load R_L via PWM control of S8*.

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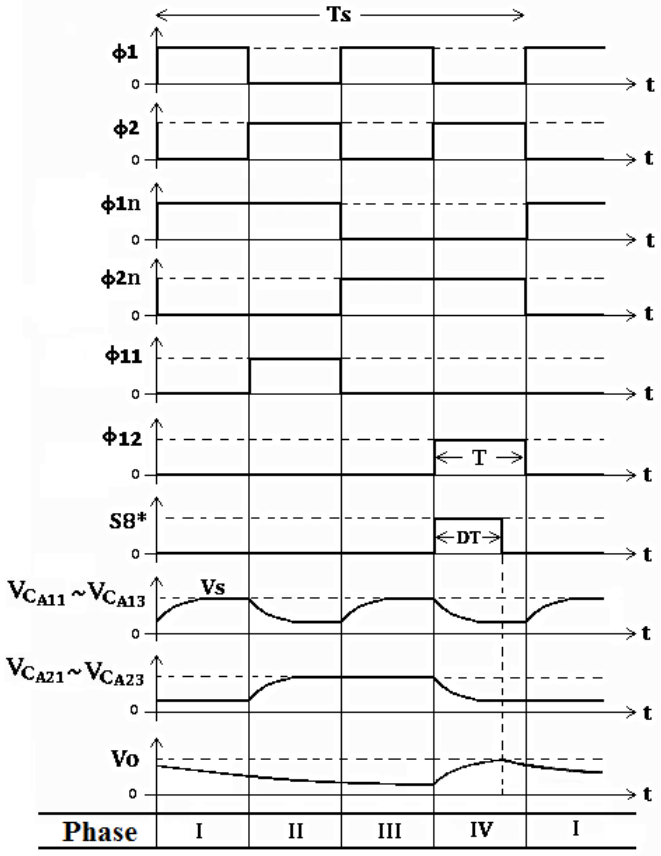

Fig. 2. Theoretical waveforms of 4×4 SPSCC.

Operation of 2×2 SPSCC

(Please see the symbol "— • — • —" of Fig. 3.)

(i) Phase I:
S1, S2, S_{A11}: turn on. Then, the Phase I topology is shown in Fig. 3(a). C_{A11} (Cell A1) are charged in parallel by the V_S.

(ii) Phase II:
S3, S4, S5, S6, S_{A11}, S_{A21}: turn on. The Phase II topology is shown in Fig. 3(b). C_{A11} (Cell A1) are discharging in series with the V_S to transfer the power to C_{A21} (Cell A2) in parallel.

(iii) Phase III:
It repeats Phase I operation as in Fig. 3(c). C_{A11} (Cell A1) are charged in parallel by theV_S.

(iv) Phase IV:
S3, S4, S7, S8* (PWM), S_{A11}, S_{A21}: turn on. The Phase IV topology is shown in Fig. 3(d). C_{A11} (Cell A1), C_{A21} (Cell A2) are discharged in series with the V_S to supply load R_L via PWM control of S8*.

By changing the operation of the switches, the SPSCC has the different circuit topologies so as to obtain the various boosting gains (e.g. 4×4, 3×3, 2×2). The switch operation for the various gains is shown in Table I, where S8* is a PWM-ON switch.

III. Simulation of SPSCC

In this section, based on Fig. 1, the closed-loop SPSCC converter is designed and simulated by OrCAD SPICE tool. The results are illustrated to verify the efficacy of the proposed scheme. The main function of SPSCC is to convert V_O to 4×4, 3×3, 2×2 times voltage of V_S at most (V_S = 3V) for supplying load R_L (300Ω) at switching

TABLE I
SWITCH OPERATION OF SPSCC (●: ON)

Stage	4×4				3×3				2×2			
Phase	I	II	III	IV	I	II	III	IV	I	II	III	IV
S1	●		●		●		●		●		●	
S2	●		●		●		●		●		●	
S3		●		●		●		●		●		●
S4		●		●		●		●		●		●
S5		●				●				●		
S6		●				●				●		
S7				●				●				●
S8*				●				●				●
S_{A11}	●		●		●		●		●	●	●	●
S_{A12}	●		●		●	●	●	●				
S_{A13}	●		●		●		●					
S_{A14}	●		●									
S_{A15}		●		●		●		●				
S_{A16}		●		●								
S_{A21}		●				●				●		●
S_{A22}		●				●		●				
S_{A23}		●				●						
S_{A24}		●										
S_{A25}				●				●				
S_{A26}				●								

frequency f_S (40kHz). The parameters are listed as: C = 400μF, C_L = 550μF (ESR 8mΩ), and the on-state resistance of switches is assumed at 0.005mΩ. Some cases will be simulated and discussed, including: (i) steady-state response, (ii) dynamic response (source/loading variation).

(i) Steady-state response:

The closed-loop 4×4/3×3/2×2 SPSCC is simulated for Verf = 47.5V/27.0V/12.0V respectively, and then these output results are obtained as shown in Fig. 4(a)-(b)/Fig. 4 (c)-(d)/Fig. 4(e)-(f). In Fig. 4(a), it is found that the settling time is about 20ms, and the steady-state value of V_O is really reaching 47.18V, and converter is stable to keep V_O following Vref (47.5V). In Fig. 4(b), the output ripple percentage is measured as rp = $\Delta vo/V_O$ = 0.0317%, and the power efficiency is obtained as η = 99.4%. In Fig. 4(c), it is found that the settling time is smaller than 15ms, and the steady-state value of V_O is really reaching 26.74V, and converter is stable to keep V_O following Vref (27.0V). In Fig. 4(d), the output ripple percentage is measured as rp = $\Delta vo/V_O$ = 0.0281%, and the power efficiency is obtained as η = 99.6%. In Fig. 4(e), it is found that the settling time is smaller than 10ms, and the steady-state value of V_O is really reaching 11.934V, and converter is stable to keep V_O following Vref (12.0V). In Fig. 4(f), the output ripple percentage can be easily found as rp = $\Delta vo/V_O$=0.0335%, and the power efficiency is obtained as η = 99.3%. Obviously, these results show that the step-up converter has a pretty good steady-state performance.

(ii) Dynamic response:

Since the source voltage is decreasing naturally with the running time of battery, or varying due to the bad quality battery, the output robustness against source noises must be considered. In the first case, it is assumed that source voltage starts at DC 3.0V, and then have a voltage drop at 20ms form 3.0V→2.5V as in the upper half of Fig. 5(a).

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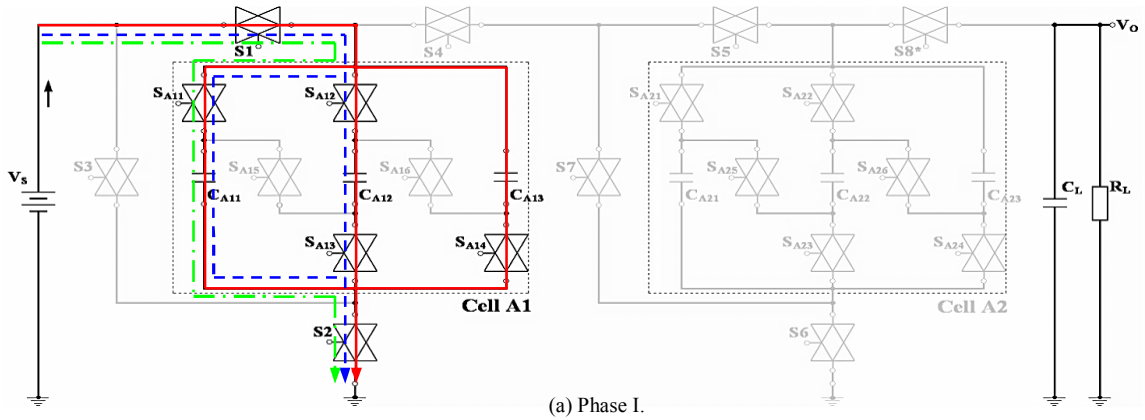
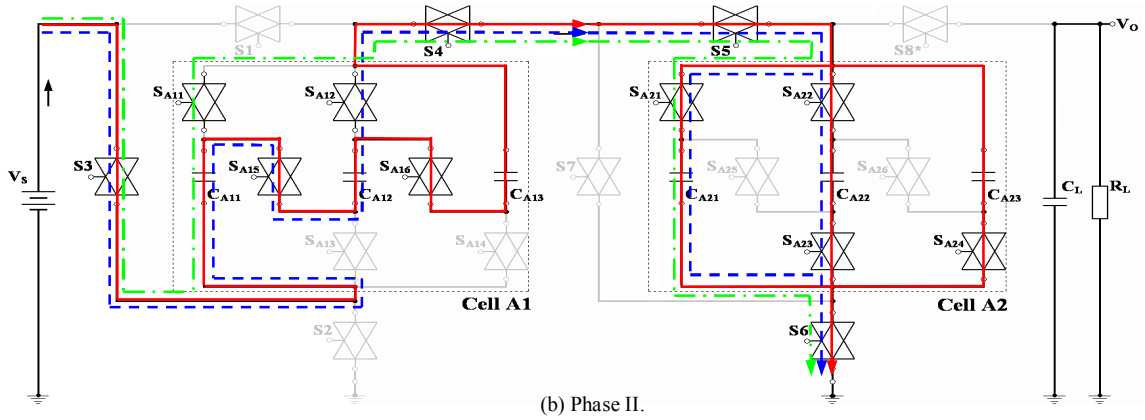
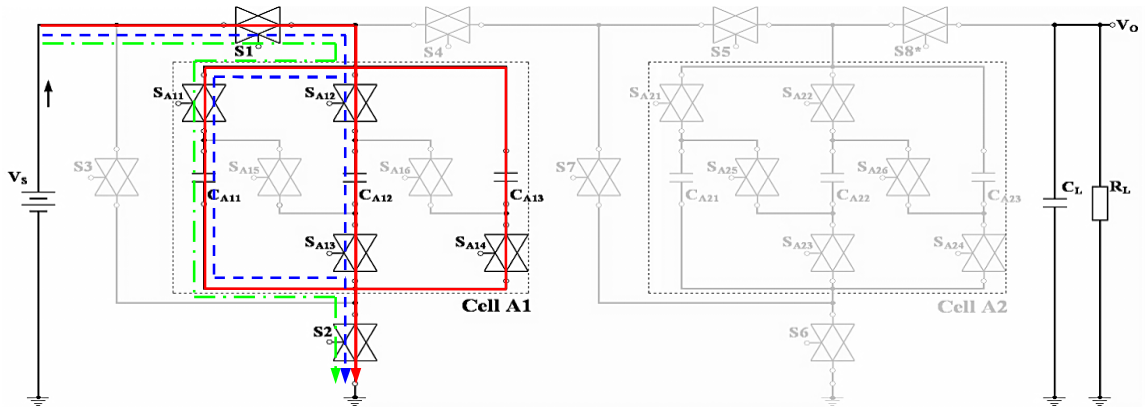


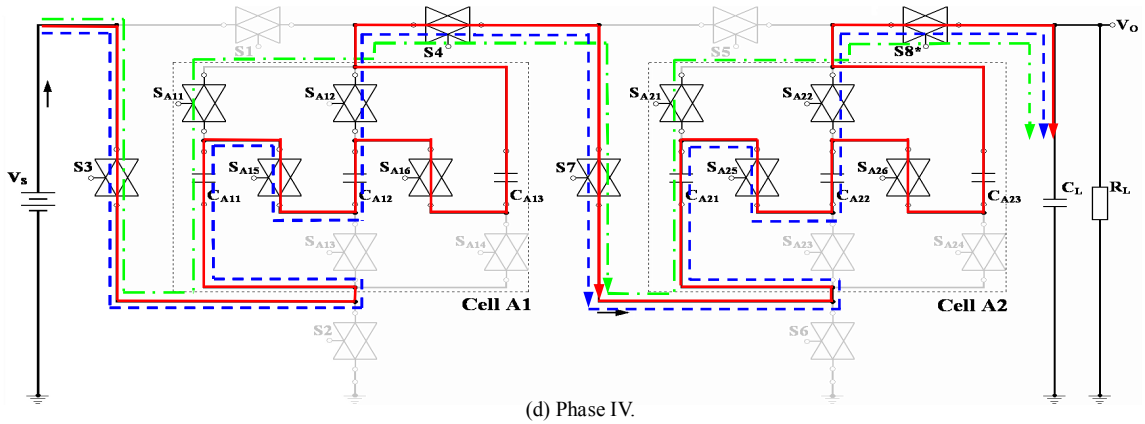
(a) Phase I.



(b) Phase II.



(c) Phase III.



(d) Phase IV.

Fig. 3. Topologies of SPSCC. (4×4: ———, 3×3: — — —, 2×2: — • — • —)

From the lower half of Fig. 5(a), obviously, V_O is still keeping on 39V (Vref=39V), even though V_S has the disturbance lower than standard source of 3.0V. In the second case, assume that V_S is the DC value of 3.0V and extra plus a sinusoidal disturbance of $0.3V_{P-P}$ as in the upper half of Fig. 5(b), and the waveform of V_O is shown in the lower half. Cleary, V_O is still keeping Vref (47.5V) in spite of sinusoidal disturbance. In the third case, the regulation capability for loading variation is discussed. Assume R_L is 300Ω normally, and it changes from 300Ω to

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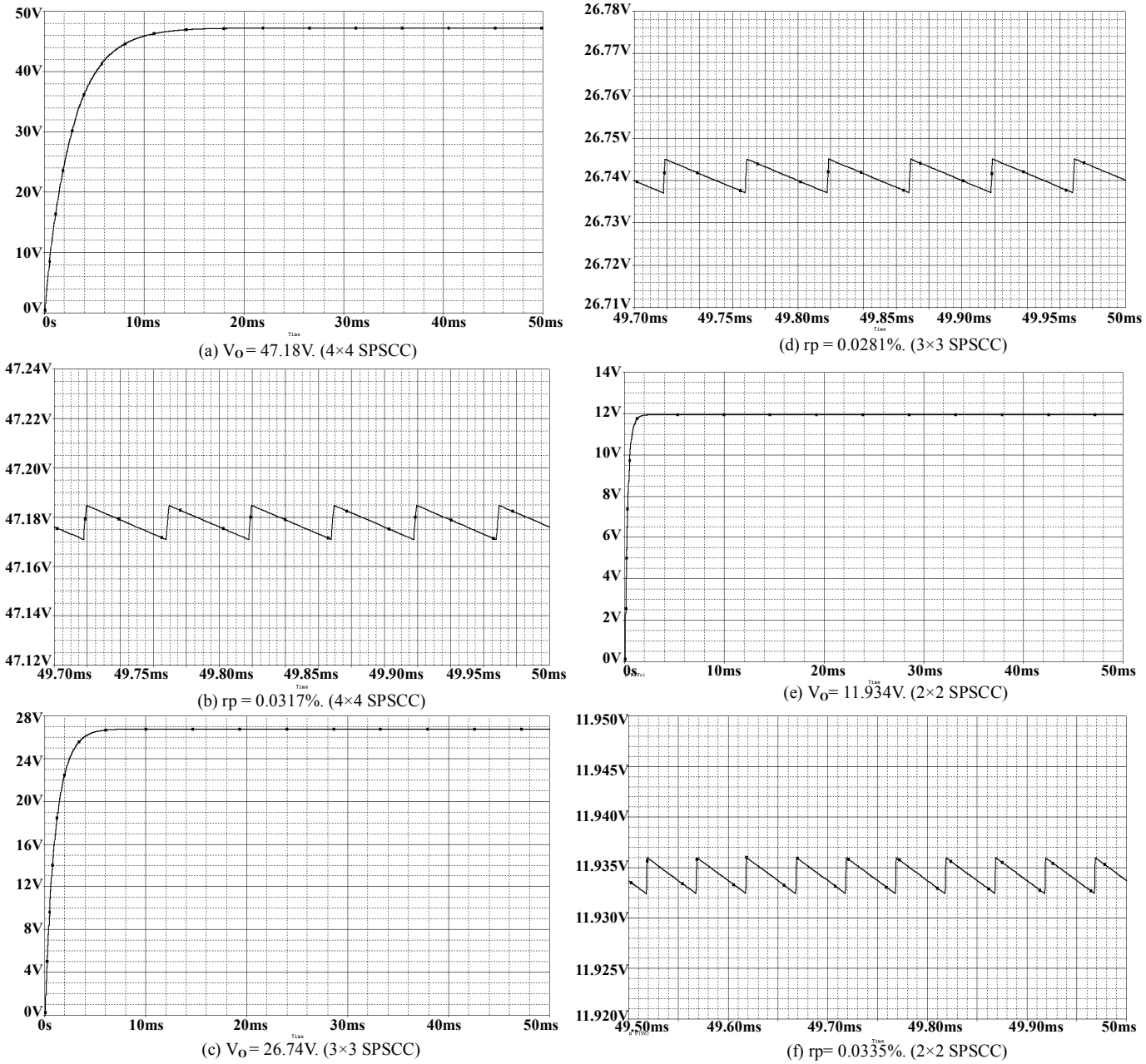

Fig. 4. SPSCC steady-state response.

60Ω at 20ms. After a short period, the load recovers from 60Ω to 300Ω at 40ms, i.e. R_L = 300Ω→60Ω→300Ω. Fig. 5(c) shows the transient waveform of V_O at the moment of loading variations. It is found that V_O has a small drop at 20ms~40ms and the curve shape becomes thicker during the heavier load, i.e. the output ripple becomes bigger at this moment. These results show that the closed-loop SPSCC has the good output robustness to source/loading variations.

IV. Conclusions

A closed-loop scheme of high-gain SPSCC is proposed by combining a phase generator and PWM controller for step-up DC-DC conversion and regulation. The advantages of the proposed scheme are listed as follows. (i) The SC-based SPSCC needs no magnetic element, so I.C. fabrication will be promising. (ii) This SPSCC use just 6 pumping capacitors to boost V_O up to 4×4 times voltage of V_S at most. (iii) By changing the operation of the switches, the SPSCC has the different circuit topologies so as to obtain the various boosting gains (e.g. 4×4, 3×3, 2×2). (iv) Since using COMS gate as a bidirectional switch, it is helpful to integrate various the step-up topologies into one structure. (v) By using PWM technique, the output regulation is enhanced as well as robustness to source/ loading variation. At present, we have implemented the hardware of SPSCC as shown the photo in Fig. 6. Next, some more experimental results will be obtained and measured for the verification of our SPSCC.

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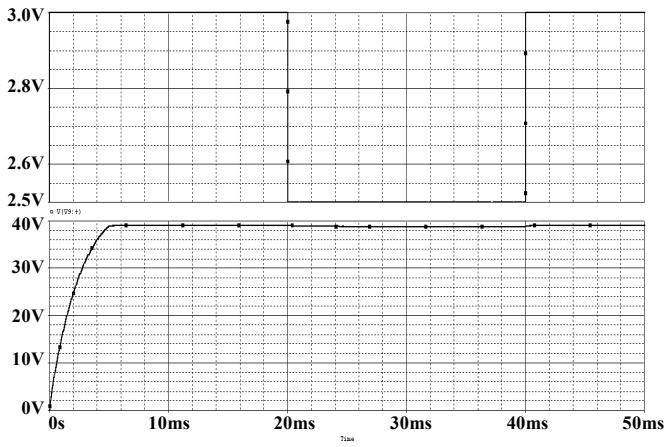
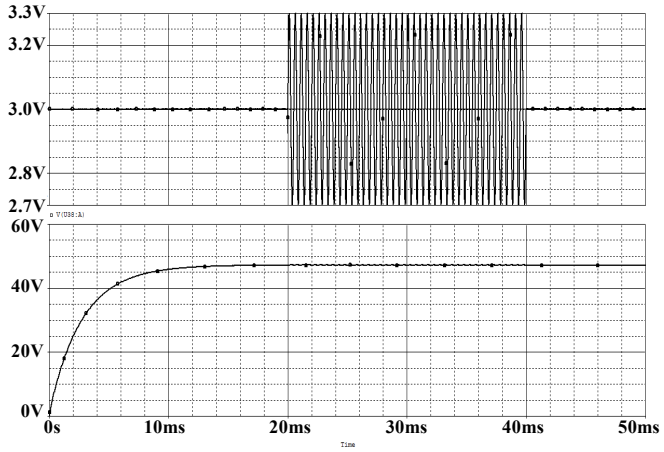
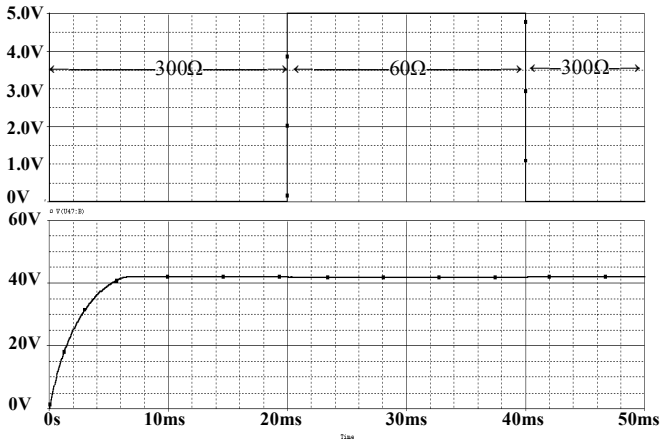


(a) Source voltage V_S=3V→2.5V.
Output voltage V_O=39V.



(b)Source voltage V_S=3±0.3sinwt.
Output voltage V_O=47.18V.



(c) Waveform of V_O when R_L=300Ω→60Ω→300Ω.

Fig. 5. SPSCC dynamic response.

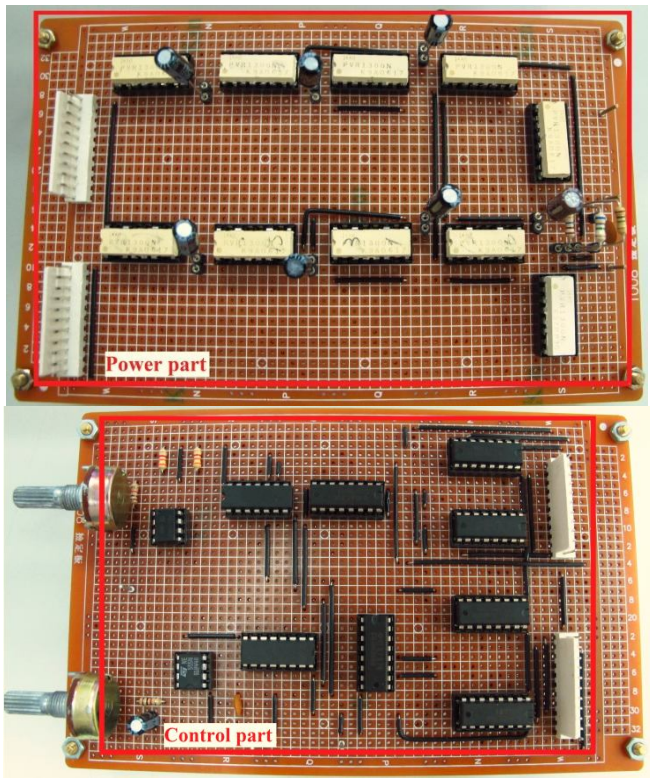


Fig. 6. Hardware implementation of SPSCC.

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