Closed-Loop 7-Level Switched-Capacitor Boost DC-AC Inverter with Sinusoidal PFM Control

Yuen-Haw Chang and Yun-Jie Huang

***Abstract*—A closed-loop 7-level switched-capacitor (SC) boost DC-AC inverter is proposed by using a sinusoidal pulse-frequency-modulation (SPFM) controller for low-power step-up inversion and regulation. In this SC inverter, there are three pumping capacitors and 10 switches between supply source and output terminal not only to boost the maximum gain up to 3, but also to invert the output voltage for the goal of 7-level DC-AC conversion. Here, the SPFM control is adopted in order to enhance output regulation capability for the various outputs (output peak value or output frequency). Besides, the 3x/2x/1x selector inside this controller is presented to select a proper gain according to the desired output voltage so as to improve the total harmonic distortion (THD), especially for the lower desired voltage. Finally, the closed-loop SC boost inverter is simulated by OrCAD, and all results are illustrated to show the efficacy of the proposed scheme.**

***Index Terms*—closed-loop, switched-capacitor (SC), boost DC-AC inverter, sinusoidal pulse-frequency-modulation (SPFM).**

I. Introduction

IN RECENT YEARS, due to the popularity of mobile devices, e.g. digital camera, e-book, smart phone, note-book, and pad …etc., the power modules of these products always ask for some good characteristics: small volume, light weight, higher efficiency, and better regulation capability. Generally, the traditional power converters have a large volume and a heavy weight because of magnetic elements. Therefore, more manufactures and researchers pay much attention to this topic, and ultimately, requiring DC-DC or DC-AC converters realized on a compact chip by mixed-mode VLSI technology.

The SC-based power converter has received more and more attention because it contains semiconductor switches and capacitors only. Thus, this kind of SC converters is one of the good solutions for low-power DC-DC/DC-AC conversion. Unlike the traditional converter, the SC converter needs no magnetic element, so it always has a small volume and a light weight. The SC converter is usually designed for an output higher than supply voltage or a reverse-polarity voltage. This function fits many applications, e.g. drivers of electromagnetic luminescent (EL) lamp, white light emitting diode (WLED), op-amp, and LCD drivers. In fact, the SC idea has existed over half a century. In 1990, the first SC step-down converters were proposed by Japan researchers [1], and their idea is to switch MOSFETS cyclically according to 4 periods of capacitors charging/discharging for step-down conversion. In 1993, Cheong *et al.* suggested a modified SC converter with two symmetrical SC cells working in the two periods [2]. In 1995, Chung and Ioinovici suggested a current-mode SC for improving current waveforms [3]. In 1998, Mak and Ioinovici suggested an SC inverter with high power density [4]. In 2004, Chang proposed the design and analysis of power-CMOS-gate-based SC boost DC-AC inverter [5]. The advantage of this SC inverter is to reduce the electromagnetic interference (EMI) problem. In 2007, Chang proposed CPLD-based closed-loop implementation of SC step-down DC-DC converter for multiple output choices [6]. In 2010, Hinago and Koizumi proposed a single-phase multilevel inverter by using switched series/parallel DC voltage sources based on multiple independent voltage sources in order to reach the higher number of levels so as to reduce the THD value [7]. In 2011, Chang proposed an integrated SC step-up/down DC-DC/DC-AC converter/ inverter [8-9].

In this paper, a closed-loop 7-level SC boost DC-AC inverter is proposed not only to enhance full-wave output regulation via SPFM technique, but also to improve the THD value.

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II. Scheme of 7-Level SC Boost DC-AC Inverter

Fig. 1 shows the closed-loop 7-level SC boost DC-AC inverter, and it contains a power part and a control part. The discussions are as follow.

A. Power Part

This SC boost inverter as in the upper of Fig.1 is composed of 10 switches (S1-S8), 3 pumping capacitors (C1-C3) and one output capacitor C_O between supply source Vs and output V_{out}, where each pumping capacitor has the same value C (C1=C2=C3=C). The main function of this power part is to boost V_{out} up to 3×, 2×, and 1× the voltage of Vs, and through H-birdge to invert V_{out} for reaching the sinusoidal waveform. Thus, this part can provide the output range of +3Vs ~ -3Vs for realizing DC-AC conversion. Fig. 3 shows the theoretical waveforms of these switches S1-S3, S7, S8, and these operations are discussed below.

1) Positive Half-Wave (PHW):
   a) Phase I:
   S1 turns on, and S2, S3, S4, S5, S6, S7, S8 turn off. The relevant topology is shown in Fig. 2(a). C1, C2, C3 are charged by Vs in parallel.

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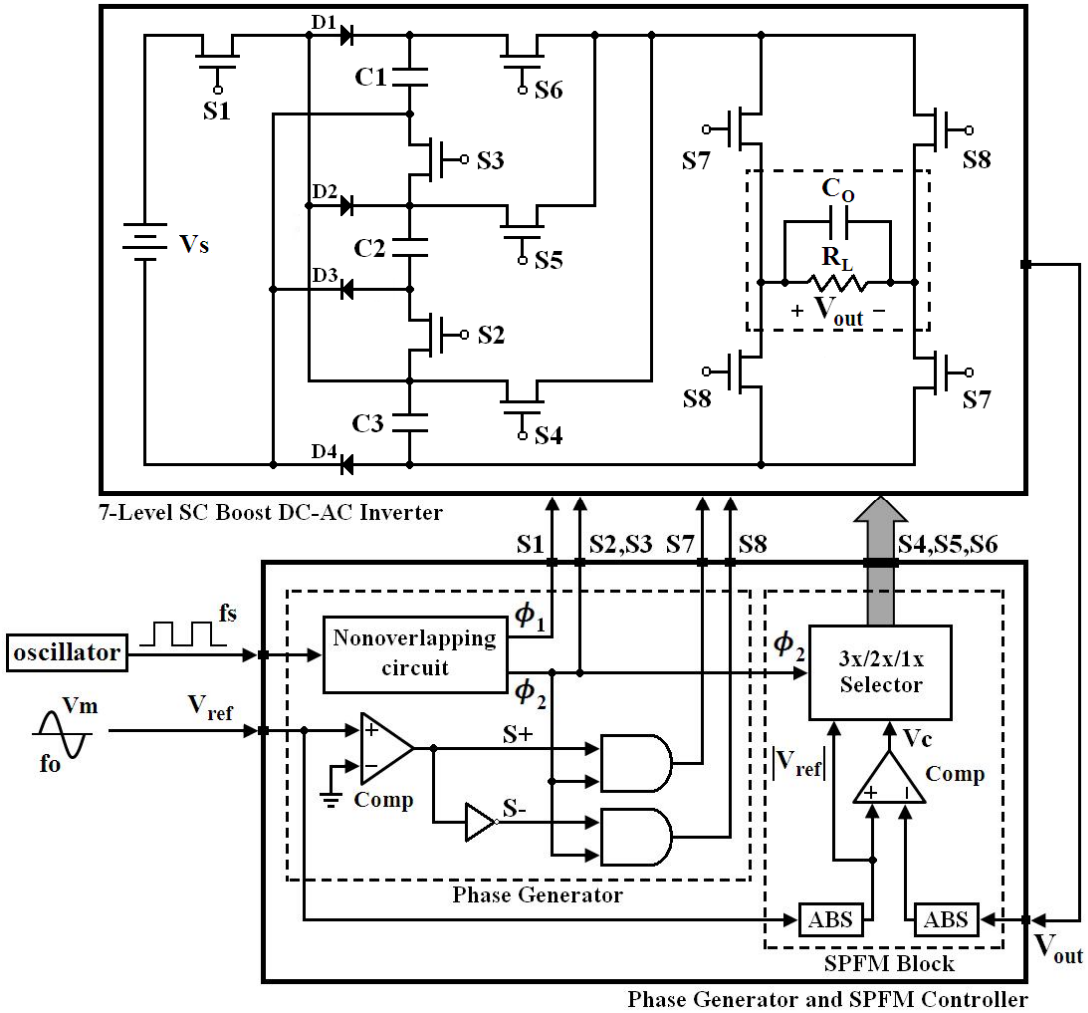

Fig. 1. Scheme of closed-loop 7-level SC boost DC-AC inverter.

b) Phase II:

In order to obtain the various voltage gains (3×, 2×, 1×), the different phase II operations (switches and topologies) are explained below.

(i) 3×:

S2, S3, S6, S7 turn on, and S1, S4, S5, S8 turn off. The current flow is passing from C1, C2, and C3 in series connection through S2, S3, S6, S7 to output terminal as shown in Fig. 2(b). So, the 3× function can be achieved with the help of C1, C2, and C3 in series.

(ii) 2×:

S2, S5, S7 turn on, and S1, S3, S4, S8 turn off. The current flow is passing from C2 and C3 in series connection through S2, S5, S7 to output terminal as shown in Fig. 2(c). So, the 2× function can be achieved with the help of C2 and C3 in series.

(iii) 1×:

S4, S7 turn on, and S1, S2, S3, S5, S6, S8 turn off. The current flow is passing from C3 through S4, S7 to output terminal as shown in Fig. 2(d). So, the 1× function can be achieved with the help of C3.

2) Negative Half-Wave (NHW):

a) Phase I:

S1 turns on, and S2, S3, S4, S5, S6, S7, S8 turn off. The relevant topology is shown in Fig. 2(a). C1, C2, C3 are charged by Vs in parallel.

b) Phase II:

In order to obtain the various voltage gains (3×, 2×, 1×), the different phase II operations (switches and topologies) are explained below.

(i) 3×:

S2, S3, S6, S8 turn on, and S1, S4, S5, S7 turn off. The current flow is passing from C1, C2, and C3 in series connection through S2, S3, S6, S8 to output terminal as shown in Fig. 2(b). So, the 3× function can be achieved with the help of C1, C2, and C3 in series.

(ii) 2×:

S2, S5, S8 turn on, and S1, S3, S4, S7 turn off. The current flow is passing from C2 and C3 in series connection through S2, S5, S8 to output terminal as shown in Fig. 2(c). So, the 2× function can be achieved with the help of C2 and C3 in series.

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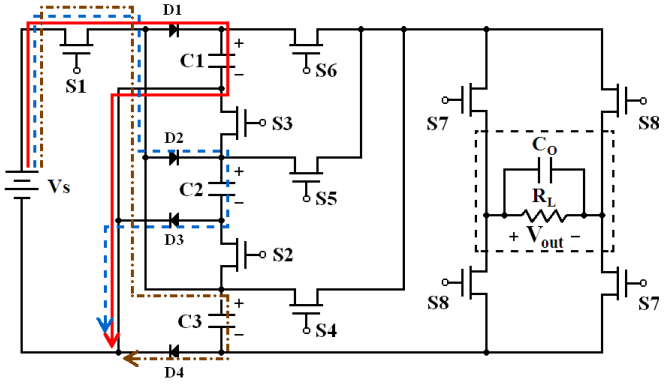

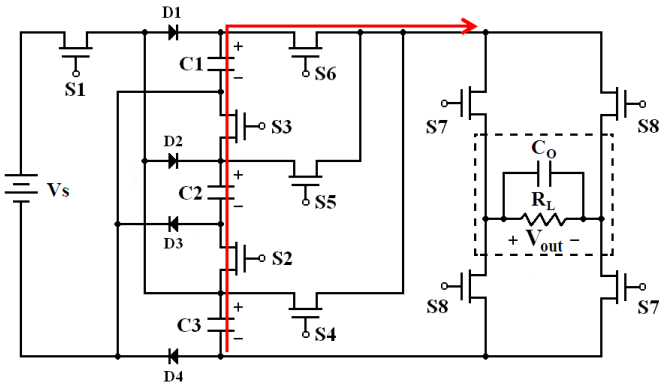

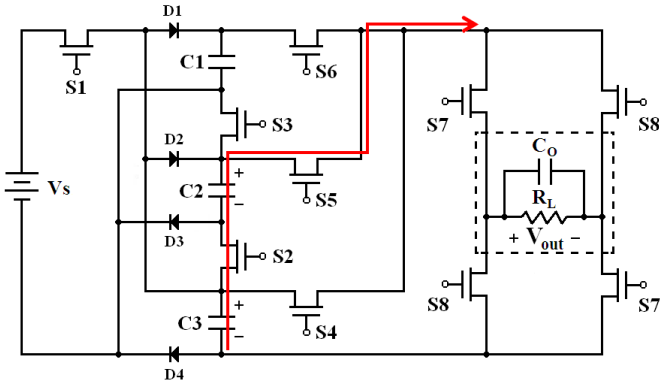

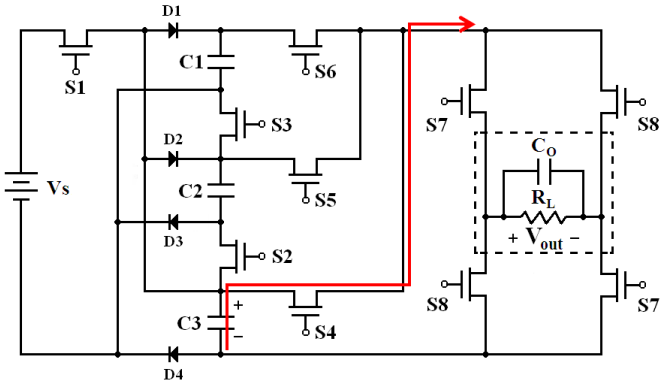

Fig. 2. (a) Phase I topology, (b) Phase II topology of 3x, (c) Phase II topology of 2x, (d) Phase II topology of 1x.

(iii) 1×:
S4, S8 turn on, and S1, S2, S3, S5, S6, S7 turn off. The current flow is passing from C3 through S4, S8 to output terminal as shown in Fig. 2(d). So, the 1× function can be achieved with the help of C3.

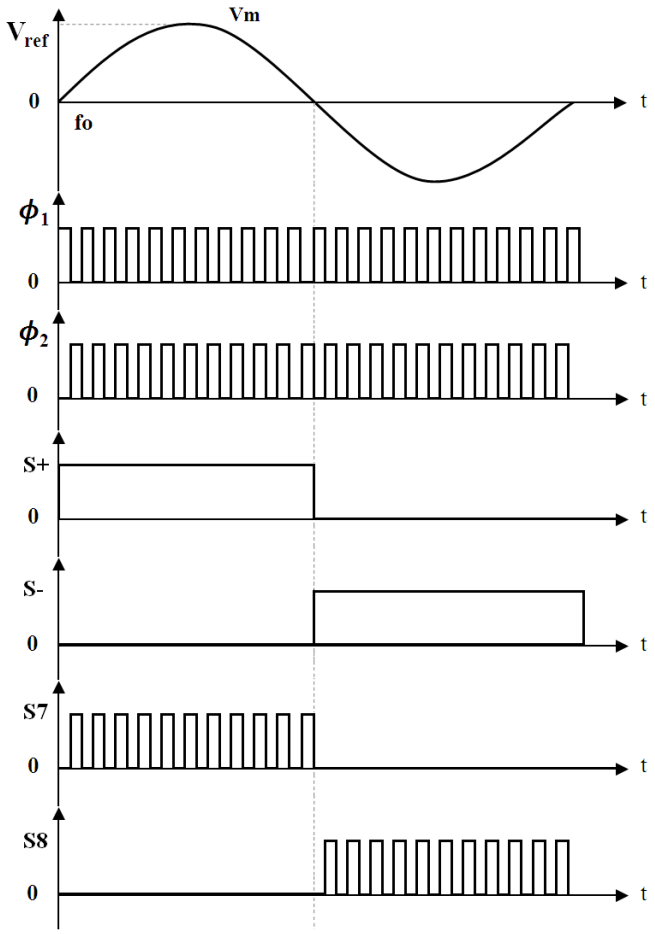

Fig. 3. Theoretical waveforms of phase generator (ϕ_1 : S1 ; ϕ_2 : S2, S3).

B. *Control Part*

In the 7-level SC boost DC-AC inverter, the SPFM-based controller is used as shown in lower of Fig. 1. The controller is composed of SPFM block and phase generator. Form signal flow, V_{out} is sent into the SPFM block, and after the operation of absolute value, V_{out} is compared with the desired output signal V_{ref} (sinusoidal reference) to obtain a control signal V_c as:

If $|V_{ref}| \geqq |V_{out}|$, then $V_c = 1$,
If $|V_{ref}| < |V_{out}|$, then $V_c = 0$.

Next, according to V_c and $|V_{ref}|$, the 3x/2x/1x selector as in Fig. 4 can select a boosting control signal (S6, S5, or S4) for a proper gain level, and its PFM rule is shown as below:

1) If $|V_{ref}| \geqq \frac{2}{3} V_{dd}$ and $V_c = 0$, then S6=0.
2) If $|V_{ref}| \geqq \frac{2}{3} V_{dd}$ and $V_c = 1$, then S6=1.
3) If $\frac{1}{3} V_{dd} \leqq |V_{ref}| < \frac{2}{3} V_{dd}$ and $V_c = 0$, then S5=0.
4) If $\frac{1}{3} V_{dd} \leqq |V_{ref}| < \frac{2}{3} V_{dd}$ and $V_c = 1$, then S5=1.
5) If $0V \leqq |V_{ref}| < \frac{1}{3} V_{dd}$ and $V_c = 0$, then S4=0.
6) If $0V \leqq |V_{ref}| < \frac{1}{3} V_{dd}$ and $V_c = 1$, then S4=1.

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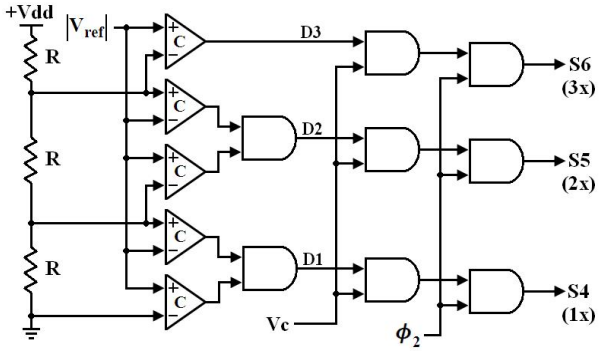

Fig. 4. 3x/2x/1x selector control circuit.

TABLE I COMPONENTS OF 7-LEVEL SC BOOST DC-AC INVERTER

Supply source (V_s)	5V
Pumping capacitor (C1~C3)	10uF
Output capacitor (Co)	0.2uF
Power MOSFETs	MbreakN (W=3m, L=18n)
On-state resistor of MOSFETs	24mΩ
Diode (D)	SD41
Load resistor (R_L)	500Ω
Switching frequency (f_s)	100kHz
Output frequency (f_o)	1.2 kHz, 1kHz, 0.8kHz

Using digital logic gates, the phase generator can be easily designed to obtain a set of non-overlapping complementary signals ϕ_1 and ϕ_2. Based on ϕ_1 and ϕ_2, the control signals S1-S3, S7 and S8 can be operated just like the waveforms in Fig. 3. Here, all detailed Boolean relationships of S1-S8 are shown as follows: (" • ": logic AND).

S1= ϕ_1,

S2=S3= ϕ_2,

S4= (ϕ_2 • D1 • V_c),

S5= (ϕ_2 • D2 • V_c),

S6= (ϕ_2 • D3 • V_c),

S7= (ϕ_2 • S^+),

S8= (ϕ_1 • S^-).

The goal is to generate these SPFM control signals S1-S8 for realizing phase I-II topologies as in Fig. 2.

III. EXAMPLE OF 7-LEVEL SC BOOST DC-AC INVERTER

In this paper, a closed-loop 7-Level SC boost DC-AC inverter with SPFM control is simulated by OrCAD, and then the results are illustrated to verify the efficacy of the proposed inverter scheme. All the parameters are listed in Table I. There are 3 cases (f_o=1.2 kHz, 1 kHz, and 0.8 kHz) to be discussed as follows.

1) Case 1: f_o=1.2 kHz

a) Vm=15V:

Let the supply source Vs be DC 5V, load R_L be 500Ω, and the peak value and output frequency of V_{ref} are Vm=15V, fo=1.2kHz. The waveform of V_{out} is obtained as in Fig. 5(a). V_{out} has the peak value of 14.777V, and the practical output frequency is about 1.2 kHz. The efficiency is 73.36%, and THD is 7.46%.

b) Vm=12V:

Let the supply source Vs be DC 5V, load R_L be 500Ω, and the peak value and output frequency of V_{ref} are Vm=12V, fo=1.2kHz. The waveform of V_{out} is obtained as in Fig. 5(b). V_{out} has the peak value of 12.78V, and the practical output frequency is about 1.2 kHz. The efficiency is 62.97%, and THD is 7.02%.

2) Case 2: f_o=1 kHz

a) Vm=15V:

Let the supply source Vs be DC 5V, load R_L be 500Ω, and the peak value and output frequency of V_{ref} are Vm=15V, fo=1kHz. The waveform of V_{out} is obtained as in Fig. 5(c). V_{out} has the peak value of 14.778V, and the practical output frequency is about 1 kHz. The efficiency is 73.91%, and THD is 5.85%.

b) Vm=12V:

Let the supply source Vs be DC 5V, load R_L be 500Ω, and the peak value and output frequency of V_{ref} are Vm=12V, fo=1kHz. The waveform of V_{out} is obtained as in Fig. 5(d). V_{out} has the peak value of 12.779V, and the practical output frequency is about 1 kHz. The efficiency is 63.57%, and THD is 6.47%.

3) Case 3: f_o=0.8 kHz

a) Vm=15V:

Let the supply source Vs be DC 5V, load R_L be 500Ω, and the peak value and output frequency of V_{ref} are Vm=15V, fo=0.8kHz. The waveform of V_{out} is obtained as in Fig. 5(e). V_{out} has the peak value of 14.777V, and the practical output frequency is about 0.8kHz. The efficiency is 75.45%, and THD is 4.69%.

b) Vm=12V:

Let the supply source Vs be DC 5V, load R_L be 500Ω, and the peak value and output frequency of V_{ref} are Vm=12V, fo=0.8kHz. The waveform of V_{out} is obtained as in Fig. 5(f). V_{out} has the peak value of 12.775V, and the practical output frequency is about 0.8kHz. The efficiency is 64.87%, and THD is 4.85%.

According to the above results, it is obvious that V_{out} is following V_{ref} for the different output peaks and frequencies. These results show that this 7-level SC boost inverter has a good closed-loop steady-state performance.

IV. CONCLUSION

A closed-loop 7-level SC boost DC-AC inverter is proposed by using the SPFM controller for low-power step-up inversion and regulation. Finally, the closed-loop SC boost inverter is simulated by OrCAD, and all results are illustrated to show the efficacy of the proposed scheme. The advantages of the scheme are listed as follows.

1) This SC-based inverter needs no large magnetic element. Thus, the IC fabrication is promising.
2) Here, the 3x/2x/1x selector inside this controller is presented to select a proper gain according to the desired output voltage so as to improve the THD, especially for the lower desired voltage.

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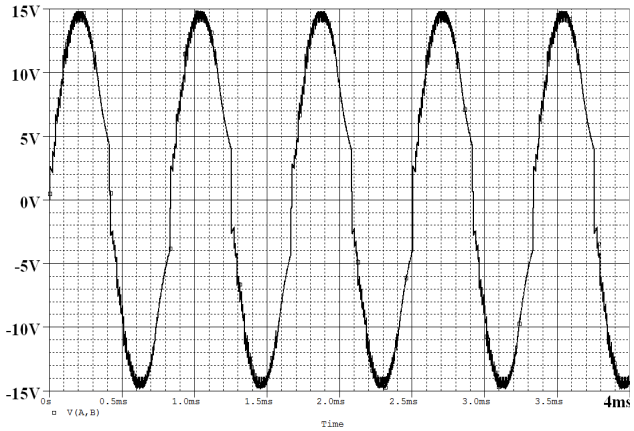

Fig. 5(a). Vout (V_{ref} : Vm=15V, fo=1.2kHZ).

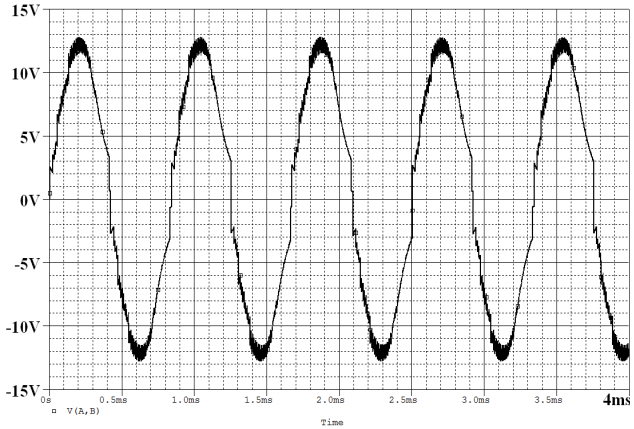

Fig. 5(b). Vout (Vref : Vm=12V, fo=1.2kHZ).

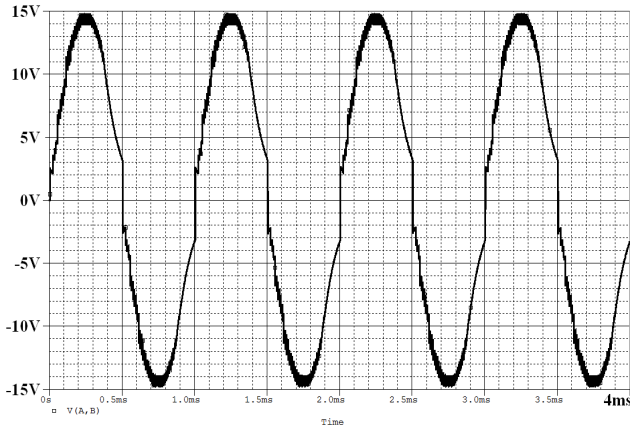

Fig. 5(c). Vout (Vref : Vm=15V, fo=1kHZ).

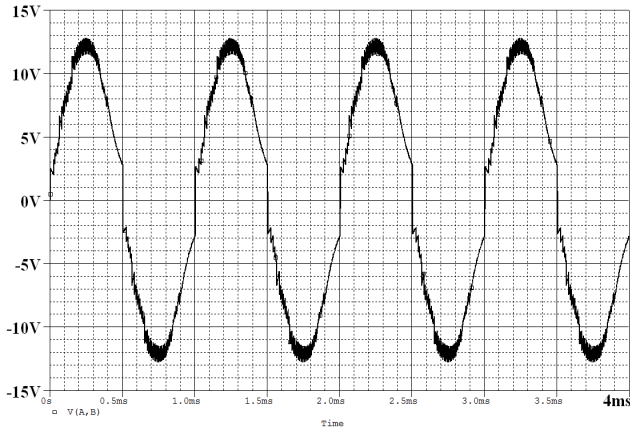

Fig. 5(d). Vout (V_{ref} : Vm=12V, fo=1kHZ).

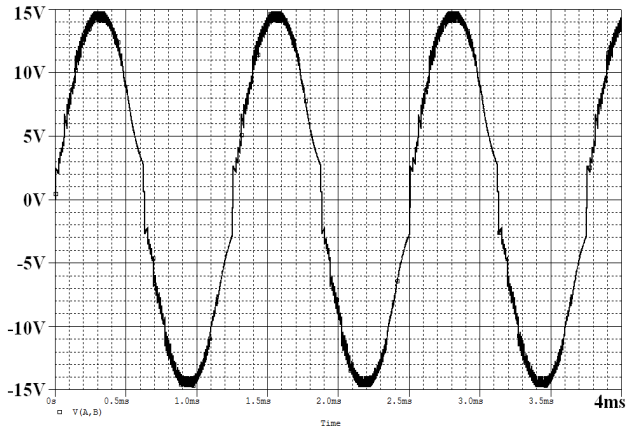

Fig. 5(e). Vout (V_{ref} : Vm=15V, fo=0.8kHZ).

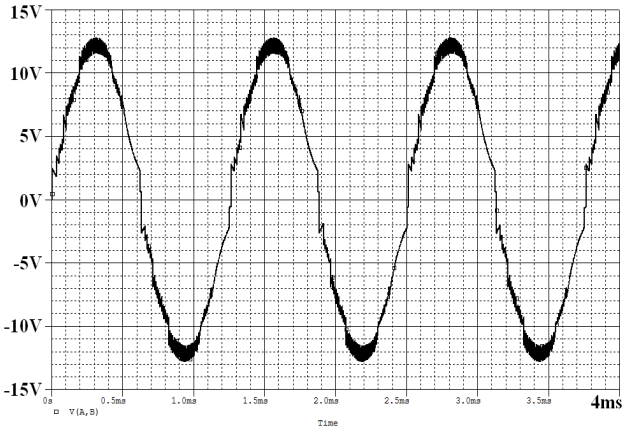

Fig. 5(f). Vout (V_{ref} : Vm=12V, fo=0.8kHZ).

3) The SPFM control is adopted in order to enhance output regulation capability for the various outputs (output peak value or output frequency).

At present, we have implemented the hardware circuit of the 7-level SC boost DC-AC inverter as the photo in Fig. 6, where the circle-marked chip (I.C. number: D35-101BE-36e, technology: TSMC 0.35μm 2P4M, 300×350μm², 1.8064 mW, max. frequency: 100 kHz) is implemented for this SPFM controller via full-custom fabrication of National Chip Implementation Center (CIC), NSC, Taiwan. Next, some more experimental results will be measured for the verification of this proposed inverter.

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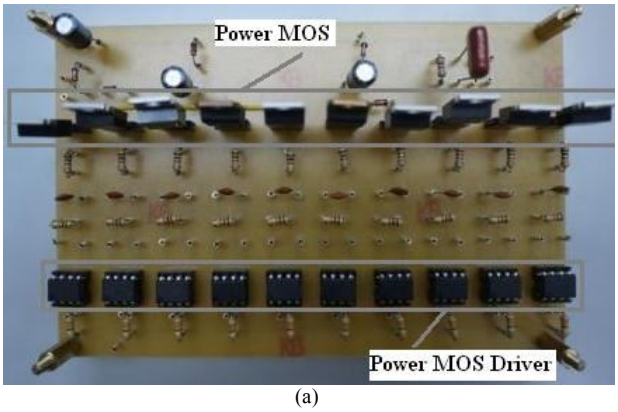
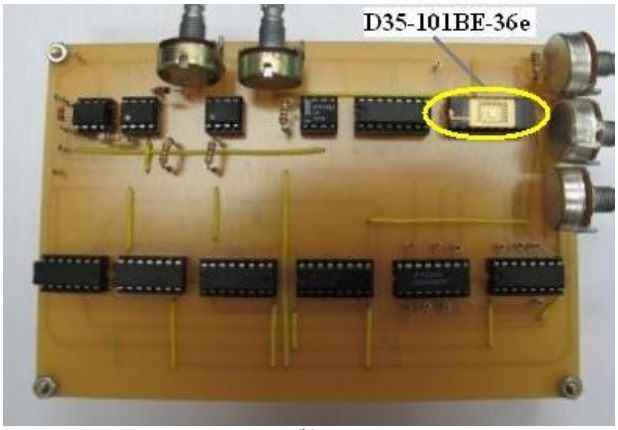


(a)



(b)

Fig. 6. 7-level SC boost DC-AC inverter containing (a) power part, (b) control part.

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