SIFO Voltage-Mode Biquadratic Filter Using DDCCTAs and Grounded Passive Elements

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***Abstract*— In this paper, a single-input five-outputs (SIFO) biquadratic active voltage filter with high-input impedance is proposed. The proposed circuit is based on using differential difference current conveyor transconductance amplifier (DDCCTA). It employs three DDCCTAs as active element together with one grounded resistors and two grounded capacitors as passive elements. The circuit also has the advantage of high-input impedance terminal, the simultaneous realization of lowpass, bandpass, highpass, bandstop and allpass voltage responses from the same topology and low sensitivity performance. PSPICE simulation results are included using 0.5 μm MIETEC CMOS technology parameters.**

***Index Terms*— Differential Difference Current Conveyor Transconductance Amplifier (DDCCTA), voltage-mode circuit,**

I. Introduction

RECENTLY, a relatively new active building block, the so-called differential difference current conveyor transconductance amplifier (DDCCTA), was introduced [1]. The DDCCTA device is realized by the combination of the differential difference current conveyor (DDCC) and the transconductance amplifier (TA) in monolithic chip for compact implementation of analog function circuits. This device provides the possibility of in built electronic tuning of the parameters of the analog function circuits to be implemented, and also has all the good properties of the DDCC, such as high-input impedance, employs fewer active and passive components, and easy implementation of differential and floating input circuits. Thereafter several different applications of the DDCCTA have been presented in the technical literature, particularly from the area of frequency filters [1]-[4].

In this paper, an electronically tunable voltage-mode biquadratic filter with one high input impedance and five output terminals employing three DDCCTAs and three grounded passive elements is described. With respect to similar type of the previously published single-input five-output voltage-mode universal filters in [5]–[14], the proposed circuit offers the following advantageous features :

(i) It realizes all the five standard biquadratic filtering functions, namely, lowpass (LP), bandpass (BP), highpass (HP), bandstop (BS) and allpass (AP) responses simultaneously from the same topology.

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(ii) All passive elements are grounded, which is advantageous in integrated circuit implementation.

(iii) The natural angular frequency (ω_0) and the quality factor (Q) are electronically controllable through the transconductance parameter (g_m) of the DDCCTA.

(iv) It does not require component matching conditions.

(v) It has high-input impedance, which can be directly connected in cascade to realize high-order filters.

(vi) It has low sensitivity performance.

II. Differential Difference Current Conveyor Transconductance Amplifier (DDCCTA)

The DDCCTA element is based on the use of the DDCC as an input stage and the TA as an output stage. As shown in Fig.1, the port characteristics of the DDCCTA can be described by the following expressions :

$$i_{Y1} = i_{Y2} = i_{Y3} = 0,\ v_X = v_{Y1} - v_{Y2} + v_{Y3},\ i_Z = i_X,\ i_O = g_m v_Z \tag{1}$$

where g_m is the transconductance parameter of the DDCCTA.

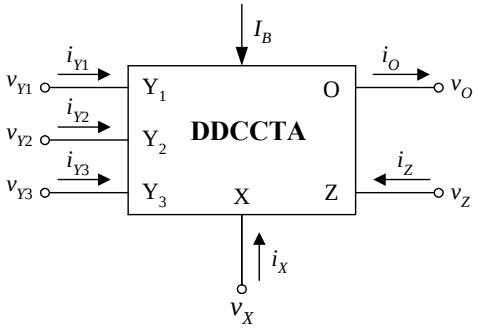

Fig. 1 Electrical symbol of the DDCCTA.

The internal structure of the DDCCTA in CMOS technology is shown in Fig.2. The scheme is based on the internal circuit of the DDCC [15], which is followed by a TA [16]. In this case, the transconductance gain (g_m) of the DDCCTA can be given by :

$$g_m = \sqrt{\mu C_{ox} \frac{W}{L} I_B} \tag{2}$$

where I_B is an external DC bias current, μ is the effective channel mobility, C_{ox} is the gate-oxide capacitance per unit area, W and L are channel width and length, respectively. It should be noted that the g_m-value of the DDCCTA can be adjustable electronically by I_B.

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III. Proposed Filter

Fig.3 shows the proposed voltage-mode biquadratic filter with one input terminal and three output terminals using three DDCCTAs and a canonical number of passive elements (one resistor and two capacitors). It can be seen that the input of the proposed filter is applied to the Y_1 terminal of the DDCCTA. Therefore, the circuit has the advantage of high-input impedance. Since all the passive components are grounded, it is therefore suitable for integrated circuit implementation point of view. Routine circuit analysis yields the following voltage transfer functions of the proposed filter in Fig.3 as :

$$HP = \frac{V_{HP}(s)}{V_{in}(s)} = \frac{s^2}{s^2 + \frac{s}{R_1C_1} + \frac{g_{m1}}{R_1C_1C_2}} \quad (3)$$

$$BP = \frac{V_{BP}(s)}{V_{in}(s)} = \frac{\frac{s}{R_1C_1}}{s^2 + \frac{s}{R_1C_1} + \frac{g_{m1}}{R_1C_1C_2}} \quad (4)$$

$$LP = \frac{V_{LP}(s)}{V_{in}(s)} = \frac{\frac{g_{m1}}{R_1C_1C_2}}{s^2 + \frac{s}{R_1C_1} + \frac{g_{m1}}{R_1C_1C_2}} \quad (5)$$

$$BS = \frac{V_{BS}(s)}{V_{in}(s)} = \frac{s^2 + \frac{g_{m1}}{R_1C_1C_2}}{s^2 + \frac{s}{R_1C_1} + \frac{g_{m1}}{R_1C_1C_2}} \quad (6)$$

and

$$AP = \frac{V_{AP}(s)}{V_{in}(s)} = \frac{s^2 - \frac{s}{R_1C_1} + \frac{g_{m1}}{R_1C_1C_2}}{s^2 + \frac{s}{R_1C_1} + \frac{g_{m1}}{R_1C_1C_2}} \quad (7)$$

It should be noted from eqs.(3)-(7) that all the five standard biquadratic filter functions are simultaneously realized from the proposed circuit. Also note that there is no need of any component-matching constraints for all filter response realizations.

The natural angular frequency (ω_0), and quality factor (Q) of this filter are obtained as :

$$\omega_0 = \sqrt{\frac{g_{m1}}{R_1C_1C_2}} \quad (8)$$

and

$$Q = \sqrt{\frac{g_{m1}R_1C_1}{C_2}} \quad (9)$$

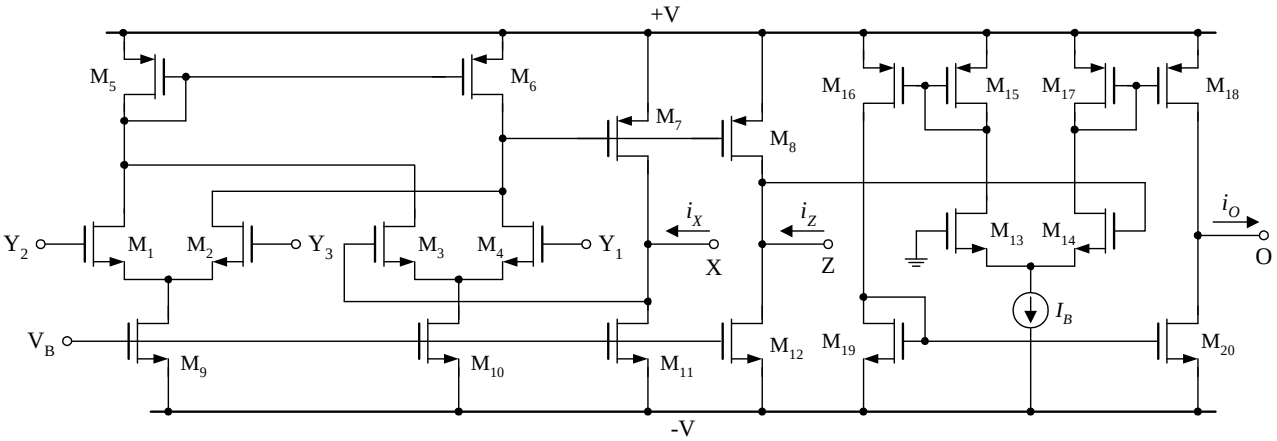

Fig.2 : CMOS implementation of the DDCCTA.

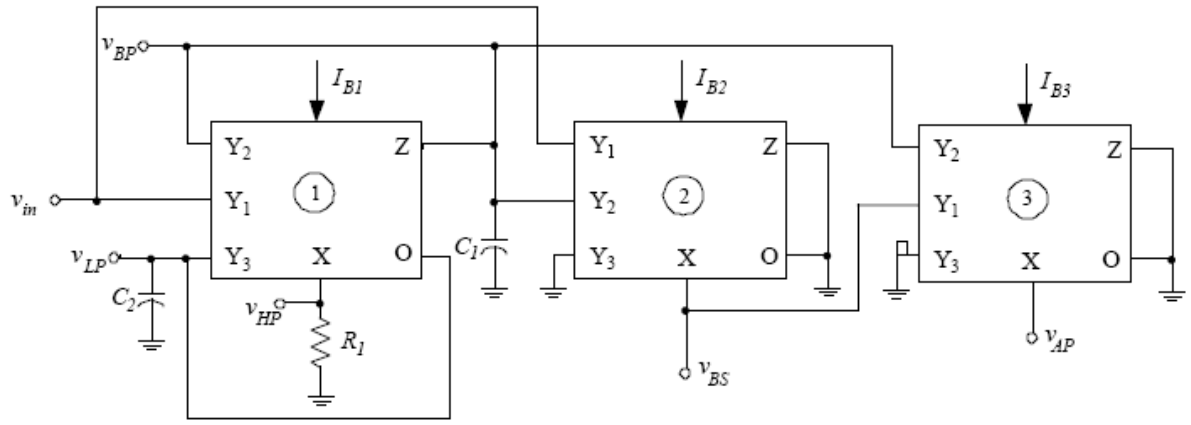

Fig.3 : Proposed voltage-mode biquad filter.

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Eqs. (8) and (9) show that the parameters ω_0 and Q for all the filter responses can electronically be tuned by g_{m1}. For the fix-valued capacitors, the ω_0 can be adjusted arbitrarily without disturbing Q by simultaneously changing g_{m1} and R_1 and keeping the product $g_{m1}R_1$ constant. On the other hand, the parameter Q can be tuned without disturbing ω_0 by simultaneously increasing g_{m1} and R_1 and keeping g_{m1}/R_1 constant.

IV. Non-ideal Analysis

Taking into consideration the DDCCTA non-idealities, the port characteristics in eq. (1) can be rewritten as :

$$v_X = \beta_1 v_{Y1} - \beta_2 v_{Y2} + \beta_3 v_{Y3},\ i_Z = \alpha i_X,\ i_O = g_m v_Z \qquad (10)$$

where and $\beta_k = 1 - \varepsilon_{vk}$ for k =1, 2, 3 and $\alpha = 1 - \varepsilon_i$. Here, ε_{vk} ($|\varepsilon_{vk}| << 1$) and ε_i ($|\varepsilon_i| << 1$) represent the voltage and current tracking errors of the DDCCTA, respectively. Thus, re-analysis of the proposed circuit in Fig.3 yields the non-ideal parameters as follows :

$$\omega_0 = \sqrt{\frac{\beta_{31}\alpha_1 g_{m1}}{R_1 C_1 C_2}} \qquad (10)$$

and

$$Q = \frac{1}{\beta_{21}}\sqrt{\frac{\beta_{31} g_{m1} R_1 C_1}{\alpha_1 C_2}} \qquad (11)$$

where β_{ki} and α_i are the parameters β_k and α of the i-th DDCCTA (i = 1, 2, 3), respectively. It is important to note that the active and passive sensitivities of ω_0 and Q in eqs. (10) and (11) are found to be within unity in magnitude. This means that the proposed filter is low-sensitivity performance.

V. Computer Simulation Results

To verify theoretical analysis, the proposed single DDCCTA-based voltage-mode universal filter of Fig.3 has been simulated with PSPICE program using MIETEC 0.5 μm CMOS technology process parameters. The DDCCTA was performed by the CMOS structure given in Fig.2 with supply voltages of +V = -V = 2 V, and V_B = -1.22 V. The aspect ratios of CMOS transistors are chosen as : $(W/L)_{M1\text{-}M4}$ = 1.8μm/0.7μm, $(W/L)_{M5\text{-}M6}$ = 5.2μm/0.7μm, $(W/L)_{M7\text{-}M10}$ = 20μm/0.7μm, $(W/L)_{M11\text{-}M12}$ = 58μm/0.7μm and $(W/L)_{M13\text{-}M20}$ = 4μm/1.0μm.

The filter is designed to realize LP, BP and HP responses with $f_0 \cong \omega_0/2\pi$ = 1.6 MHz and Q = 1. For this purpose, the active and passive components are chosen as : $g_m \cong$ 100 μA/V (I_B = 16 μA), R_1 = 10 kΩ and $C_1 = C_2$ = 10 pF. The simulated responses comparing with the ideal responses are illustrated in Fig.4. Figs.5 and 6 also show the simulated and ideal gain and phase responses of the BS and AP filters, respectively. From the results, it can be observed that the simulation results agree very well with theoretical predictions.

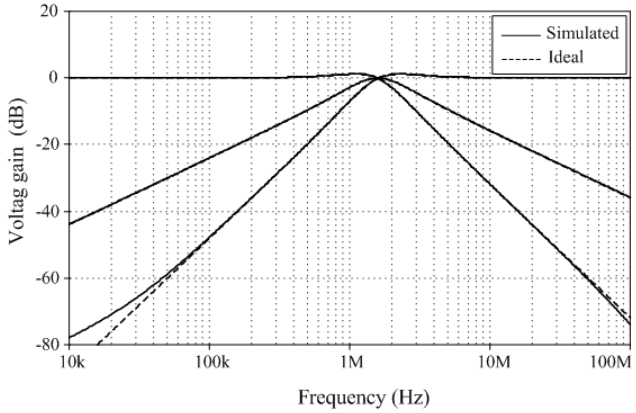
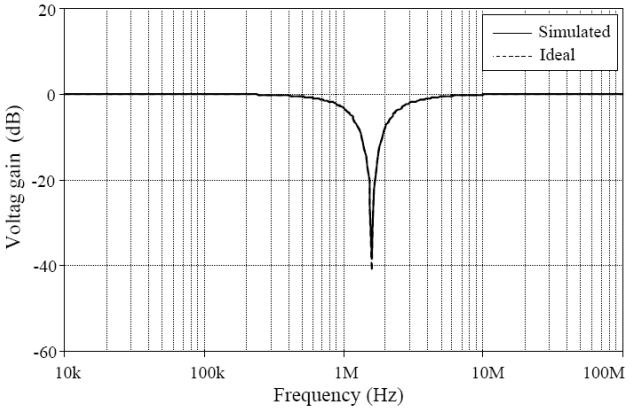
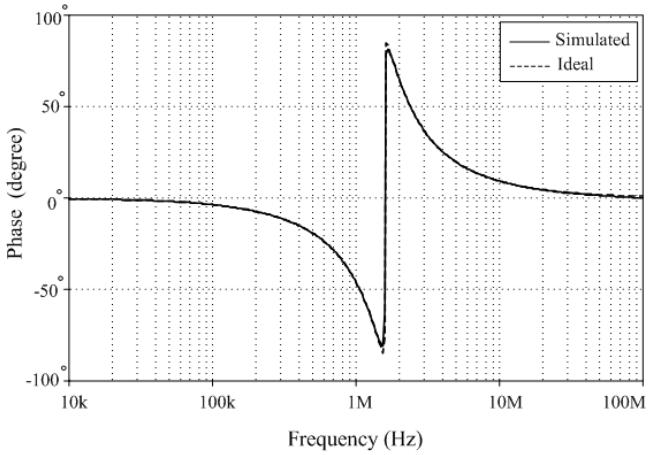


Fig.4 : Ideal and simulated frequency responses of LP, BP and HP for the proposed filter in Fig.3.



(a)



(b)

Fig.5 : Ideal and simulated frequency responses of the BS filter.
(a) gain response (b) phase response

In order to investigate a time-domain response of the proposed voltage-mode universal filter, a 1.6 MHz sinusoidal input voltage with 200 mV peak is applied to the filter. The results obtained are shown in Fig.7. The variation of total harmonic distortion (THD) with the amplitude of input signal is shown in Fig.8. The THD (%) is found low within 2% for a wide amplitude variation.

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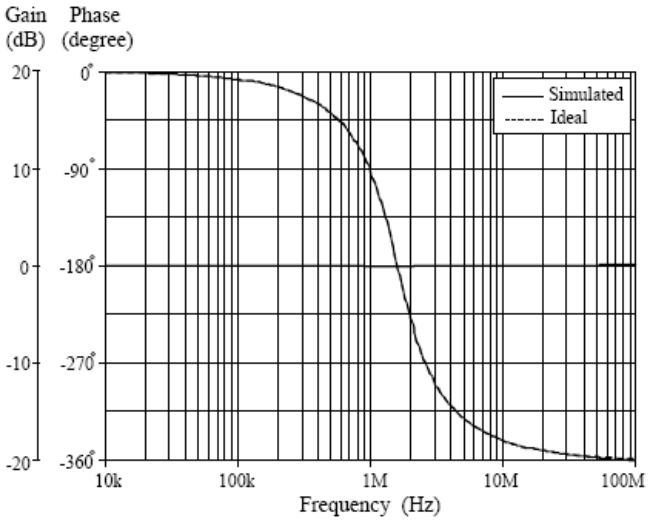

Fig.6 : Ideal and Simulated frequency responses of the AP filter.

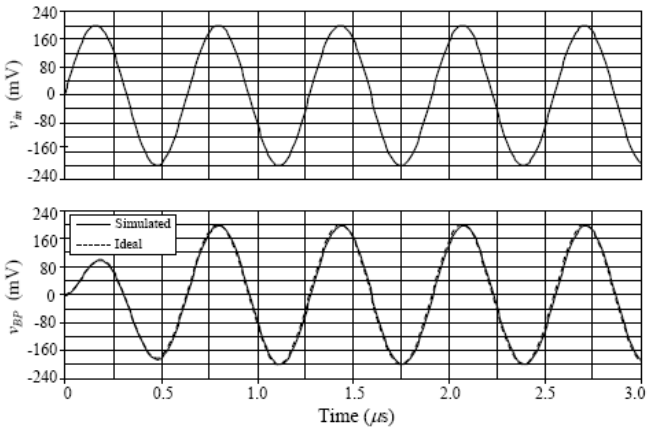

Fig.7 : Time domain response of the BP filter for a 200 mV (peak) sinusoidal input voltage at 1.6 MHz.

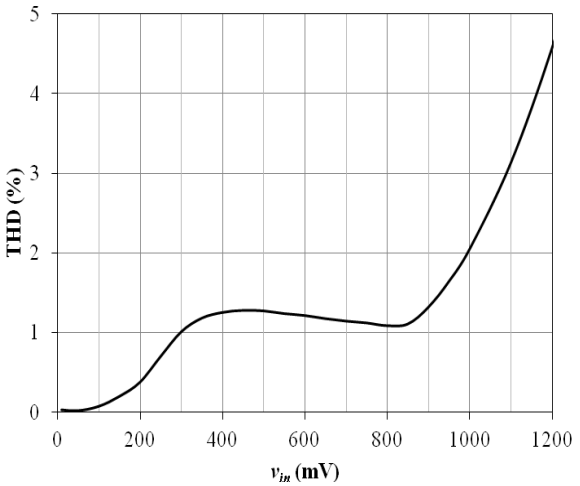

Fig.8 : THD variation of the BP filter versus amplitudes of an applied sinusoidal voltage signal at 1.6 MHz.

VI. Conclusion

A single-input five-output voltage-mode biquad filter for simultaneously realize LP, BP, HP, BS and AP responses without changing the configuration has been presented. The presented circuit uses three DDCCTAs, one grounded resistor and two grounded capacitors, which is a canonical structure and suitable for integration. It has high-input impedance, and exhibits electronic controllability of both ω_0 and Q through the bias current of the DDCCTA. Also, no critical component matching conditions are required. Both its active and passive sensitivities are low.

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