# High-Gain Switched-Inductor Switched-Capacitor Step-Up DC-DC Converter

Yuen-Haw Chang and Yu-Jhang Chen

***Abstract*—A closed-loop scheme of high-gain switched-inductor switched-capacitor step-up DC-DC converter (SISCC) is proposed by using a phase generator and pulse-width-modulation-based (PWM-based) gain compensator for step-up DC-DC conversion and regulation. In the power part of SISCC, there are two cascaded sub-circuits including: (i) pre-stage: a two-stage serial-parallel switched-capacitor (SC) circuit, and (ii) core-stage: two switched-inductor (SI) resonant boosters in parallel. In the pre-stage SC circuit, it provides at most 3 times voltage of source Vs for supplying the rear boosters. In the core-stage SI boosters, the step-up gain can reach to 2/(1-D), where D means the duty cycle of the MOSFET in SI. Theoretically, the SISCC can boost the output voltage Vo to 16 times voltage of Vs when D=0.67. Further, the PWM technique is adopted not only to enhance the output regulation for the compensation of the dynamic error between the practical and desired outputs, but also to reinforce output robustness against source or loading variation. Finally, the closed-loop SISCC is designed by OrCAD SPICE, and is simulated for some cases: steady-state and dynamic response (source/loading variation). All results are illustrated to show the efficacy of the proposed scheme.**

***Index Terms*— high-gain, switched-capacitor, switched-inductor, step-up converter, serial-parallel, resonant booster, pulse-width-modulation.**

## I. Introduction

In recent years, with the rapid development of power electronics technology, the step-up DC-DC converters are emphasized more widely for the electricity-supply applications, such as photovoltaic system, fuel cell, X-ray systems. General speaking, these power converters are always required for a small volume, a light weight, a high efficacy, and a better regulation capability.

Based on the structure of charge pump, an SC converter is one of the good solutions to low power and high gain DC-DC conversion. The advantage is that this kind of SC converter uses semiconductor switches and capacitors only. However, most SC circuits have a voltage gain proportional to the number of pumping capacitors. In 1976, Dickson charge pumping was proposed based on a diode-chain structure via pumping capacitors [1]. It provides voltage gain proportional to the stage number of capacitors, and the detailed dynamic model and efficiency analysis were discussed [2]. But, its drawbacks include the fixed voltage gain and the larger device area. In 1993, Ioinovici *et al.* suggested a voltage-mode SC with two symmetrical capacitor cells working complementarily [3]. In 1997, Zhu and Ioinovici performed a comprehensive steady-state analysis of SC [4]. In 2009, Tan *et al.* proposed a low-EMI SC by interleaving control [5]. In 2011, Chang proposed an integrated SC step-up/down DC-DC/DC-AC converter/ inverter [6]-[7]. However, the drawbacks of most SC converters are with more component count and more complicated circuit structure, especially as to extend the converter for the higher voltage gain.

Generally, a simple conventional booster consists of one magneticing inductor and one capacitor, and it can provide the voltage gain of 1/1-D. But, the inductor may result in electromagnetic interference (EMI) problem. Here, for the boost-type converters, there are some topologies introduced as follows. (i) The quadratic cascade boost converter can provide a high voltage gain and this gain is square times or higher than that of the simple booster [8]-[9]. (ii) Based on the scheme of the simple booster, the fly-back converter uses just one switch and coupled-inductors to achieve the high-gain conversion [10]-[11]. However, it often leads to the worst EMI problem due to the coupled-inductor. (iii) The diode-clamped step-up converter can provide the voltage gain proportional to the number of stage, which is able to be extended by adding capacitors and diodes [12]. But, it may result in the larger voltage-drop consumption due to cut-in voltage of the diodes in series.

Based on the above descriptions, for achieving a compromise among volume size, component count, and voltage gain, the SISCC is proposed here by combining the contents of [6],[13]-[14]. Further, the closed-loop high-gain step-up SISCC is proposed by using PWM-based gain compensator to enhance regulation capability and overall voltage gain can reach to the value of 3 x 2/(1-D).

## II. Configuration of SISCC

Fig. 1 shows the overall circuit configuration of SISCC, and it contians two major parts: power part and control part for achieving the closed-loop high-gain step-up DC-DC conversion and regulation.

### *A. Power part of SISCC*

The power part of SISCC is shown in the upper half of Fig. 1, and it consists of a two-stage serial-paraller SC circuit (front) and SI resonant boosters (rear) connected in cascade between source Vs and output Vo. The converter consists of one inductor (L), four switches ($S_1$-$S_4$), four

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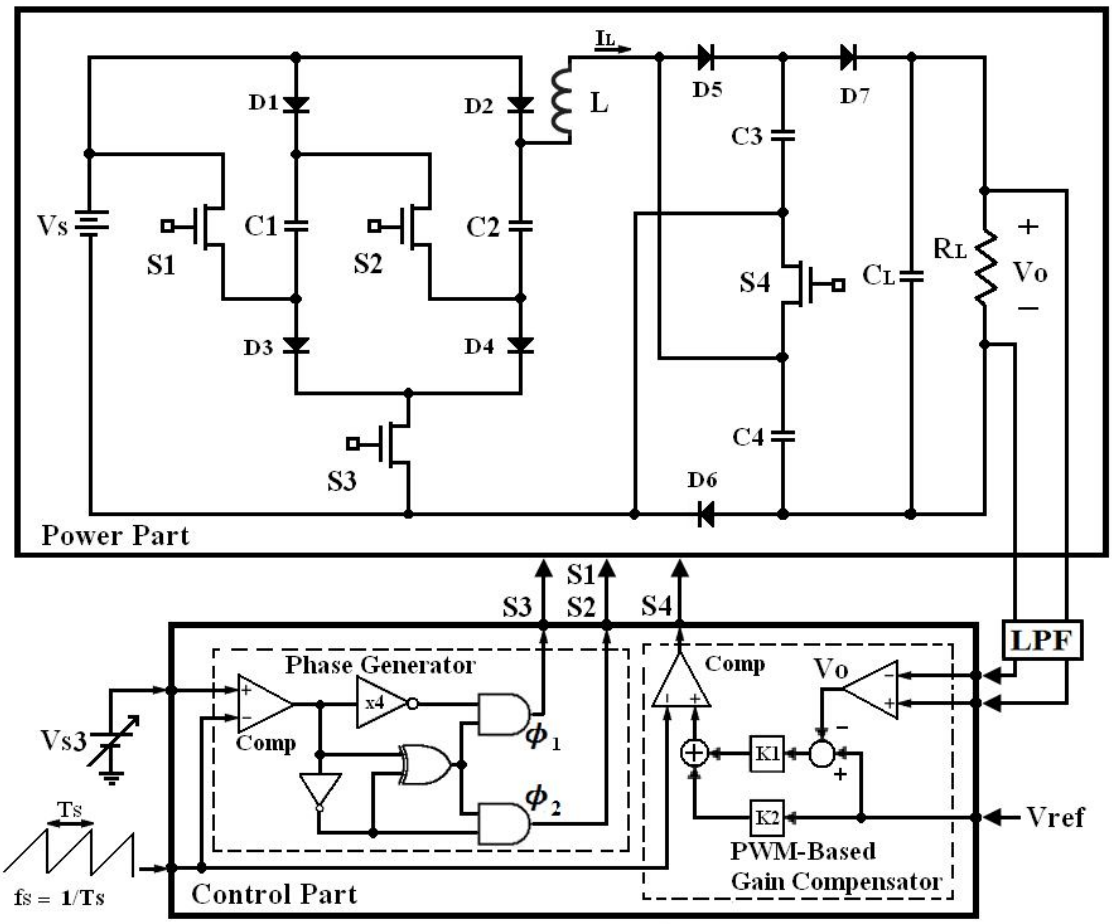


Fig. 1.Configuration of SISCC.

capacitors ($C_1$-$C_4$), one output capacitor ($C_L$) and 7 diodes, where each capacitor has the same capacitance C ($C_1$=$C_2$=$C_3$=$C_4$=C). Fig. 2 shows the theoretical waveforms of SISCC in a switching cycle $T_S$. Each $T_S$ contains three phases: Phase I, II, and III. The step-up function of this converter can be achieved by charging into capacitors or inductor in parallel and discharging from capacitors in series within these phases. The operations for Phase I, II, and III are described as follows.

(i) Phase I:

During this time interval, $S_3$, $S_4$, turn on, and $S_1$, $S_2$ turn off. Then, the diodes $D_1$-$D_4$, $D_7$ are on, and $D_5$ and $D_6$ are off. The current-flow path is shown in Fig. 3(a). The capacitors $C_1$, $C_2$ and magnetic inductor L are charged in parallel by source Vs. At the same time, capacitors $C_3$ and $C_4$ are discharged in series to supply the energy to $C_L$ and $R_L$.

(ii) Phase II:

During this time interval, $S_1$, $S_2$, $S_4$ turn on, and $S_3$ turns off. Then, $D_7$ is on and $D_1$-$D_6$ are off. The current-flow path is shown in Fig. 3(b). The capacitors $C_1$, $C_2$, are discharge in series with source Vs to charge in inductor L. At the same time, capacitors $C_3$, $C_4$ are discharged in series to supply the energy to $C_L$ and $R_L$.

(iii) Phase III:

During this time interval, $S_1$, $S_2$ turn on, and $S_3$, $S_4$, turn off. Then the diodes $D_5$-$D_7$ are on, and $D_1$-$D_4$ are off. The current-flow path is shown in

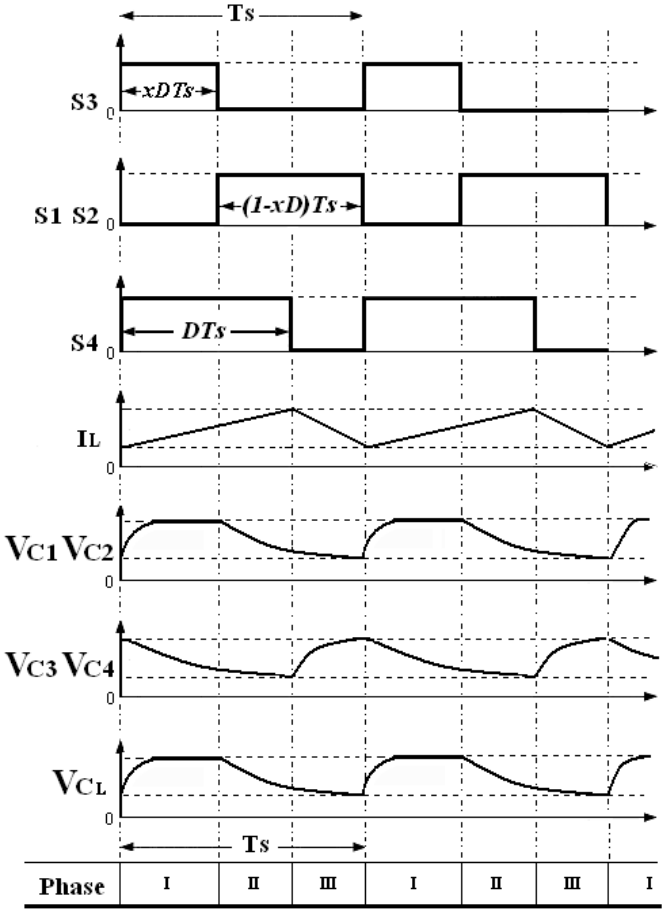


Fig. 2.Theoretical waveforms of SISCC

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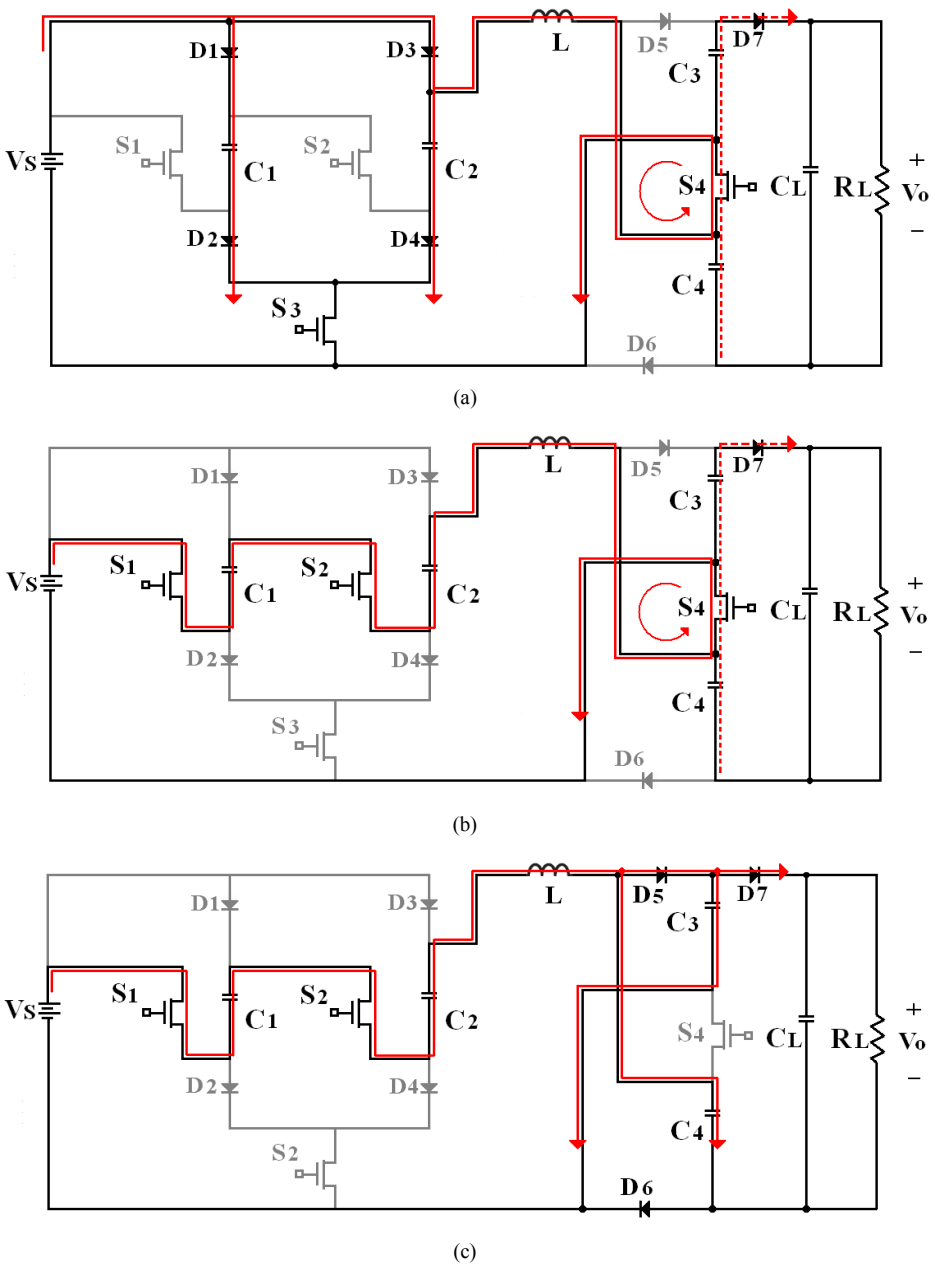


Fig.3. Topologies of SISCC for (a) Phase I, (b) Phase II, (c) Phase III.

Fig. 3(c). The source Vs, $C_1$, $C_2$ and L are connected in series to transfer the energy to capacitors $C_3$, $C_4$ in parallel. At the same time, these two capacitors $C_3$, $C_4$ in parallel are connected with $C_L$ and $R_L$ to transfer the energy.

Based on the cyclical operations of Phase I, II, and III, the overall step-up gain can reach to the value of 3x2/(1-D) theoretically. Extending the capacitor count, the gain can be boosted into the value of $(m+1)\times n/(1-D)$, where m and n are the number of pumping capacitors in the pre-stage and core-stage, respectively.

### *B. Control part of SISCC*

The control part of SISCC is shown in the lower half of Fig.1. It is composed of low-pass filter (LPF), PWM-based gain compensator, and phase generator. From the controller signal flow, the feedback signal Vo is sent into the OP-amp LPF for high-frequency noise rejection. Next, the filtered signal Vo is compared with the desired output reference

TABLE I
ALL COMPONENTS OF SISCC

| | |
|---|---|
| Supply source (Vs) | 5V |
| Pumping capacitor ($C_1$~$C_4$) | 30uF |
| Output capacitor ($C_L$) | 300uF |
| Inductor (L) | 470uF |
| Parasitic resistance of inductor | 0.1Ω |
| Switching frequency (fs) | 100kHz |
| Diodes : D1~D4,D7 / D5~D6 | 120NQ045 / D1N4148 |
| Power MOSFETs($S_1$~$S_4$) | MbreakN |
| On-state resistance of MOSFETs (Ron) | 0.03Ω |
| Load resistor ($R_L$) | 700Ω |
| Gain Compensation ($K_1$, $K_2$) | $K_1$ =20, $K_2$ =0.06 |

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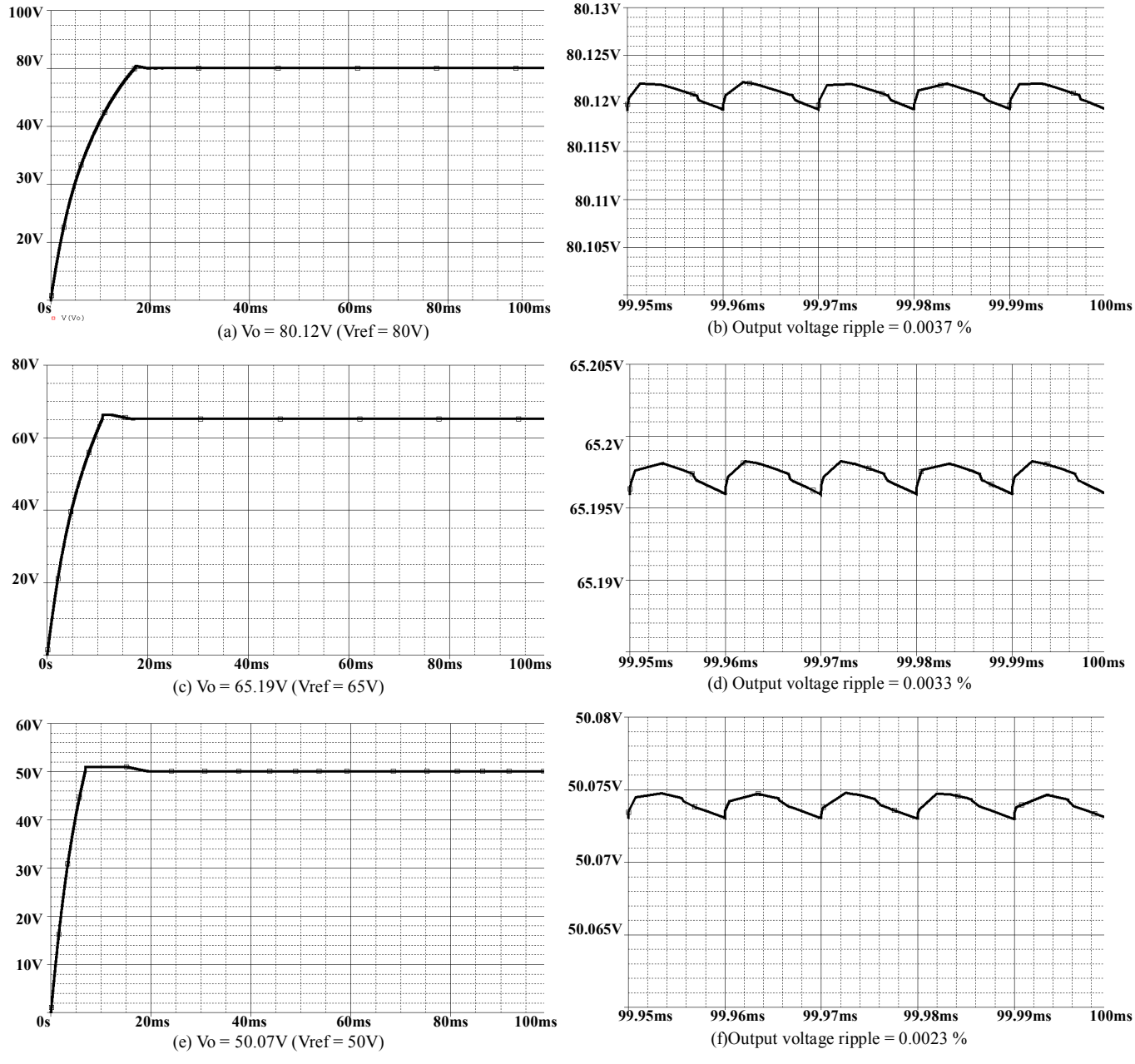
Vref. The correspond duty-cycle D can be produced via the gain compensator. The main function is to keep Vo on following Vref by using PWM duty-cycle adjustment of $S_4$. In the phase generator, firstly, an adjustable voltage Vs3 is compared with a ramp function to generate a flexible and non-symmetrical clock signal. And then, this clock is sent to the non-overlapping circuit for obtaining a set of non-overlapping phase signals $\phi_1$ and $\phi_2$ so as to produce the driver signals of $S_1$-$S_3$. Here the pre-charge time (xDTs of Phase I) can be adjusted by changing the DC value of Vs3, i.e. the rate x as in Fig. 2 can be regulated by Vs3. The main goal is to generate the driver signals of MOSFETs for the different topologies as in Fig. 3(a)-(c). In this paper, the closed-loop control will be achieved via the PWM-based gain compensator and phase generator in order to improve the regulation capability of this converter.

## III. EXAMPLES OF SISCC

In this section, based on Fig. 1, the closed-loop SISCC converter is designed and simulated by OrCAD SPICE tool. The results are illustrated to verify the efficacy of the proposed converter. The component parameters of the converter are listed in Table I. This converter is preparing to supply the load $R_L$=700Ω. For checking closed-loop performances, some cases will be simulated and discussed, including: (i) Steady-state response (ii) Dynamic response (source/loading variation).

(i) Steady-state response:

The closed-loop SISCC converter is simulated for Vref = 80V / 65V / 50V respectively, and then these output results are obtained as shown Fig. 4(a)-(b) / Fig. 4(c)-(d) / Fig. 4(e)-(f). In Fig. 4(a), it can be found that the settling time is about 20ms, and the steady-state value of $V_O$ is really reaching 80.12V, and converter is stable to keep $V_O$ following Vref (80V). In Fig. 4(b), the output ripple percentage is measured as rp = $\Delta vo/V_O$= 0.0037%, and the power efficiency is obtained as $\eta$= 89.6%. In Fig. 4(c), it




(a) Vo = 80.12V (Vref = 80V)

(b) Output voltage ripple = 0.0037 %

(c) Vo = 65.19V (Vref = 65V)

(d) Output voltage ripple = 0.0033 %

(e) Vo = 50.07V (Vref = 50V)

(f)Output voltage ripple = 0.0023 %

Fig. 4 Steady-state response of SISCC

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can be found that the settling time is smaller than 20ms, and the steady-state value of $V_O$ is really reaching 65.18V, and converter is stable to keep $V_O$ following Vref (65V). In Fig. 4(d), the output ripple percentage is measured as rp = $\Delta vo/V_O$= 0.0032%, and the power efficiency is obtained as $\eta$= 90.1%. In Fig. 4(e), it is found that the settling time is smaller than 20ms, and the steady-state value of $V_O$ is really reaching 50.07V, and converter is stable to keep $V_O$ following Vref (50V). In Fig. 4(f), the output ripple percentage can be easily found as rp = $\Delta vo/V_O$=0.0021%, and the power efficiency is obtained as $\eta$= 89.7%. These results show that this closed-loop SISCC has a high voltage gain and a good steady-state performance.

(ii) Dynamic response:

Since the voltage of battery is getting low as the battery is working long time, or the bad quality of battery results in the impurity of source voltage, such a source variation must be considered, as well as loading variation.

(a) Case I:

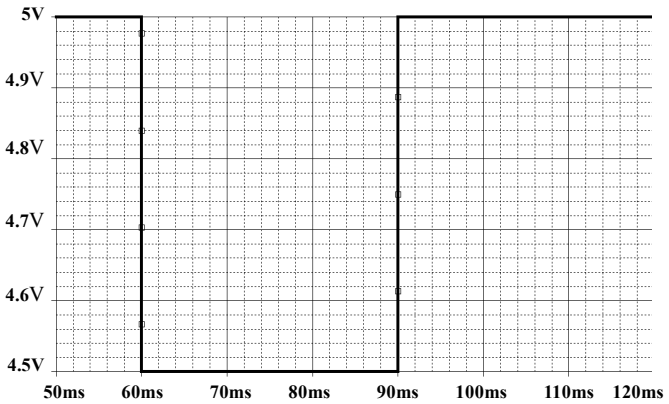
Assume that source voltage at DC 5.0V, and then it has a voltage instant variation: 5.0V→4.5V →5.0V as in Fig. 5(a). Obviously, $V_O$ is still keeping on about 54V (Vref=54V) as shown in Fig. 5(b), even though $V_S$ has the disturbance lower than standard source of 5.0V.

(b) Case II:

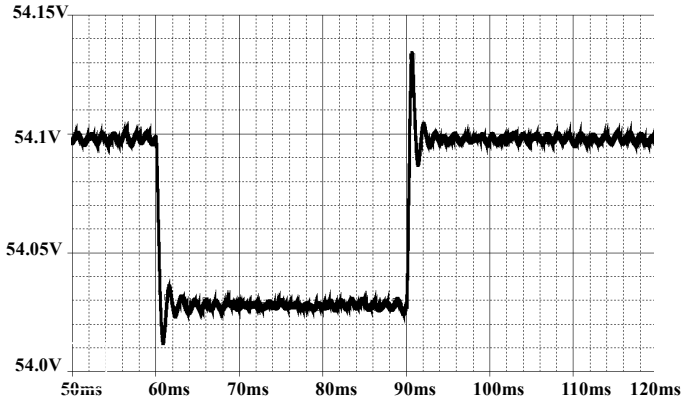
Assume that $V_S$ is the DC value of 5.0V and extra plus a sinusoidal disturbance of 0.4$V_{P-P}$ as in Fig. 5(c), and the waveform of $V_O$ is shown as in Fig. 5(d). Clearly, by using the closed-loop controller, $V_O$ is still keeping on Vref (62V) in spite of sinusoidal disturbance.

(c) Case III:

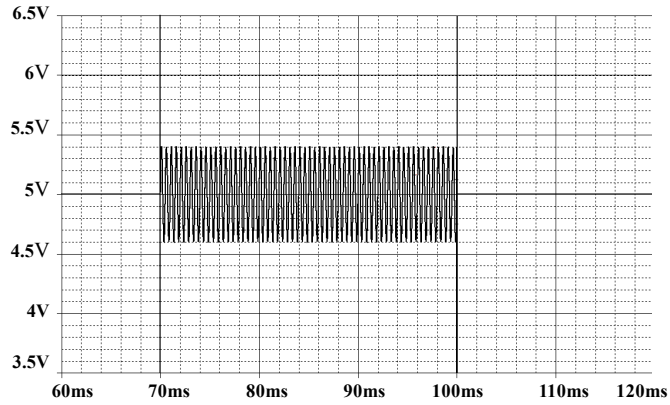
Assume that $R_L$ is 700Ω normally, and it



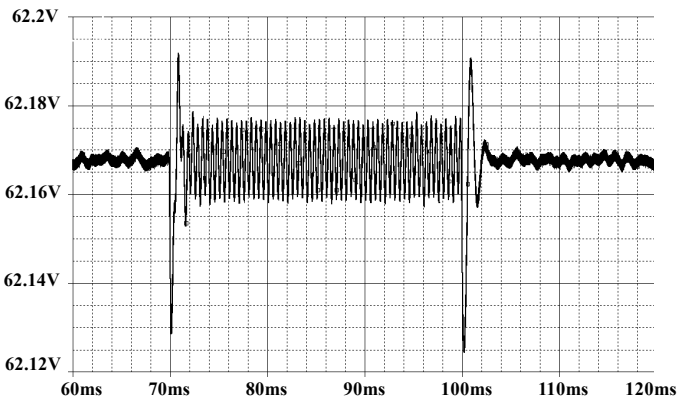

(a) Source: Vs = 5V→4.5V→5V



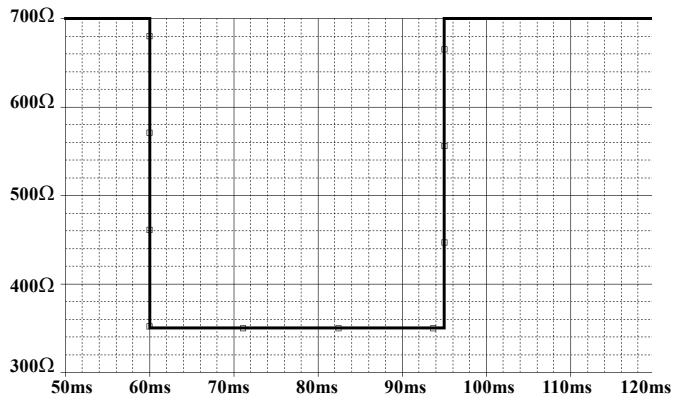

(b) Output: Vo (Vref = 54V)



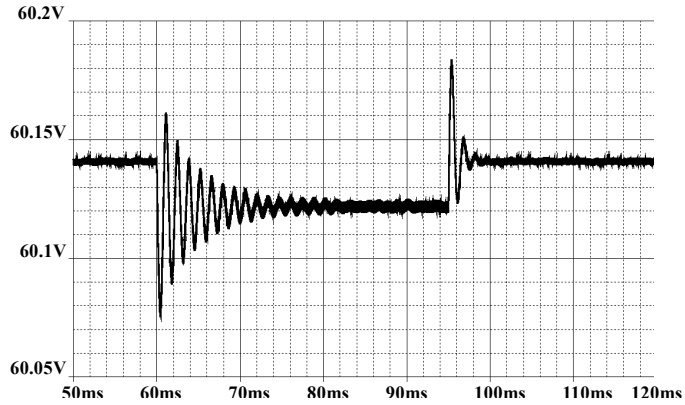

(c) Source: $V_S$=5+0.4sinwt V




(d) Output: Vo (Vref = 62V)




(e) Load: $R_L$=700Ω→350Ω→700Ω.




(f) Output: Vo (Vref = 60V)

Fig. 5 Dynamic response of SISCC

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changes from 700Ω to 350Ω. After a short period of 35ms, the load recovers from 700Ω to 350Ω, i.e. $R_L$=700Ω→350Ω→700Ω. Fig. 5(e) shows the transient waveform of $V_O$ at the moment of loading variations. It is found that $V_O$ has a small drop (0.1V) at $R_L$ : 700Ω→350Ω. The curve shape becomes thicker during the heavier load as in Fig. 5(f), i.e. the output ripple becomes bigger at this moment.

These results show that the closed-loop SISCC has the good output regulation capability to source/loading variations.

## IV. Conclusions

A closed-loop scheme of SISCC is presented by using a phase generator and PWM-based gain compensator for step-up DC-DC conversion and regulation. The advantages of the proposed scheme are listed as follows. (i) In the SISCC, the large conversion ratio can be achieved with four switches and five capacitors for a step-up gain of 16 or higher. (ii) In this SISCC circuit, we used 7 diodes to replace MOSFETs so that the complexity of circuit implementation can be reduced much. (iii) As for the higher step-up gain, it can be easily realized through extending the number of stages (i.e. pumping capacitors). (iv) The PWM technique is adopted here not only to enhance output regulation capability for the different desired output, but also to reinforce the output robustness against source/loading variation. At present, the prototype circuit of this converter is implemented in the laboratory as shown in the photo of Fig. 6. Some experimental results will be obtained and measured for the verification of the proposed converter.

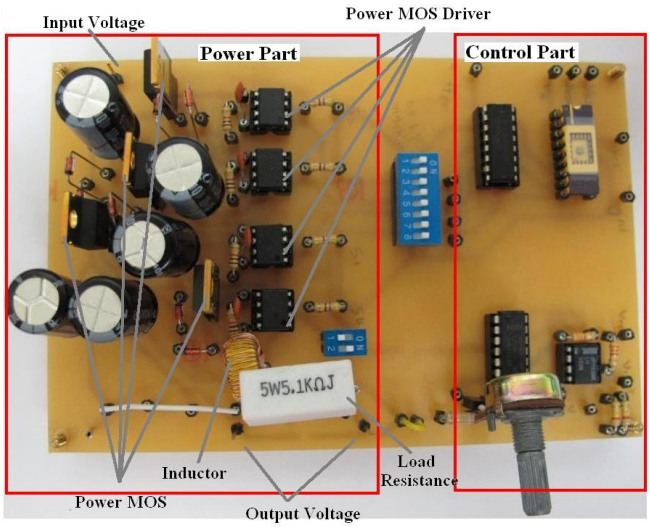


Fig. 6 Prototype circuit of SISCC

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