Hardware-Software Co-Simulation of Downlink LTE-Based Transceiver

Rih-Lung Chung*, Po-Hao Chang

***Abstract*—In this paper, we employ the hardware-software co-simulation scheme to implement some critical blocks of the LTE downlink transceiver in the frequency division duplexing (FDD) mode. We adopt the Simulink® and System Generator® tools for rapid prototyping the system. First, we design a packet control circuit in the LTE's transmitter end to generate control signal of the transmitted signal frame. According to the control signal, synchronization signals, modulated data, and cyclic-prefix (CP) signals can be arranged in the right time duration. We then implement pseudo-noise binary generator and quadrature-phase-shift keying (QPSK) symbol-mapping circuits, and use the inverse fast-Fourier transform (IFFT) module of the System Generator® to generate orthogonal frequency-division-multiplexing-access (OFDMA) signal. Next, we design CP-insertion circuit to generate guard-interval signals. In the receiver end, we implement CP-removing circuit, and use the FFT module for realizing the downlink LTE's demodulator. Finally, we employ the software-defined radio (SDR) platform to verify the correctness of the downlink LTE-based system.**

Index Terms*— *LTE downlink, OFDMA, System Generator, WARP software-defined radio platform

I. Introduction

The long term evolution (LTE) is the technique proposed by the third Generation Partnership Project (3GPP) and is designed for the fourth generation (4G) mobile communication systems. In the downlink LTE system, the orthogonal frequency division multiplexing access (OFDMA) is adopted as the physical layer technique to improve the transmission data rates.

Firstly, the OFDMA modulates a stream of data on different parallel orthogonal subcarriers. In so doing, the data rates can be improved significantly. Secondly, by adding the cyclic prefix (CP) prior to transmitted OFDMA signal, it can protect the information data from the harmful effects occurred by the multipath channel. Thirdly, the data rates of the OFDMA can be link adaptation according to the quality of the feedback channel state information.

In this paper, we aim to implement some critical blocks of the LTE downlink transceiver in the frequency division duplexing (FDD) mode [1-3]. We employ the hardware-software co-simulation scheme for designing communication algorithm and use WARP software defined radio (SDR) [10] as the hardware verification platform.

*Corresponding author: Rih-Lung Chung is with Department of Electronic Engineering, Chung Yuan Christian University, Chungli City, 32023, Taiwan. He is now an Assistant Professor in Department of Electronic Engineering. (e-mail: rlchung @cycu.edu.tw).

Po-Hao Chang is with Chung Yuan Christian University, Chungli City, 32023, Taiwan, He is now pursuing the master degree in the master program in Communication Engineering. (e-mail: g10079026@cycu.edu.tw).

Besides, we use the System Generator® of Xilinx for rapid prototyping the downlink LTE system. First, we use the MATLAB/Simulink® software to simulate transmitter and receiver algorithms of LTE downlink in the accuracy of floating points. Next, we use the System Generator® to simulate the transceiver algorithms in the accuracy of fixed points, and then use the Embedded Development Kit (EDK) tool of the Xilinx ISE design suite to generate bit stream file. Finally, we download the bit stream file to the Xilinx Virtex-4 digital signal processor of the WARP platform for hardware verification.

The remaining parts of the paper are organized as follows. Section II describes the LTE downlink structure. Section III introduces the signal frame structure of the LTE downlink of FDD mode. In Section IV, we use System Generator® to design critical blocks of the LTE downlink transceiver. In Section V, simulation and analysis results are included. Finally, concluding remarks are made in Section VI.

II. The LTE Downlink Structure

In this paper, we construct the downlink LTE transceiver according to the 3GPP LTE specification [1-3], which is plotted in Fig. 1.

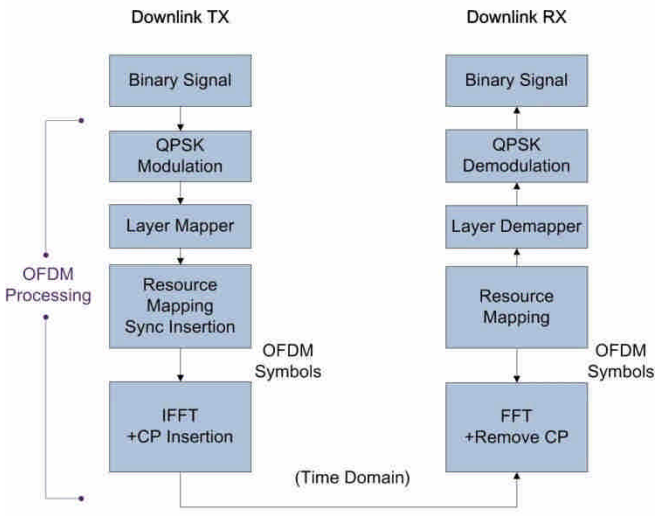

Fig. 1 LTE physical layer downlink model.

In the transmitter end, we adopt the pseudo noise (PN) binary sequence generator to generate random binary sequence, and then map the binary sequences to the quadrature-phase-shift-keying (QPSK) symbols. In this paper, we aim to implement the single-input single-output (SISO) transceiver, and thus we omit the antenna-port mapping building block. Next, the synchronization signals

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are added after symbol mapping to make transmitter and receiver synchronized. Finally, we take inverse fast-Fourier-transform (IFFT) operator on the QPSK symbols to generate the OFDMA signal. Besides, we also add the long enough cyclic prefix (CP) prior to the OFDMA signal to prevent the harmful effect of multipath channels. The CP length can be set according to the distance between the user equipment (EP) and base-station. In the receiver end, we assume that the timing offset is perfectly estimated. We first remove the CP, and then take FFT operator the received signal for transform the time-domain signal into the frequency-domain signal.

III. LTE's Signal Frame Structure of FDD Mode

The LTE physical layer (PHY layer) defines frequency division duplex (FDD) and time division duplexing (TDD) modes for data transmission [1-3]. In this paper, we adopt FDD-LTE for hardware implementation.

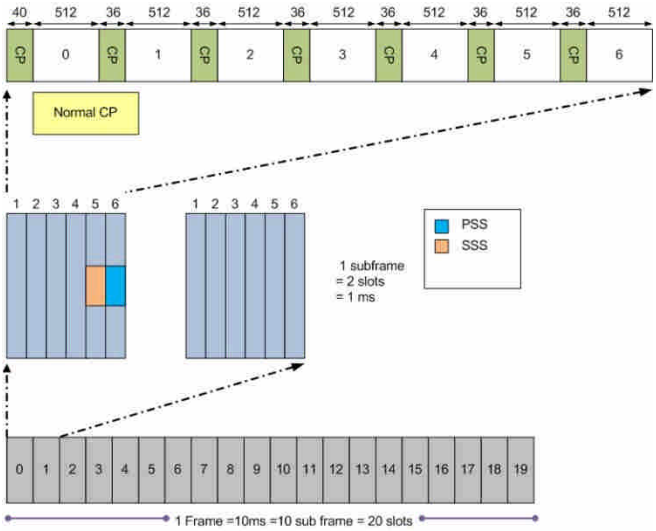

Fig. 2 Signal frame structure of LTE downlink in the normal CP mode.

According to the 3GPP-LTE specification [1-3], the resource block (RB) is the basic element for data transmission. In the downlink LTE, a signal frame consists of ten sub-frames, and one sub-frame consists of two time slots, as shown in Fig. 2. Besides, there are two types of CPs; they are normal CP (NCP) and extended CP (ECP). The former is composed by six OFDMA signals and the latter is composed by seven OFDMA signals. In this paper, we adopt NCP type.

As for synchronization signals, there are primary synchronization signals (PSS), and secondary synchronization signals (SSS). As shown in Fig. 2, the PSS is in the sixth OFDMA symbol on the zeroth and tenth time slots. The SSS is in the fifth OFDMA symbol on the zeroth and tenth time slots [4].

IV. LTE Downlink System Design Flow

The 3GPP-LTE PHY defines six physical channels, including three resource channels and three control channels [1-3]. In this paper, we study and implement on the resource channels, i.e., physical downlink shared channel (PDSCH), which aims to transmit data. The block diagram of the PDSCH is plotted in Fig. 3.

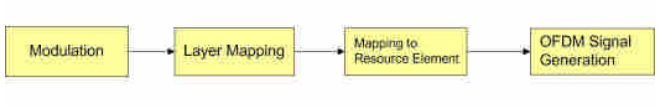

Fig. 3 The design flow for LTE PDSCH system model.

The functionalities of the PDSCH are defined as follows [7].

1. The binary PN sequence is as the transmitted data for PHY layer.
2. The binary PN sequence is then symbol mapping to the QPSK symbols
3. Arrange the QPSK signals on the pre-defined signal frame structure.
4. Add the synchronization signals on the SS frame.
5. Take the IFFT operation on the QPSK signals to generate OFDMA symbol.
6. Add CP prior to the OFDMA symbol.

The primary parameters of LTE downlink system used in this paper are listed in Table I.

TABLE I.
The Parameters of LTE Downlink System

Parameter	Assumption
Channel Bandwidth	5 MHz
Number of Physical Resource Blocks	25
Number of subcarriers	300
Frame Structure	FDD (type I)
Cyclic Prefix type	Normal CP
Subcarrier spacing	15KHz
Subcarrier frequency in a Resource block	180KHz
Number of OFDM symbols per sub frame	14
Number of antennas	1 (SISO)
Modulation	QPSK

In what follows, we introduce the designs of the LTE downlink systems block-by-block [6].

A. *Packet Control Circuits*

The design of the packet control circuits aims to put the synchronization and data signals on the pre-defined signal frame. Packet control circuits are made of logic modules, and are represented Boolean signals. In this paper, we design the packet control circuits to present signal frame the LTE downlink system. As shown in Fig. 4, one OFDMA symbol of the downlink LTE has CP, direct current (DC), two RBs, and two blocks of zeros. Fig. 4 shows the 512-points OFDMA symbol have two 150-points RBs to be put information data. In this paper, we have to design two different OFDMA symbols with different CP-length signals

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for putting RB's data. In the NCP OFDMA, the NCP is composed by one 40- points CP and six 36-points CPs. To design more easily, we first design 40-points CP and 36-points CP individually, and then combine both CPs into one NCP. Therefore, the length of OFDMA symbol after adding CP, has 552 points and 548 points, respectively.

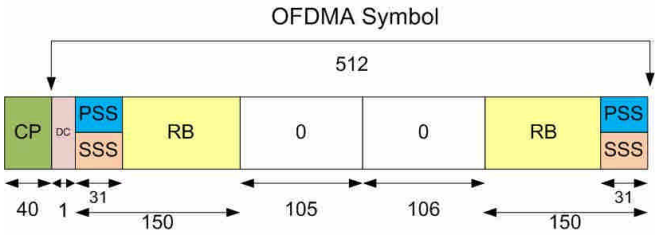

Fig. 4. Frequency-domain signal frame structure of the OFDMA symbol.

B. Synchronization Signals

The synchronization signals used in the LTE have two types, including primary synchronization signals (PSS), and secondary synchronization signals (SSS). The PSS is located at the sixth OFDMA symbol on the zeroth and the tenth time slots, and the PSS is length-31 complex-valued signal. The SSS is located at the fifth OFDM symbol on the zeroth and the tenth time slots, and the SSS is length-31 real-valued signal.

In the hardware design, the first work is to design the period of SS, where the period is in the duration of seven OFDMA symbols. Next, we then put the two synchronization signals into the zeroth and the fifth sub-frames. Besides, because only real-valued signals are permitted in the hardware implementation, the complex-valued signal PSS should be first separated as real part and imaginary part signals and then be put in the pre-defined signal frame, as shown in Fig. 5.

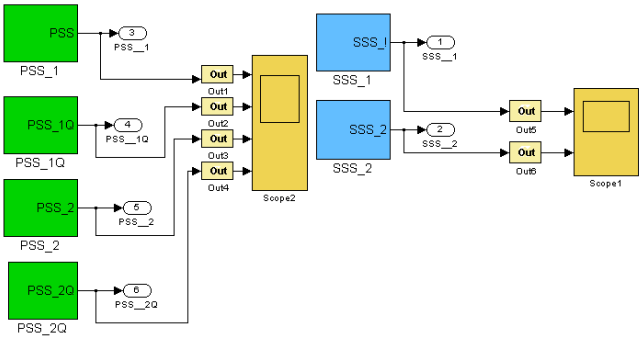

Fig. 5 SS mapping circuit design by using System Generator®.

C. QPSK Modulator and IFFT Operator

In what follows, we introduce the generation of QPSK signals. We first use the binary PN sequence as the input signal to the serial-to-parallel (S/P) circuit, in which the S/P circuit is designed to transform the two-bits binary signal into one quaternary signal. Next, we use the quaternary signals as the input of the selector, and mapped the signals into QPSK symbols [5]. The whole procedure is plotted in Fig. 6

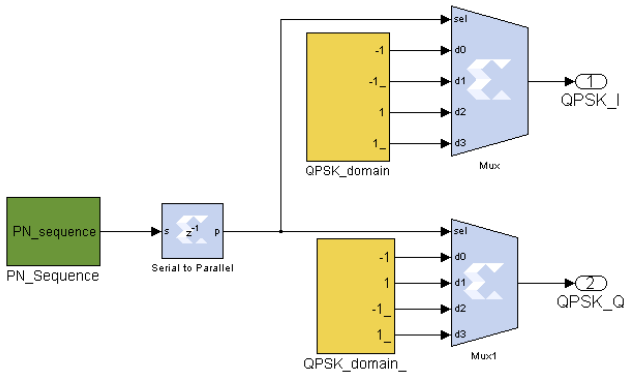

Fig. 6 QPSK design flow by using System Generator®.

Here, we use the "To FIFO" module, as shown in Fig. 7, to put the QPSK signals only in the RB's subcarriers, and to insert zeros in the null subcarriers. This is because that by using the "To FIFO" the signals can be first be written in the memory, and then be read out only in the addresses of RB's subcarriers. After generating QPSK signals, we may perform the built-in IFFT module of system generator on them to generate OFDMA signals. It is should be noted that we must design the "start" signal three clocks prior to the timing of input signals of the IFFT, which is shown in Fig. 8. For the OFDMA symbol is generated periodically, and thus the "start" signal must be produced periodically.

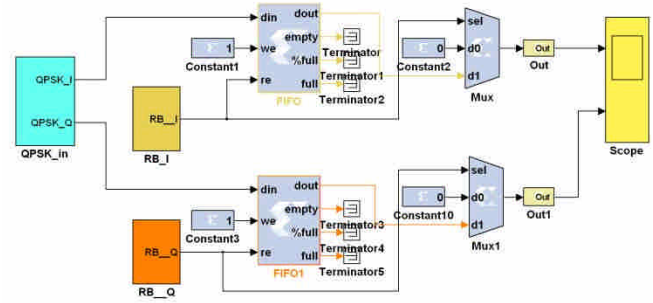

Fig. 7 Putting signal in the addresses of RB by using "FIFO".

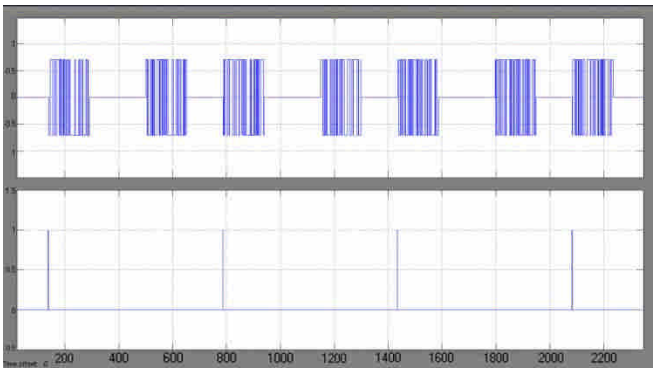

Fig. 8 The "start" signal design of the IFFT module.

D. Cyclic Prefix (CP) Module

In this subsection, we use dual-port RAM to insert CP prior to the OFDMA signal. Because the LTE downlink has two CPs with different length, we use two dual-port RAMs. Then we combine these two signals to the one signal frame, as shown in Fig. 9.

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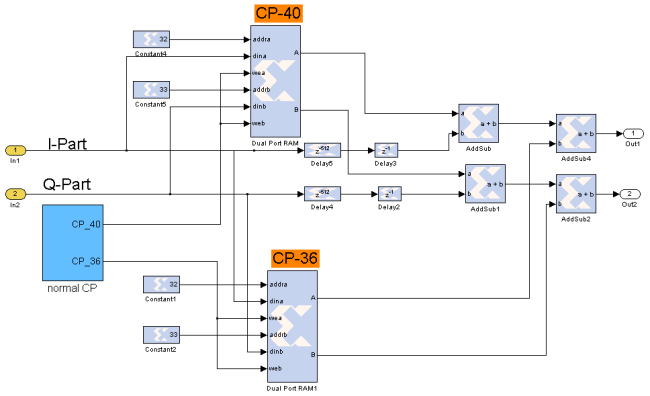

Fig. 9. The CP design by using System Generator®.

E. The Receiver Module

In the receiver end, we assume that the starting position of the OFDMA signal is known, and therefore the received signal can exactly be put in to the FFT module through the correct design of the "start" signal of the FFT module. In so doing, the correct demodulation is done, as shown in Fig. 10.

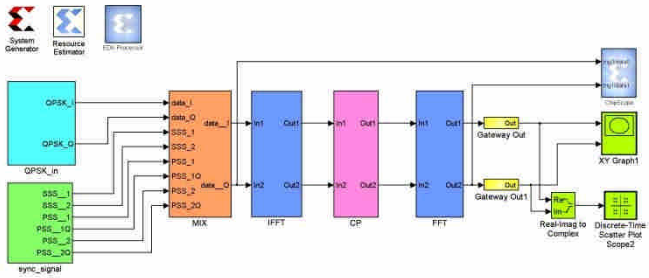

Fig. 10. The whole system design by using System Generator®.

F. Design of "start" Signal of the FFT

Fig. 11 plots the design of "start" signal of the FFT used in the receiver. It should be noted that the propagation delay of the IFFT and CP modules in the transmitter should be considered, and thus the FFT module can be correctly performed. In our design, the propagation delays of the IFFT and the CP are represented by 1132 and 514 clock durations, respectively.

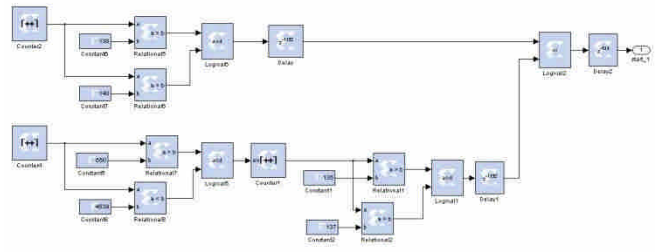

Fig. 11. The "Start" signal design by using System Generator®.

V. Simulation and Analysis Results

In this paper, we use WARP software defined radio (SDR) platform for hardware verification. This platform includes the oscillator of 100 MHz, and one Virtex-4 FX100, and thus can support our design [8-10]. Table II shows the requirements of hardware complexities. From top to down, the table lists the used number of slices, flip-flops (FFs), the look-up table (LUT), the input/output blocks (IOB), the embedded multipliers, and tristate buffers (TBUFs), respectively. The percentage of the used slices is 39%.

TABLE II.
The Used System Resource

Parameter	Usage
Slices	16527/42176(39%)
Slices Flip-Flops	18512/84352(22%)
LUT's(Look up Table)	23174/84352(27%)
IOB(Input /Output blocks)	275/768(36%)
Embedded Mults (Embedded multipliers)	57
TBUFs(Tristate Buffers)	0

Fig. 12 to Fig. 14 shows the simulation results. After removing the CP of the time-domain received signal and then passing the CP-removing signal into the FFT module, the signal demodulation result in the case without noise is shown in Fig. 12. From the figure, it can be seen that the received signal can be correctly demodulated. Fig. 13 shows the comparison between the imaginary part of the transmitted signal before the IFFT and the imaginary part of the demodulated signal after the FFT to verify the correctness of our design by using System Generator®. From the figure, we can observe that transmitted data and demodulated data are the same. It can be also seen that there is time lag between the transmitter and receiver signals. This time lag primarily comes from the processing time of the IFFT and FFT. Finally, Fig. 14 shows the hardware verification result by using the WARP SDR platform and the EDK software. We use the Chipscope of System Generator® to view logic signals of the transmitter and receiver signals. The figure is composed by three parts. Fig. 14(a) shows the signal of the packet control, Fig. 14(b) shows the logic signals of the transmitted signals, and Fig. 14(c) shows the logic signals of the demodulated signals. Comparing the results of the Fig. 14(b) and Fig. 14(c), it can be observed that both of the logic signals are the same, and thus the correctness of the hardware circuit is verified.

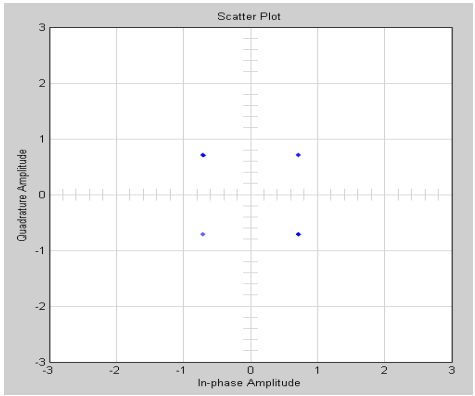

Fig. 12 Demodulated signal in the case without noise.

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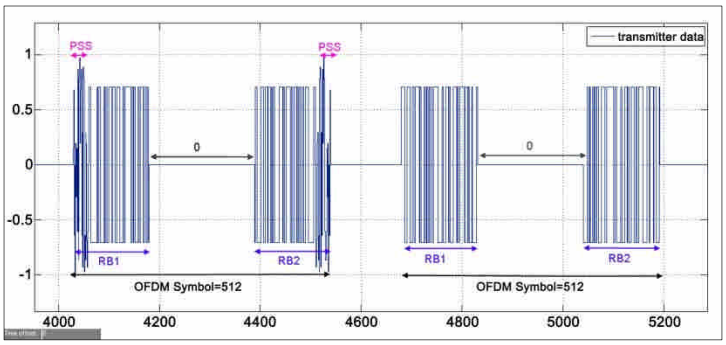
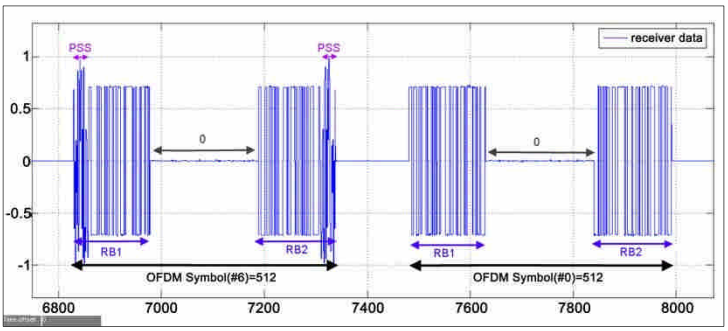
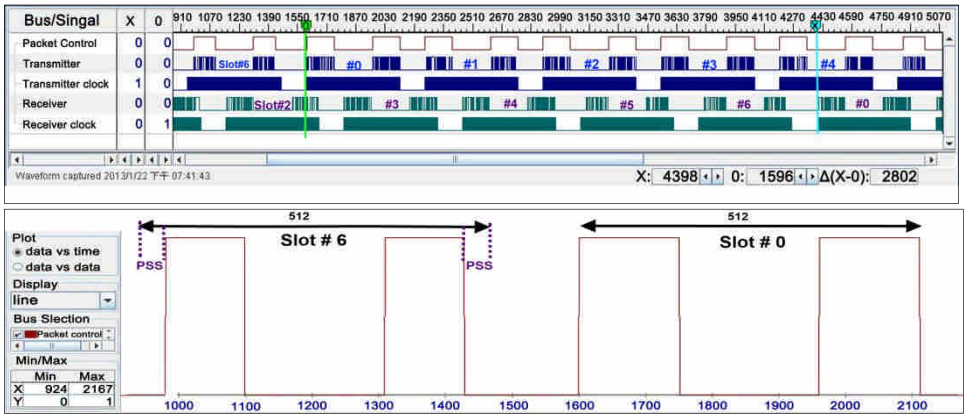


(a) Imaginary part of the transmitted signal.

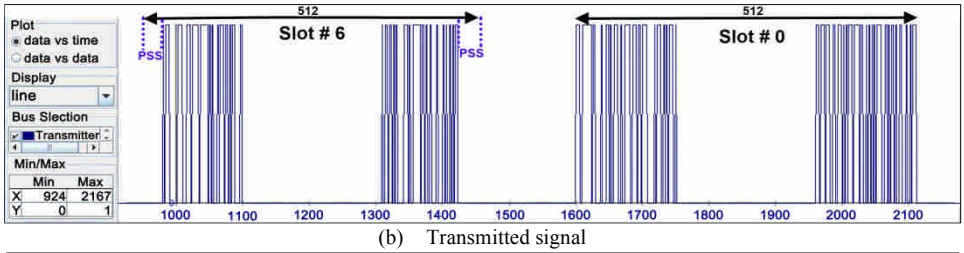


(b) Imaginary part of the demodulated signal.

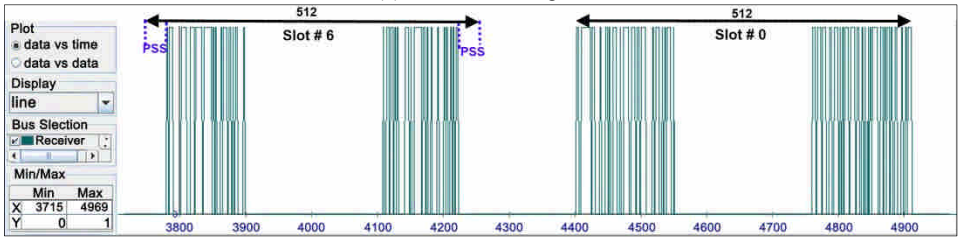
Fig. 13 Comparison between imaginary part of the transmitted signal and the imaginary part of the demodulated signal by using System Generator®, (a) transmitted signal and (b) demodulated signal.



(a) Packet control signal



(b) Transmitted signal



(c) Demodulated signal

Fig. 14. Comparison between the imaginary part of the transmitted signal and the imaginary part of the demodulated by using Chipscope, (a) Packet control signal (b) transmitted Signal, and (c) demodulated signal.

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VI. CONCLUSIONS

In this paper, we employed the MATLAB/Simulink® software and the building blocksets of System Generator® to implement the critical PDSCH circuits of the SISO downlink LTE systems [1-3]. We conduct the system verification of the LTE downlink system on the WARP software defined radio platform [11].

First, we use the MATLAB/Simulink® to simulate the downlink LTE transceiver algorithms block-by-block in the accuracy of floating points. In so doing, the simulated results can be as hardware design references. Next, we employ System Generator® to implement the LTE downlink modules correspondingly. Finally, we use the Xilink ISE Design Suite to synthesize the bit stream file, and download the file on the WARP SDR platform. Simulated results show that the transmitted data can be recovered correctly. Besides, we also use the Chipscope to verify the correctness of the hardware implementation.

In this paper, we have implemented the packet control circuits, the CP module, symbol mapper/demapper circuits, the synchronization-signals module, QPSK modulator and demodulator, and OFDM modulator and demodulator. By using resource estimator, it shows that the designed system requires 16,527 slices, which can be implemented in the Virtex-4. As for future works, we will use multirate signal processing technique to improve the hardware efficiency. Besides, we will implement synchronization and channel estimator circuits for dealing with channel effects.

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