A Novel High Performance Nanoscaled Dopingless Lateral *PNP* Transistor on Silicon on Insulator

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***Abstract*— In this paper we propose a novel lateral *pnp* bipolar transistor on silicon on insulator. The novelty of the device is the realization of *p*-emitter, *n*-base and *p*-collector regions in an undoped silicon film by using the concept of charge plasma. The *n* and *p* regions in the proposed *pnp* transistor are not realized by the conventional diffusion or ion implantation techniques. However, *n* and *p* charge plasma is created by using of metals of different work functions to realize emitter, base and collector regions. The 2D simulation study has revealed that a very high current gain is achieved in the proposed device in comparison to conventional *pnp* transistor. Further, since the proposed device is not using the conventional ways of creating different doping regions, therefore, various doping related issues related to doping fluctuations, doping activations and the requirement of high temperature annealing are absent in the proposed device and is hence more robust and reliable.**

***Index Terms*— Charge plasma, SOI, lateral BJT, current gain.**

I. Introduction

The increasing demand of higher performance portable devices has provided enough motivation to device designers to go for the system on chips (SoC). In a SoC, the entire system, which may a multi signal and/or multi technology, is fabricated on a single substrate. Among many technologies which are being used to realize a SoC efficiently, the bipolar-CMOS technology (BiCMOS) is potentially favorable and strong. BiCMOS is the only technology providing bipolar and CMOS domains together. Bipolar technology is best suited for the realization of analog circuitry, as it provides large output resistance (desirable for many analog applications), high transconductance and high speed [1-2]. For designing high performance push-pull circuits and active resistors for analog applications, a high performance *pnp* BJT is highly desirable. The *pnp* bipolar transistors can act as efficient drivers in the output stages of analog devices, like operational amplifiers, by reducing the supply current [3-4]. Further, complementary bipolar technology using *npn* and *pnp* bipolar transistors have applications in amplifiers, feedback circuits, current mirrors and push pull circuits. The performance of BiCMOS can be significantly improved if it is realized on SOI substrates. The SOI-BICMOS possesses superior dc/ac isolation, reduces noise, higher speed, reduced cross talk etc. However, the technology is complex and costlier, as there are severe compatibility problems between vertical bipolar junction transistor (BJT) and CMOS devices. The problems of SOI-BiCMOS can be addressed by using lateral BJTs instead of vertical, as lateral BJT share fabrication scheme with CMOS and is more compatible with it. However, the lateral BJTs are inferior to vertical ones in terms of cutoff frequency (f_T) and current gain (β) due to large base resistance [5-10].

Keeping in mind the broad range of applications of *pnp* transistor, efforts have been made in this work to improve the performance of a lateral *pnp* transistor on SOI. The problem of poor current gain in a lateral *pnp* BJT has been addressed by proposing a new structure of lateral *pnp* transistor on SOI. The proposed device uses the concept of charge plasma [11-14] to realize emitter, base and collector regions and is being called as lateral *pnp* bipolar charge plasma transistor (BCPT). The p^+ emitter, *n* base and *p* collector regions have been creating not by using conventional ion implantation or diffusion techniques, however, by using metals of different work functions. These metals induce *p* and *n* type doping in a thin undoped silicon film. A significant improvement in current gain is achieved in the proposed device in comparison to the conventional *pnp* transistor. The 2D simulation study using Atlas device simulator [15] has shown a significant improvement in the current gain in comparison to the conventional *pnp* transistor. However, cutoff frequency is poor in the proposed device and need to be improved to use the device for high frequency applications. Further, the proposed device is robust and reliable as doping related issues like doping fluctuations, doping activations and the requirement of high temperature annealing are absent in the proposed device.

This paper is divided into five sections. Section II discusses the proposed and the conventional devices and their parameters. Section III discusses various simulation models used in the study. The results and discussion have been done in section IV. Section V concludes the paper.

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II. DEVICE SCHEMATICS AND SIMULATION PARAMETERS

The schematic diagrams of the proposed lateral *pnp* BCPT and the conventional lateral BJT are shown in Figure 1. The

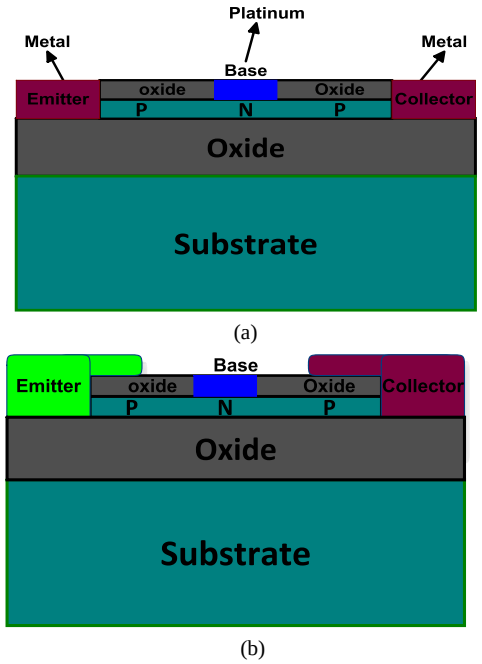


Figure 1: Schematic diagrams of (a) Conventional BJT and (b) Proposed *pnp* BCPT.

proposed and the conventional devices use the background *p* type doping of $N = 1 \times 10^{13}$ /cm^3, the buried-oxide layer thickness (t_{box}) of 375 nm, the gate-oxide thickness (t_{ox}) of 5 nm and the silicon film thickness (t_{Si}) of 15 nm. The electrode lengths of the emitter, base, and collector regions are chosen to be 0.2, 0.1, and 0.4 µm, respectively in the proposed device. For creating the emitter, by inducing holes in the undoped silicon body, platinum (work function Φ =5.65 eV) is employed as the emitter electrode metal. For inducing electrons to create the base region, hafnium (work function Φ = 3.90 eV) is used. As the collector of p-n-p transistor needs to have a lower carrier concentration than the base region, to induce holes to create the collector region, Au (work function Φ = 5.0 eV) is used. The separation between the electrodes (L_S) in the proposed device is taken as 100 nm. It is also important to choose an appropriate thickness for the silicon film to maintain uniform induced carrier distribution through-out the silicon thickness and it has to kept within the Debye length [11-14].

III. DEVICE SIMULATION MODELS

A two dimensional (2D) device simulator Atlas [15] has been used to simulate the devices. To accurately design and simulate the devices, various models have been used. The models include *fldmob*, *consrh*, *auger* and *BGN etc*. The recombination effects are taken into account by using Klassens's model [16-18] for concentration dependent lifetimes for Shockley-Read-Hall (SRH) recombination with intrinsic carrier life times $n_{ie} = n_{ih} = 0.2$µs. The other models used include Fermi-Dirac distribution, Philips unified mobility model, band gap narrowing (*BGN*) model [12-14] ,Selberherr impact ionization model (*selb*) [19] and Shirahata mobility model [20].

IV. SIMULATION RESULTS AND DISCUSSION

The important phenomenon in this work is the creation of charge plasma of different types (*n* and *p*) and different concentrations. This is being done by using metals of different work functions, as mentioned above. The induced charge plasma concentration in the emitter, base and collector regions, taken along a cross section at a distance of 2 nm, is shown in Figure 2. It shows the induced charge concentration for both equilibrium conditions (with V_{BE} = 0V and V_{CE} = 0V) and non-equilibrium conditions like forward active mode (with V_{BE} = 0.7V and V_{CE} = 1V). The induced concentrations in the emitter, base and collector regions are $p_E = 2 \times 10^{18}$ /cm3, $n_B = 1 \times 10^{20}$ /cm3 and $p_C = 2 \times 10^{17}$ /cm3 respectively.

Figure 3 shows the band diagrams of the proposed device under equilibrium and non equilibrium conditions. Figure 3(a) shows that the alignment of quasi Fermi levels under equilibrium conditions for both electrons and holes.

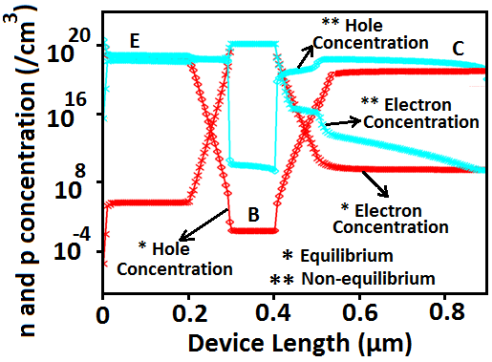
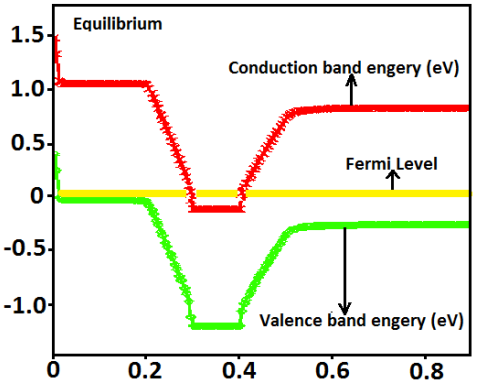


Figure 2: Total carrier concentration in the proposed pnp BCPT structure for different bias conditions (under thermal equilibrium and under non-equilibrium conditions).

As expected, the quasi Fermi levels for electrons and holes under equilibrium conditions are aligned, as shown in Figure 3 (a). Figure 3(b) shows the band diagram for the proposed device under forward active mode. Under non-equilibrium conditions, the alignment breaks, there are different quasi Fermi levels for electrons and holes. This can be attributed to high plasma concentration on either side of the forward biased base-emitter junction.



(a)

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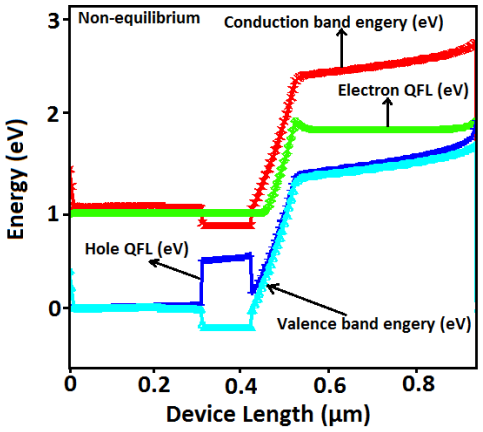

(b)

Figure 3: Energy band diagrams of the *pnp* BCPT structure for different bias conditions (a) under thermal equilibrium (b) under non-equilibrium conditions.

The important characteristics of Gummel plots of the proposed and the conventional devices are shown in Figure 4. It is clear that the base current of the proposed *pnp* BCPT device is significantly lower than the conventional BJT. This can be attributed to the presence of Surface Accumulation Layer Transistor (SALTran) effect [21-22]. Figure 5 shows the comparison of the current gains of the proposed and the conventional devices. It is clear that the current gain is significantly higher in the proposed *pnp*-BCPT device. The higher current gain can be due to accumulation of holes at the surface. The accumulation of holes results in an electric field due to the concentration gradient from the metal–semiconductor interface toward the emitter–base junction. This electric field repels the minority carrier electrons injected from the base into emitter and subsequently reduces the base current. Hence a large current gain is achieved in the proposed device in comparison to the conventional *pnp* transistor. Further it is observed that the peak current gain of proposed *pnp* BCPT is 1450 and that of conventional *pnp* BJT is around 10. One of the biggest problem with the proposed device is its poor cutoff frequency in comparison to the conventional device. Figure 6 shows that the cutoff frequency is lower in the proposed device in comparison to the conventional device. Therefore, it cannot used efficiently for high frequency applications. Hence it is mandatory to address the f_T problem of the proposed device to increase its application domain.

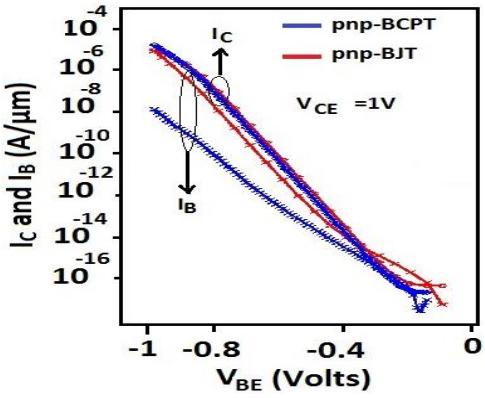

Figure 4: Gummel plots for the conventional pnp BJT and the proposed pnp BCPT structures.

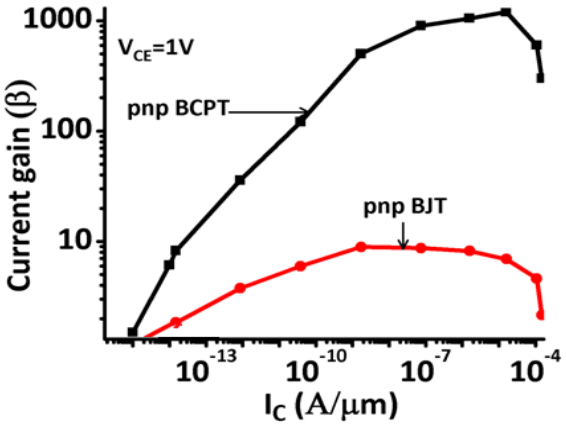

Figure 5: Current gain comparison of the conventional *pnp* BJT, *pnp* BCPT structures.

Figure 6 shows that the cutoff frequency of *pnp* conventional BJT is 1.15 GHz and that of the proposed *pnp* is 0.92 GHz. The lower cutoff frequency in the proposed device can be attributed to higher parasitic capacitance and the presence of gaps in the proposed device. The output characteristics of the proposed device are shown in Figure 7. It is clear that the proposed device has reasonably good breakdown strength.

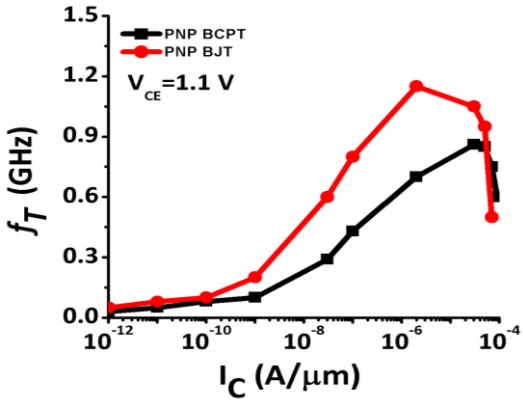

Figure 6.Cutoff frequency (f_T) comparison of the conventional *pnp* BJT, *pnp* BCPT structures.

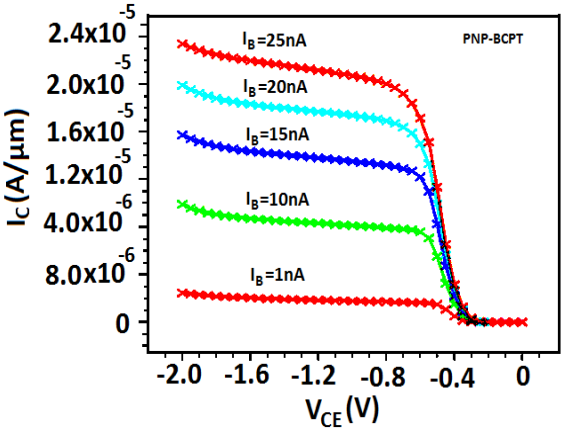

Figure 7: Output Characteristics of proposed *pnp* BCPT

Figure 8 and Figure 9 show the effect of emitter electrode work function variations on the current gain and the cutoff frequency of the proposed device. It is observed that work function variation significantly changes the current gain and

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the cutoff frequency of the proposed device. This can be attributed to the fact that the change in work function of emitter electrode changes the charge plasma concentration in the emitter, which changes emitter efficiency and in turn changes current gain and cutoff frequency. It is seen from Figures (8 and 9) that the cutoff frequency and the current gain increase with the increase in emitter work function. However, increase cannot be linear and can saturate after some threshold emitter work function.

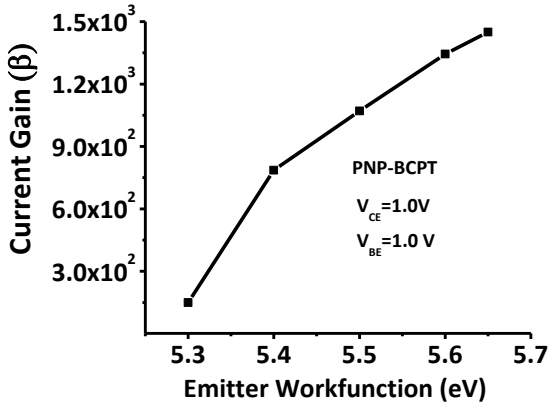

Figure 8: Variation of current gain with Emitter work-function

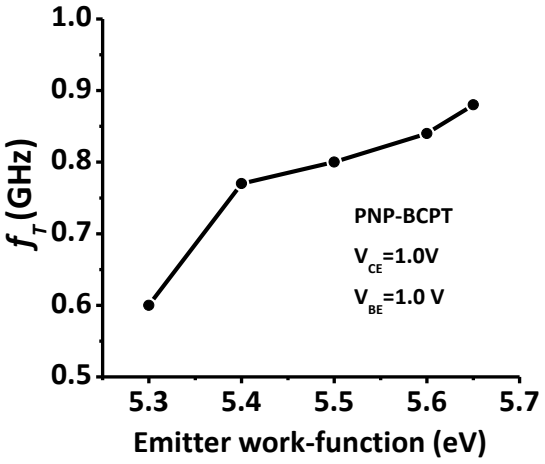

Figure 9: Variation of cutoff frequency (f_T) with Emitter work-function

V. CONCLUSIONS:

In this paper, the charge plasma concept has been used to improve the performance of a lateral *pnp* transistor. Metals of different work functions has been used to induce *p* type and *n* type doping concentration in a thin silicon film of around 15 nm to realize emitter, base and collector regions. The simulation study has shown that a large current gain is achieved in the proposed device in comparison to the conventional device. Further, the proposed device is highly reliable as there are no doping related issues like doping fluctuations, doping activations and the requirement of high temperature. The major problem in the proposed device is the poor cutoff frequency, which need to be improved on priority.

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