PVT Insensitive Reference Current Generation

Suhas Vishwasrao Shinde

***Abstract*— In this paper, supply, process & temperature compensated, low voltage current reference for CMOS integrated circuits is presented. To minimize production cost, it uses no BJTs, external components or trimming procedures. This circuit is designed in Intel-22nm process and evaluated by computer simulations. The circuit behaviour is supported by theoretical expressions and is in agreement with simulation results. A comparison with most current references in the literature shows considerable tolerance improvement. Simulation results show PVT tolerance of +/-10% and 1σ standard deviation of 5uA at mean of 82uA. An autonomous, all MOS, low voltage & process technology independent features make it suitable for advanced sub micron processes like 14nm, 10nm & beyond.**

***Keywords*— CMOS integrated circuits, current reference, bandgap reference, process and temperature compensation, sub threshold, weak inversion, strong inversion, PTAT, CTAT, BGR.**

I. Introduction

An ideal current reference circuit should be autonomous and should be used locally per analog block from modularity point of view. This avoids long reference current distribution network and associated issues of IR drop, noise coupling and current mirroring mismatch. A classical way of current reference generation is by a resistor as current defining element [16]. This requires precise bandgap reference voltage and off-chip precision resistor which consumes I/O pin. It also involves a feedback loop hence may break in to oscillations if not meeting sufficient phase margin criteria. Although this current reference is very accurate it increases the system cost. Several integrated current reference circuits have been reported in the past which avoids explicit voltage reference and external components. However these current references either compensate for temperature or for process and not for both. In this paper, MOS reference current circuit has proposed which has very low sensitivity for supply, process and temperature variations. Further it enables modular design approach for large systems because it does not require bandgap reference (BGR) circuit, regulator or external components. This architecture exploits the sub threshold region properties of MOSFET to generate reference current. This sub threshold region operation allows use of low supply voltage (~1V).

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Low voltage operation is gaining importance for advanced sub micron processes due to devices shrinking down and becoming more fragile with reduced electrical stress limit.

The proposed scheme of reference current generation is realized by summation of process & supply compensated proportional to absolute temperature (PTAT) & complementary to absolute temperature (CTAT) currents. Precise reference current is generated by adjusting negative temperature coefficient of CTAT current such that it ideally cancels positive temperature coefficient of PTAT current. This architecture is feed forward system and hence no stability issue arises. All MOS implementation, low voltage operation and process technology independent operation makes it suitable for advanced sub micron processes like 14nm, 10nm and onwards.

This paper is organised in to 6 sections. Section II describes theory and circuit of supply and process immune PTAT current generation. Section III explains theory and circuit of supply and process immune CTAT current generation. Section IV develops new reference current generation circuit and section V reports simulation results from Intel-22nm process, testing theory and validating proposed reference current circuit. Finally section VI gives concluding remark.

II. PTAT Current Generation

In this section, a standard voltage reference circuit [9] is described as supply & process insensitive PTAT current generating circuit. A PTAT current circuit is as shown in fig. 1a). Here devices MP9 and MP10 are operated in strong inversion whereas MN7 and MN8 are operated in weak inversion.

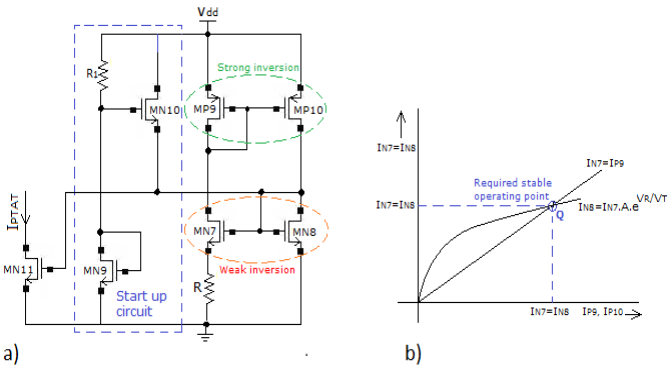

Fig. 1 a) PTAT circuit and [9] b) start-up operating points.

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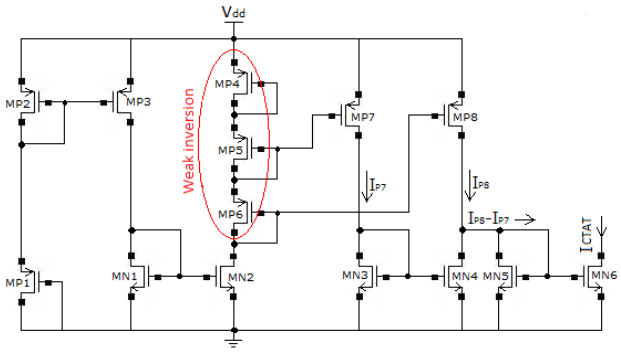

Fig. 2. CTAT current circuit [8].

Hence,

$$I_{P9}=\frac{\beta_{p9}}{2}(V_{GS9}-V_{TP})^2$$

$$I_{P10}=\frac{\beta_{p10}}{2}(V_{GS10}-V_{TP})^2 \quad \text{and}$$

$$I_{N7}=I_0\frac{W_{N7}}{L_{N7}}e^{(V_{GS7}-V_{TN})/\eta V_T}$$

$$I_{N8}=I_0\frac{W_{N8}}{L_{N8}}e^{(V_{GS8}-V_{TN})/\eta V_T}$$

Designing, $\beta_{N8}=A\,\beta_{N7}$ =>

$$\frac{W_{N8}}{L_{N8}}=A\frac{W_{N7}}{L_{N7}}$$

Therefore,

$$I_{N8}=I_0\,A\frac{W_{N7}}{L_{N7}}e^{(V_{GS8}-V_{TN})/\eta V_T}$$

$$I_{N8}=I_0\,A\frac{W_{N7}}{L_{N7}}e^{(V_{GS7}+V_R-V_{TN})/\eta V_T}$$

since $V_{GS8}=V_{GS7}+V_R$

Therefore,

$$I_{N8}=I_0\,A\frac{W_{N7}}{L_{N7}}e^{V_R/\eta V_T}\cdot e^{(V_{GS7}-V_{TN})/\eta V_T}$$

$$I_{N8}=\underbrace{I_0\frac{W_{N7}}{L_{N7}}e^{(V_{GS7}-V_{TN})/\eta V_T}}_{I_{N7}}.Ae^{V_R/\eta V_T}$$

$$\therefore\quad I_{N8}=I_{N7}\,Ae^{V_R/\eta V_T}$$

Designing for $I_{P10}=B\,I_{P9}$ =>

$$I_{N8}=B\,I_{N7}$$

Therefore,

$$V_{REF}=\eta V_T\ln\left(\frac{S_{N7}}{S_{N8}}.\frac{S_{P10}}{S_{P9}}\right)$$

Where A=SN8/SN7, B=SP10/SP9

and

$$I_{PTAT}=V_{REF}/R$$

Therefore

$$I_{PTAT}=\frac{\eta V_T}{R}\ln\left(\frac{S_{N7}}{S_{N8}}.\frac{S_{P10}}{S_{P9}}\right)$$

$$I_{PTAT}=\frac{\eta}{R}\frac{KT}{q}\ln\left(\frac{S_{N7}}{S_{N8}}.\frac{S_{P10}}{S_{P9}}\right)$$

(1)

Since $V_T = KT/q$

Where the slope,

$$m=\frac{\eta}{R}\frac{K}{q}\ln\left(\frac{S_{N7}}{S_{N8}}.\frac{S_{P10}}{S_{P9}}\right)$$

(2)

Where K= Boltzmann constant

q = Electronic charge

$\eta \sim 1$

The slope or temperature coefficient of CTAT current can be adjusted through design parameter SN7, SN8, SP10, SP9 and resistor R.

The circuit in fig. 1 a) has two stable operating points; First, where no current flows in any branch of circuit and PTAT voltage is zero & second, where IN7 is equal to IN8. The circuit is brought up to this 2nd stable operating point by start up circuit comprised of MN9, MN10 & resistor R1.

III. CTAT Current Generation

This section presents supply and process insensitive CTAT current generation based on subtraction of two currents [8]. It uses natural variation of two currents to cancel out variation in the difference current. The current subtraction is such that their difference is non-zero but their process coefficient is the same. Hence their variation across process gets cancelled. Although process coefficient is made zero (theoretically!), variation with respect to another independent variable temperature exist. The observed temperature coefficient of current is negative giving rise to CTAT current. The underlying theory and model of process compensation of current for circuit in fig. 2 is as follows.

$$I_{P8}\approx\beta z_8(V_{GS8}-V_{TP})^2 \quad \text{and}$$

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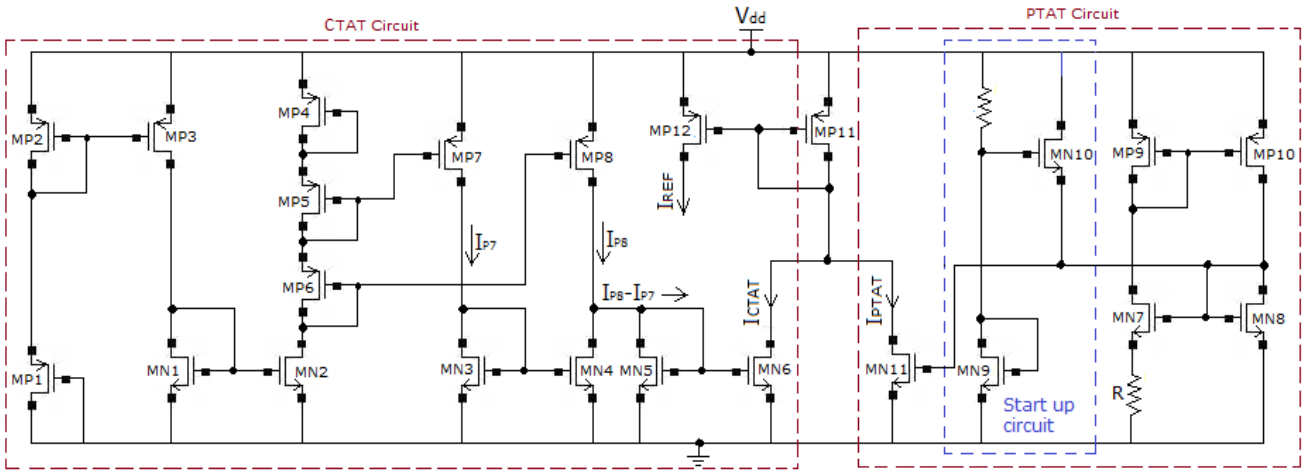

Fig. 3. Proposed reference current generation circuit.

$$I_{P7} \approx \beta z_7 (V_{GS7}-V_{TP})^2$$

Where reference current,

$$I_{REF} = I_{P8} - I_{P7} \quad (I_{P8} \neq I_{P7})$$

For reference current variation with respect to process to be zero,

$$\frac{\partial I_{REF}}{\partial P} = 0 \Rightarrow \frac{\partial I_{P8}}{\partial P} = \frac{\partial I_{P7}}{\partial P}$$

Where

$$\frac{\partial I_{P8}}{\partial P} = z_8 (V_{GS8}-V_{TP})^2 \frac{\partial \beta}{\partial P} - 2\beta z_8 (V_{GS8}-V_{TP}) \frac{\partial V_{TP}}{\partial P} \quad \text{and}$$

$$\frac{\partial I_{P7}}{\partial P} = z_7 (V_{GS7}-V_{TP})^2 \frac{\partial \beta}{\partial P} - 2\beta z_7 (V_{GS7}-V_{TP}) \frac{\partial V_{TP}}{\partial P}$$

Therefore

$$z_8 (V_{GS8}-V_{TP})^2 \frac{\partial \beta}{\partial P} = -2\beta z_7 (V_{GS7}-V_{TP}) \frac{\partial V_{TP}}{\partial P} \quad \text{and}$$

$$z_7 (V_{GS7}-V_{TP})^2 \frac{\partial \beta}{\partial P} = -2\beta z_8 (V_{GS8}-V_{TP}) \frac{\partial V_{TP}}{\partial P}$$

Therefore

$$\frac{z_8 (V_{GS8}-V_{TP})^2}{z_7 (V_{GS7}-V_{TP})^2} = \frac{z_7 (V_{GS7}-V_{TP})}{z_8 (V_{GS8}-V_{TP})}$$

$$\Rightarrow$$

$$\left(\frac{z_8}{z_7}\right)^2 = \frac{(V_{GS7}-V_{TP})^3}{(V_{GS8}-V_{TP})^3}$$

$$\Rightarrow$$

$$\frac{z_8}{z_7} = \left(\frac{V_{GS7}-V_{TP}}{V_{GS8}-V_{TP}}\right)^{3/2}$$

$$\Rightarrow$$

$$\frac{z_8}{z_7} = \left(\frac{aV_{TP}-V_{TP}}{bV_{TP}-V_{TP}}\right)^{3/2}$$

Where $V_{GS7} = aV_{TP}$ and $V_{GS8} = bV_{TP}$

$$\Rightarrow$$

$$\frac{z_8}{z_7} = \left(\frac{a-1}{b-1}\right)^{3/2} \quad (3)$$

For b=3 and a=2, $z_8/z_7 = 0.3535 \Rightarrow z_7 = (2.84)z_8$

Thus choosing MP7 size 2.84 times MP8 creates zero process coefficient (ZPC). The process insensitive difference current is immune against supply variation as well because subtraction operation of I_{P7} and I_{P8} cancels out their variation partially. Although process and supply variation is cancelled the variation due to other independent variable called temperature still exist which exhibits CTAT behaviour.

IV. IREF CURRENT GENERATION

The basic principle of the reference current generation is illustrated in fig. 4 where supply & process insensitive PTAT & CTAT currents are added. Fig. 3 shows complete circuit schematic of current reference, developed by combining PTAT & CTAT circuits from sections II & III respectively. It's all MOSFET integrated circuit design with 1V supply. The negative temperature coefficient of CTAT current can be adjusted to match the positive temperature coefficient of PTAT current to nil temperature variation. From equation (2) design parameters SN7, SN8, SP10, SP9 and R can be tuned to adjust negative temperature coefficient of CTAT current. The design equations are solved and circuit is optimized considering extremes of supply, process and temperature corners for minimum reference current variation.

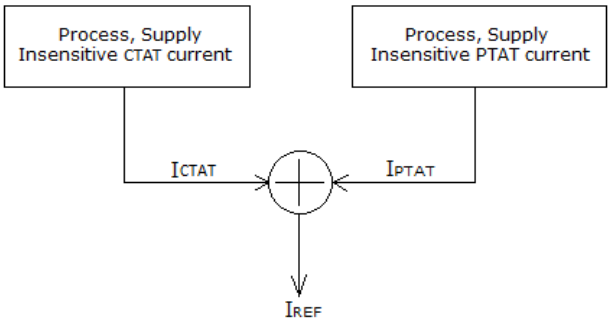

Fig. 4. Basic principle of reference current generation.

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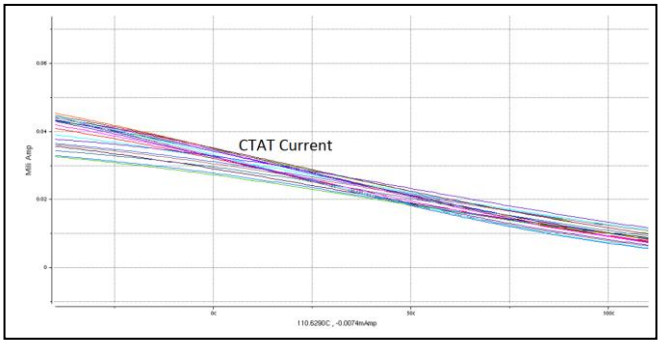
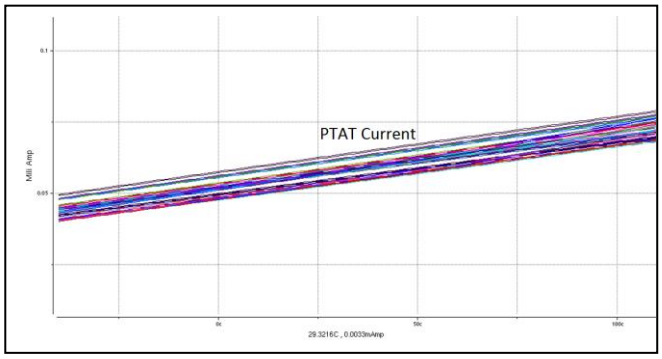
The low voltage operation of this circuit is an advantage over prior art architectures which require 2.5V [7] and 3.5V [2] supply voltages. Some reported current reference circuits [6] involve feedback loops hence critical from stability point of view. This circuit has no stability issues being feed-forward system.

V. Simulation Results

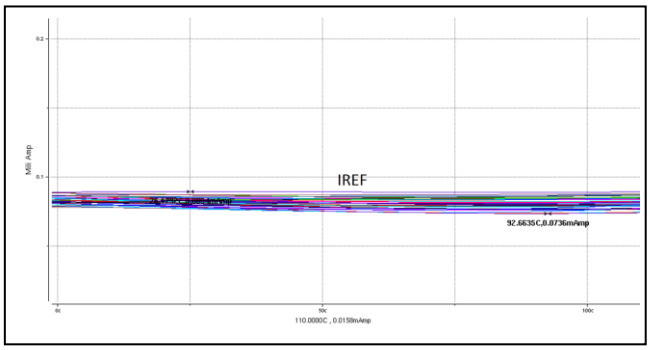
This current reference is designed in Intel-22nm process and simulation results are reported to test mathematical model and validate the design. Fig. 5 a) shows I-T characteristic curve of PTAT current generated by voltage reference circuit depicted in fig. 1 a). Fig. 5b) shows I-T characteristic curve of CTAT current generated by circuit architecture in fig. 2. The addition of these two currents results in to reference current characteristics as plotted in fig. 5c). The extreme PVT variation observed is +/- 10%. This tolerance is over temperature range of 0^0C to 110^0C, supply variation +/-5% and on-die calibrated resistor variation of +/- 5%. The PVT performance comparison of this current reference with prior published work in [4], [6] & [7] shows better results due to the fact that they do not address all variations together. The +/-10% tolerance is mainly attributed to non linearity of PTAT & CTAT currents with respect to temperature, partial compensation of CTAT current with respect to supply variation and small but finite variation of calibrated resistor. A word of caution to designers about SPICE simulations! Precaution has to be taken with respect to SPICE simulations since sub threshold region models may not be accurate for their process.



a)



b)



c)

Fig. 5 a) PTAT current b) CTAT current and c) IREF current.

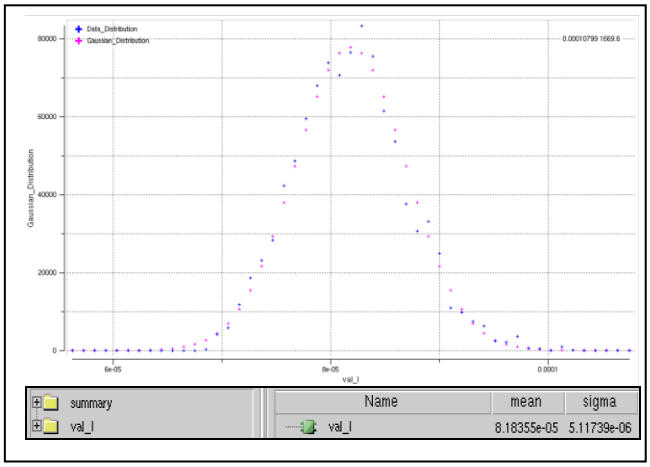


Fig. 6. Monte Carlo results showing normal Pdf with μ=82uA and 1σ SD = 5uA.

The incorrect modelling of weak inversion region tends to predict good results and hence silicon correlation becomes necessary. Finally Fig. 6 shows statistical simulation results for reference current under typical conditions, supply=1V, process = typical, and temperature = 50^0C. Observed 1σ standard deviation for 1000 runs is 5uA at mean value of 82uA. This statistical spread, σ/μ =0.06 is significantly lesser than reported results in [2].

VI. Conclusion

This paper demonstrates an alternative approach of reference current generation with necessary mathematical expressions. It verifies approach through circuit simulations of current reference designed in Intel 22nm process. The proposed architecture provides immunity against supply, process and temperature variations. An autonomous nature makes it suitable for modular design style of large systems. This circuit is easy to use for biasing applications in analog circuits. An autonomous, low voltage, CMOS compatibility and process insensitive features make it suitable for advanced sub micron processes.

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