Closed-Loop Adaptive Switched-Capacitor Step-Down DC-DC Converter for Piezoelectric Energy Harvesting

Yuen-Haw Chang and Chun-Hung Wang

Abstract—A closed-loop scheme of adaptive switched-capacitor converter (ASCC) is presented by combining a phase generator and non-overlapping circuit to realize the switched-capacitor-based (SC) step-down conversion for piezoelectric energy harvesting. In the power part of ASCC, there are two cascaded sub-circuits: (i) Front: the bridge rectifier and a filter capacitor (C1), and (ii) Core: 5-stage serial-parallel SC step-down converter and an output capacitor (C2). By using the front bridge rectifier, it converts the AC source of piezoelectric device into the DC source, and then harvests the energy to store in the filter capacitor (C1) for building the DC supply Vdc. The core 5-stage serial-parallel SC converter can provide 5 different step-down voltages (V1, V2, V3, V4, V5), and with the help of the phase generator, perform an adaptive charging operation stage by stage (from the lower voltage to the higher one) for the protection of the battery load. Finally, the closed-loop ASCC is designed by OrCAD Pspice, and simulated for some cases: steady-state and dynamic responses (source/loading variation). All results are illustrated to show the efficacy of the proposed scheme.

Index Terms—adaptive, piezoelectric, harvesting, switched-capacitor, step-down converter, serial-parallel.

I. INTRODUCTION

Recently, with the rapid development of power electronics technology, the demand on voltage supply increases more and more. The step-up/down DC-DC converters are employed more widely for the electricity-supply applications, such as photovoltaic system (PV), fuel cell, X-ray systems, and are asked for some characteristics of light weight, small volume, high efficiency and better regulation capability.

The SC power converter based on structure of charge pump is one of the good solutions to low power and high gain DC-DC conversion, because it has only semiconductor switches and capacitors. Unlike traditional converters, SC converter needs no magnetic element, so it has light weight and small volume and low EMI. However, most SC circuits have voltage gain proportional to the number of pumping capacitors. Now, various SC types have been suggested and the well-known topologies are described as follow. In 1976, Dickson charge pumping was proposed based on a diode-chain structure via pumping capacitors [1]. It provides voltage gain proportional to the stage number of pumping capacitor, and the detailed dynamic model and efficiency analysis were discussed [2]. But, its drawbacks include the fixed voltage gain and the larger device area. In 1993, Ioinovici et al. suggested a voltage-mode SC with two symmetrical capacitor cells working complementarily [3]. In 1997, Zhu and Ioinovici performed a comprehensive steady-state analysis of SC [4]. In 2009, Tan et al. proposed a low-EMI SC by interleaving control [5]. In 2011, Chang proposed an integrated SC step-up/down DC-DC/DC-AC converter/inverter [6]-[8]. In 2002, Ottman et al. proposed the prototype of piezoelectric energy harvesting circuit based on the LC resonant booster for wireless remote power supply [9]. In this paper, with on magnetic elements, the closed-loop adaptive SC-based piezoelectric energy harvesting circuit is presented to achieve the multistage charging operation of battery.

II. CONFIGURATION OF ASCC

Fig. 1 shows the overall circuit configuration of closed-loop ASCC, and it contains two major parts: power part and control part for an adaptive multi-stage charging operation of battery. Fig. 2 shows the detailed logic circuit of the control part.

A. Power part

The power part of ASCC is shown in the upper half of Fig. 1, and it consists of a bridge rectifier and SC step-down DC-DC converter connected in series between the piezoelectric device and the battery load. The bridge rectifier contains 4 diodes (D1-D4) and one input filter capacitor C1 to obtain a rectified, filtered, and stable supply voltage Vdc. The SC step-down converter is composed of 5 pumping capacitors (C1-C5), 7 power switches (S1-S7, S8, S9), one output filter capacitor Cm, and 8 diodes (D12-D20), where each capacitor has the capacitance C (C1=C2=C3=C4=C5). Fig. 3 shows the theoretical waveforms of ASCC. Here, the whole charging operation is scheduled and divided into 5 stages (Stage I, II, III, IV, and V) for the protection of the battery load, especially for the lower battery voltage. In each stage, there are two interleave operations: charging capacitors in series (as 𝜙1=1) and discharging capacitors in parallel (as 𝜙2=1), where 𝜙1 and 𝜙2 are a set of non-overlapping anti-phase signals, so as to realize the SC step-down conversion. The operations of these 5 stages are described as follows.

(i) Stage I : between 0 and \( \phi = \frac{7}{8} \)

At the charging cycle ( 𝜙1=1 ), turn on \( S_1, S_2, \) and...
turn off $S_o$, $S_1$-$S_5$. Then, the diodes $D_5$-$D_8$ are on, and $D_9$-$D_{12}$ are off. The current-flow path is shown as """" in Fig. 4(a). The capacitors $C_1$-$C_5$ are charged in series by source $V_s$. At the discharging cycle ($\phi_2 = 1$), $C_1$-$C_5$ are discharged in parallel to supply the energy to output filter capacitor $C_o$ and battery load $C_{Bat}$. The current-flow path is shown as """" in Fig. 4(a).

(ii) Stage II : between $\bigtriangleup$ and $\bigtriangleup$

At the charging cycle ($\phi_1 = 1$), turn on $S_o$, $S_1$, and turn off $S_o$, $S_1$-$S_5$. Then, the diodes $D_1$-$D_4$ are on, and $D_5$-$D_{12}$ are off. The current-flow path is shown as """" in Fig. 4(b). The capacitors $C_1$-$C_4$ are charged in series by source $V_c$. At the discharging cycle ($\phi_2 = 1$), $C_1$-$C_4$ are discharged in parallel to supply the energy to output filter capacitor $C_o$ and battery load $C_{Bat}$. The current-flow path is shown as """" in Fig. 4(b).

(iii) Stage III : between $\bigtriangleup$ and $\bigtriangleup$

At the charging cycle ($\phi_1 = 1$), turn on $S_o$, $S_1$, and turn off $S_o$, $S_1$, $S_2$, $S_3$. Then, the diodes $D_5$, $D_6$ are on, and $D_7$-$D_{12}$ are off. The current-flow path is shown as """" in Fig. 4(c). The capacitors $C_1$-$C_3$ are charged in series by source $V_o$. At the discharging cycle ($\phi_2 = 1$), $C_1$-$C_3$ are discharged in parallel to supply the energy to output filter capacitor $C_o$ and battery load $C_{Bat}$. The current-flow path is shown as """" in Fig. 4(c).

(iv) Stage IV : between $\bigtriangleup$ and $\bigtriangleup$

At the charging cycle ($\phi_1 = 1$), turn on $S_o$, $S_2$, and turn off $S_o$, $S_1$, $S_2$, $S_5$. Then, the diodes $D_4$ are on, and $D_5$-$D_{12}$ are off. The current-flow path is shown as """" in Fig. 4(d). The capacitors $C_1$, $C_2$ are charged in series by source $V_c$. At the discharging cycle ($\phi_2 = 1$), $C_1$-$C_2$ are discharged in parallel to supply the energy to output filter capacitor $C_o$ and battery load $C_{Bat}$. The current-flow path is shown as """" in Fig. 4(d).

(v) Stage V : between $\bigtriangleup$ and $\bigtriangleup$

At the charging cycle ($\phi_1 = 1$), turn on $S_o$, $S_1$, and
turn off $S_6$, $S_2$-$S_5$. Then, the diodes $D_5$-$D_{12}$ are off. The current-flow path is shown as "---" in Fig. 4(e). The capacitors $C_1$ are charged in series by source $V_s$. At the discharging cycle ($\phi_2=1$), $C_1$ are discharged in parallel to supply the energy to output filter capacitor $C_o$ and battery load $C_{Bat}$. The current-flow path is shown as "- - -" in Fig. 4(e).

Based on the operations as above, the battery voltage $V_{Bat}$ can be raising up to the supply voltage $V_s$ stage by stage. This way can avoid large peak current on the battery to extend the usage lifetime of battery.

**B. Control part**

The control part of ASCC is shown in the lower half of Fig. 1, and its detailed logic circuit is as in Fig. 2. It is
composed of non-overlapping circuit and phase generator. From the controller signal flow, the feedback signals $V_o$ and $V_s$ are sent into the phase generator for making the switch signals $S_1$-$S_5$. In the phase generator, it includes the NMOS-based voltage divider, voltage comparator, and some AND logic gates. This voltage divider has a NMOS-cascaded structure to produce a various division of supply voltage $V_s$ as:

$$\frac{V_s}{2}, \frac{V_s}{3}, \frac{V_s}{4}, \frac{V_s}{5}, \text{and} \frac{V_s}{6}.$$  

In the voltage comparator, the output voltage $V_o$ is compared with these divisions of $V_s$ in order to produce the basic control signals $S_1$-$S_5$ for the multi-stage operation. Finally, the practical switch signals $S_1$-$S_5$ can be obtained with the help of the synchronous operation of $S_i$ via some AND logic gates. Here, $S_i$ is the switch signal generated by $\phi_i$ and $S_{OFF}$ to control the energy transferring from the piezoelectric device to the SC bank, and $S_o$ is generated by $\phi_2$ and $S_{OFF}$ to control the energy transferring from the SC bank to the battery load, where $\phi_1$ and $\phi_2$ are a set of non-overlapping clocks produced by the non-overlapping circuit. Based on these designs, the control part can generate these switch signals exactly like the waveforms in Fig. 3 for achieving the charging operation of battery stage by stage.

![Fig. 5. Steady-state response of ASCC for Case I](image)

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**III. EXAMPLES OF ASCC**

In this section, based on Fig. 1, the ASCC is designed and simulated by OrCAD Pspice tool. The results are illustrated to verify the efficacy of the proposed converter. The relevant component parameters are listed in Table I. For checking closed-loop performances, some topics will be discussed as including: (i) Steady-state response (ii) Dynamic response (source/loading variation).

(i) **Steady-state response:**

Case I:

Assume the supply voltage $V_s$ is 18V, and then the steady-state result of output voltage $V_o$ within 6.5 sec is obtained as in Fig. 5(a). Obviously, $V_o$ is raising to get close to $V_s = 18V$ stage by stage. After 5.88 sec, the

<table>
<thead>
<tr>
<th>TABLE I Components of ASCC</th>
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<tr>
<td>Rectified supply source ($V_s$)</td>
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<tr>
<td>Pumping capacitor ($C_1$-$C_5$)</td>
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<tr>
<td>Filter capacitor ($C_{i, o}$)</td>
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<tr>
<td>Battery Capacitor ($C_{Bat}$)</td>
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<tr>
<td>Power MOSFETs ($S_i, S_o, S_1$-$S_5$)</td>
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<tr>
<td>Switching frequency ($f_s$)</td>
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<td>Diodes ($D_1$-$D_{12}$)</td>
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operation starts entering the Stage OFF as shown in Fig. 5(b). Now, the charged battery keeps its voltage at about 17.28V.

Case II:
Assume the supply voltage $V_s$ is 12V, and then the steady-state result of output voltage $V_o$ (within 10 sec) is obtained as in Fig. 5(c). Obviously, $V_o$ is raising to get close to $V_s = 12V$ stage by stage. After 8.73 sec, the operation starts entering the Stage OFF as shown in Fig. 5(d). Now, the charged battery keeps its voltage at about 11.75V.

Case III:
Assume the supply voltage $V_s$ is 9V, and then the steady-state result of output voltage $V_o$ (within 11 sec) is obtained as in Fig. 5(e). Obviously, $V_o$ is raising to get close to $V_s = 9V$ stage by stage. After 10.32 sec, the operation starts entering the Stage OFF as shown in Fig. 5(f). Now, the charged battery keeps its voltage at about 7.87V.

Fig. 6. Dynamic response of ASCC for source variation.
Case I: (a)(b) $V_s = 18V \rightarrow 0V$ at 0.5sec, $0V \rightarrow 18V$ at 2.0sec. Case II: (c)(d) $V_s = 18V \rightarrow 0V$ at 2.0sec, $0V \rightarrow 18V$ at 3.0sec

Fig. 7. Dynamic response of ASCC for loading variation.
Case III: (a)(b) $C_{Bat} = 1mF \rightarrow 2mF$ at 1.5sec. Case IV: (c)(d) $C_{Bat} = 1mF \rightarrow 2mF$ at 7.0sec
start entering the Stage OFF as shown in Fig. 5(f). Now, the charged battery keeps its voltage at about 8.78V.

(ii) Dynamic response:
Since the piezoelectric device always generates the kind of pulsing source voltage, it is not easy to provide a pure and constant supply. Also, the number/capacitance of battery could be changed. Thus, these two situations (source variation/loading variation) should be considered here.

Case I:
Assume that supply voltage $V_s$ is 18V, and it has a voltage drop down to 0V from 0.5 sec to 2 sec as in Fig. 6(a). Fig. 6(b) shows the whole waveform of $V_o$. Obviously, the voltage level of $V_o$ stops raising to hold at 3.4V during the interval of $V_s = 0$V. When $V_s$ recovers back to 18V, $V_o$ keeps going back to the charging operation.

Case II:
Assume that supply voltage $V_s$ is 18V, and it has a voltage drop down to 0V from 2 sec to 3 sec as in Fig. 6(c). Fig. 6(d) shows the whole waveform of $V_o$. Obviously, the voltage level of $V_o$ stops raising to hold at 4.6V during the interval of $V_s = 0$V. When $V_s$ recovers back to 18V, $V_o$ keeps going back to the charging operation.

Case III:
Assume that $C_{Bat}$ is 1mF normally, and it changes from 1mF to 2mF at 1.5 sec as in Fig 7(a). Fig 7(b) shows the result of $V_o$. Clearly, it is found that $V_o$ has a sudden voltage drop while $C_{Bat}$: 1mF$\rightarrow$2mF. At the same time, the charging operation is going from Stage II back to Stage I for adapting the loading variation.

Case IV:
Assume that $C_{Bat}$ is 1mF normally, and it changes from 1mF to 2mF at 7 sec as in Fig 7(c). Fig 7(d) shows the result of $V_o$. Clearly, it is found that $V_o$ has a sudden voltage drop while $C_{Bat}$: 1mF$\rightarrow$2mF. At the same time, the charging operation is going from Stage OFF back to Stage V for adapting the loading variation.

The above results show that the closed-loop ASCC has a good output regulation capability to source/loading variations.

IV. CONCLUSIONS
A closed-loop scheme of ASCC is presented by combining a phase generator and non-overlapping circuit to realize step-down conversion and regulation for piezoelectric energy harvesting. The advantages of the proposed scheme are listed as follows. (i) In the ASCC, there are totally 5 stages scheduled for running the charging operation in order to protect the battery load. (ii) The ASCC belongs to the kind of SC circuit, so it needs no magnetic element (like inductor or transformer). Thus, the fabrication of ASCC is promising in the future. (iii) In the control part, the adaptive phase generator with changing the stage number is designed for being able to adapt the source/loading variations. At present, the prototype circuit of the proposed converter is implemented in the laboratory as shown the photo in Fig 8. Some experimental results will be obtained and measured for the verification of the proposed converter.

REFERENCES