EOS Protection Circuit for USB2 Transceiver

Suhas Vishwasrao Shinde

Abstract—**This paper presents CMOS integrated electrical over stress (EOS) protection circuit for USB2 transceiver. A unique full speed SE0 state in USB2 standard protocol produces overshoot and undershoots in presence of on board choke. The purpose of choke is to minimize EMI for USB2 differential signalling. This works fine as long as data signalling is differential. In the presence of SE0 state, single transition occurs on either Dp or Dn pad causing high inductive kick back from choke resulting in to excessive overshoot and undershoots. The electrical over stress on cascode devices leads to device degradation resulting in to violation of USB2 output driver impedance spec of 45 Ω +/-5%. This in turn increases defects per million count over time. To mitigate this reliability issue EOS protection circuit is proposed. This circuit is designed in Intel-22nm process and evaluated by computer simulations across all PVT conditions. Proposed EOS protection circuit reduces respective overshoot and undershoot of 4.2V and -0.6V to 3.7V and -0.34V. For the growing EOS concern of deep submicron devices in 14nm, 10nm and onward technologies, this invention becomes an ideal choice.**

Keywords— **CMOS integrated circuits, EOS protection, SE0 state, EOP, USB2 standard, Overshoot, Undershoot.**

I. INTRODUCTION

An USB2 standard was developed ~20 years back without much consideration about future manufacturing processes. The USB2 low/full speed signalling is 3.3V hence 3.3V supply is commonly used for transceiver circuits implementing low/full speed as well as high speed signalling modes. The advanced manufacturing processes like 22nm, 14nm and 10nm uses devices with reduced threshold voltages and electrical stress limits. Circuit implementation in these technologies with 3.3V supply is almost impossible unless process offers a flavour of high voltage devices like 1.8V with higher electrical stress limit. However this is against the trend of advanced process technology where devices are shrinking down. Their threshold voltages and stress limits are reducing. This necessitates some innovations in process as well as in design to mitigate EOS issue. Intel 22nm process does not support 3.3V devices so output driver is always designed with stacked 1.8V devices to minimize electrical over stress. However large overshoot/undershoot may violate stress limits of these devices hence alternative approach in circuit design was an urgency to deal with this EOS issue. This motivates this work on developing novel EOS protection circuit for USB2 transceiver in Intel 22nm process [1].

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This is based on charge injection and drain from pad subjected to undershoot and overshoot respectively. This helps neutralizing the pad partially to reduce overshoot and undershoot. It uses scheme of detection of SE0 condition and single transition on either Dp or Dn pad and accordingly inject or drain charge from pad to reduce overshoot and undershoot. Although this paper discusses EOS issue in reference to USB2, it can be used for USB3 and other standards where such OS/US scenario occurs.

This paper is divided in to 7 sections. Section II describes SE0 signalling protocol in USB2 standard. Section III explains EOS issue specifically to USB2 application. Section IV explains principle of suppressing overshoot & undershoots. Section V discusses detailed circuit implementation. Section VI gives simulation results validating proposed EOS protection circuit. Finally, the work in this paper is summarized in section VII.

II. USB2-SE0 PROTOCOL

The Single Ended Zero (SE0) state in USB2 standard communication protocol is used to indicate end-of-packet (EOP). This EOP is signalled by driving Dp and Dn pads to logical low state for two bit times followed by driving the lines to the J state for one bit time. USB2 defines two states of differential signalling, J state and K state. The J state corresponds to logical high and logical low driven on pads Dp and Dn respectively. On the contrary, K state is defined as logical low and logical high driven on Dp and Dn pads respectively. The transition from SE0 state to the J state defines the end of data packet at the receiver. The J state is asserted for one bit time and then both the Dp and Dn output drivers are placed in high impedance state. All USB2 devices attach to USB through ports on specialized USB devices known as hubs. When the data packets pass through hub, EOP may get stretched by hub switching skews. This is known as dribble and lead to the case shown in fig. 1 b). The width of EOP is twice the bit duration and can be as low as one bit duration. USB2 has three transfer rates, high speed is 480Mbps, full speed is 12Mbps and low speed is 1.5Mbps. From these transfer rates we find bit duration for full speed to be 83ns and low speed 666ns. Considering timing variations due to differential buffer delay, rise and fall time mismatches, noise and other random effects, EOP width can be between 160ns and 175 ns for full speed and between 1.25us and 1.5us for low speed. As shown in fig. 1 b) it can be one bit duration where it may reduce as little as 82ns for full speed and 670ns for low speed. Our point of interest here is EOP since differential transitions are missing. Further to add we will be focusing only on full speed mode since it will have 3.3V signalling with rise and fall times as low as 4ns. The next section will make this intent clear to readers.

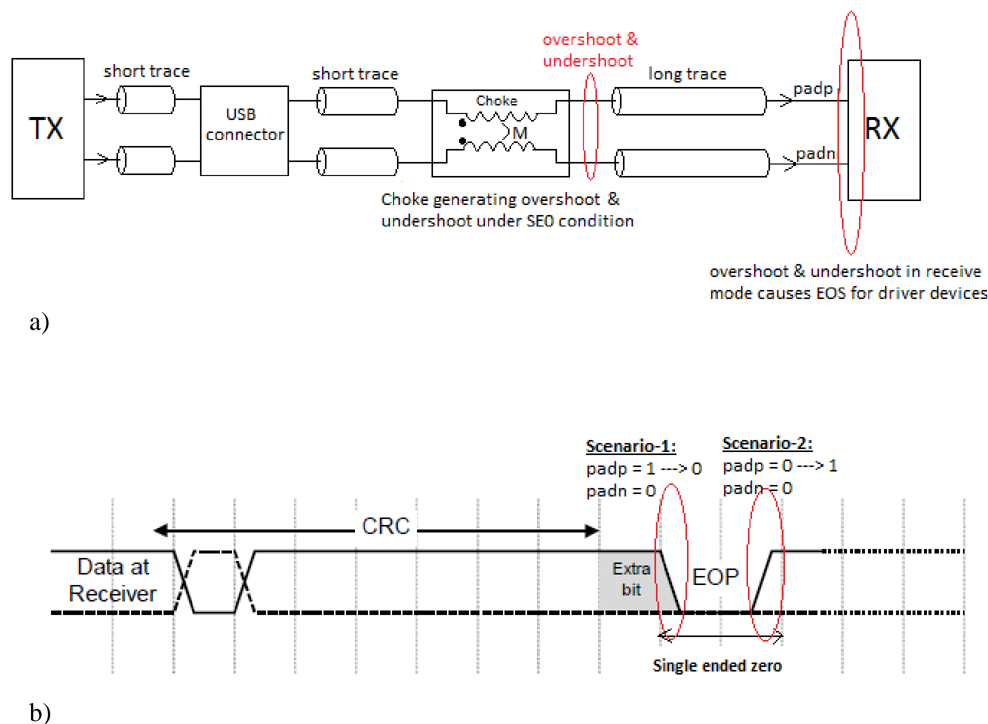

Fig. 1. (a) Application platform of USB2 and (b) SE0, EOP condition with highlighted scenario-1 and scenario-2.

III. An EOS Issue

One of the techniques to deal with EMI issue in serial interfaces is using mutually coupled inductor choke. Choke placement is closer to the output of transmitter following USB2 connector as shown in fig. 1 a). The differential signalling through choke is adjusted for 50% cross-over minimizing common mode noise. This in turn reduces common mode noise induced electromagnetic interference. However when single ended transition occurs on differential lines as shown in fig. 1 b), the same choke generates overshoot and undershoots due to inductive kick back. The effect is severe for high slew rates. In USB2 standard communication protocol single edge transition occurs in SE0 state as shown in fig. 1 b). The SE0 state in high speed does not generate overshoot and undershoot to stress the devices because its small swing signalling, 400mV. However full speed is 3.3V signalling with highest possible slew rate of 4ns hence generates excessive overshoot and undershoots. The low speed is also 3.3V signalling but fastest slew rate is 20ns hence overshoot and undershoots are not generated. The generated overshoot and undershoots propagate down the line to receiver. At receiving end, transmitter is tri-stated and sees these overshoot and undershoots. The drain-bulk, drain-source and drain-gate junction of 1.8V cascode transistor experience electrical over stress as depicted in fig. 2. As activity factor increases, the transistor devices see OS/US very often and degrade quite rapidly. This leads to change in device parameters like threshold voltage, transconductance and thereby finally affects the transmitter output impedance. USB2 defines transmitter output impedance specification to be 45 Ω +/- 5%. This specification may get violated over time leading to increased defects per million (DPM) number. To mitigate this reliability issue, EOS protection circuit is designed in Intel 22nm process. This EOS issue is divided in to two scenarios as shown in fig. 2. Scenario-1 is defined as padp making transition from high to low when padn is at logic low level. This scenario corresponds to undershoot on both padp and padn. Scenario-2 is defined as padp making transition from logic low level to logic high level and padn is still at logic low level. This scenario corresponds to overshoot on padp and undershoot on padn. These two scenarios occur due to tightly coupled two inductors of 200nH present in choke. Observed overshoot may go as high as 4.2V and undershoot as low as -0.6V. These voltage levels are high enough to violate the EOS limits of cascode devices of transmitter. Although not shown in fig. 3, there could be other structures connected to pads like receiver circuit, ESD protection circuit. These other devices/components connected to pad also undergo electrical stress and may degrade over time. This requires reliability simulations like “Aging” to determine amount of degradation over time and caused defects per million. Removing on board choke solves this EOS issue but results in to increased EMI. Alternative solutions to suppress EMI are not applicable USB2 application. For example Spread spectrum clocking for data bit stream may solve both EMI and EOS issue but violates the 500ppm requirement of USB2.

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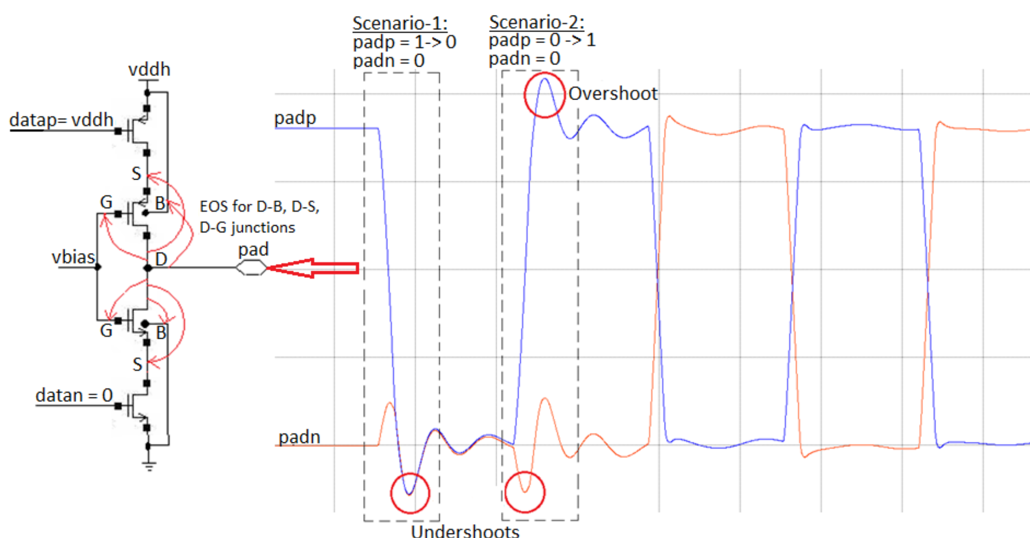
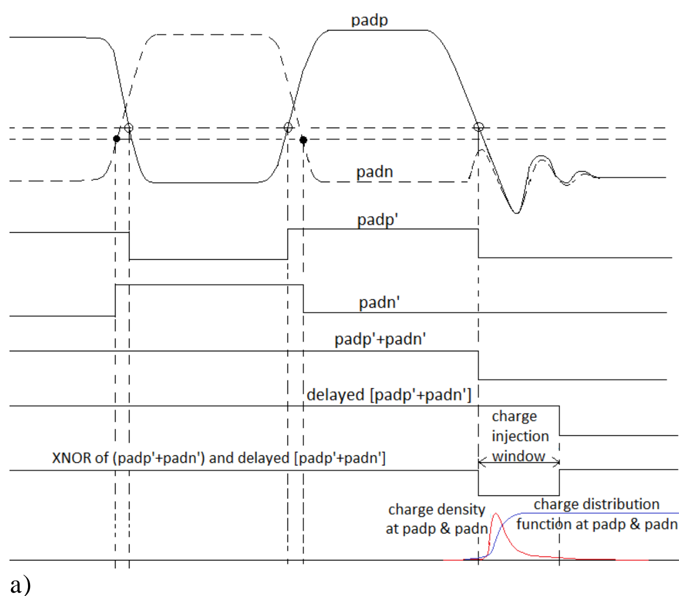


Fig. 2. On receiving side, electrically over stressed tri-stated output driver due to subjected overshoot and undershoots.

IV. Principle of OS/US Suppression

This invention detects overshoot & undershoot scenarios ahead of time and injects the charge in to pad when undershoot occurs and drains the charge from pad when overshoot occurs. The basic idea of charge injection and drain is illustrated in this section. Here we will be considering two different scenarios to address the issue. Scenario-1 is when padp makes transition from logic high to logic low and padn is at logic low level during EOP window. Scenario-2 is when padp makes transition from logic low level to logic high level and padn is at logic low level during EOP window.



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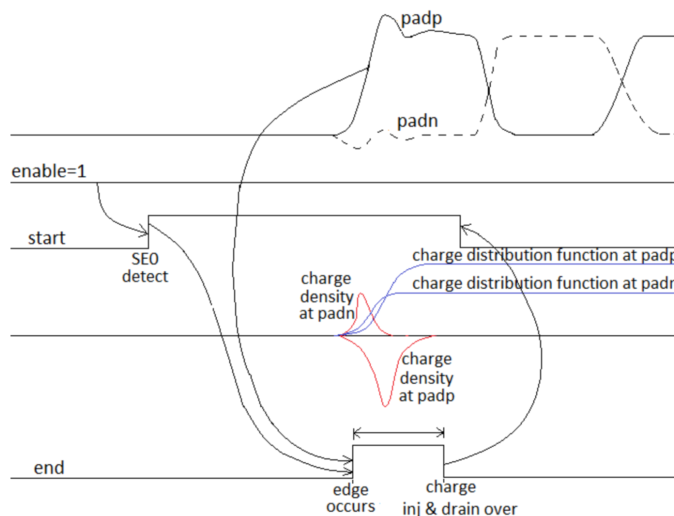


b)

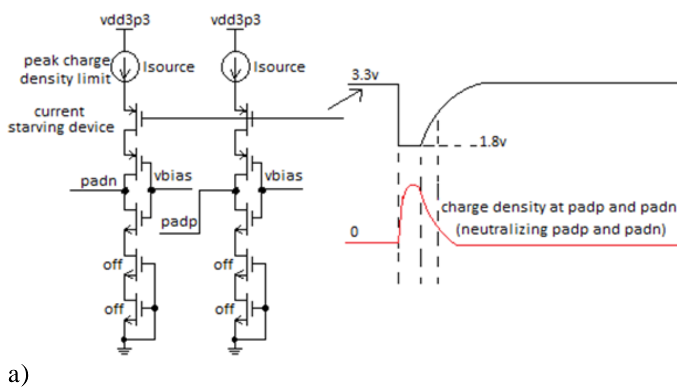
Fig. 3. (a) Scenario-1 solution and (b) scenario-2 solution waveforms.

<u>Scenario-1:</u> (padp = 1→0, padn =0)

In SE0 state (FS mode) of USB2 protocol padn is low and padp transitions from high to low for every end of packet (EOP). This scenario causes single edge transition and thereby undershoot on padp and padn. Two different low threshold detectors are used to detect signals padp and padn going low. The inverted outputs of these detectors are lebelled as padp’ and padn’. The OR logic of these two signals results in logic low level when padn=0 and padp makes transition from high to low (crosses low threshold). The XNOR logic of this signal with its delayed version creates a window for charge injection. The charge injection & drain circuit is enabled in this window injecting a controlled amount of charge in to padp and padn to neutralize the pads partially to lower undershoot. The total amount of charge injected can be found by integrating charge density function. This can also be given as charge distribution function with respect to time. The final steady state value of

this function is the total amount of charge injected as shown in fig. 3 a). The toal amount of charge injected can be controlled by peak current limiter and charge injection window length. The exact nature of charge density is controlled by controlling rise and fall slew at input of current starved devices. This input is exponential in nature and derived from output of RC circuit.

The charge injection mechanism is as illustrated in fig. 4 a). The constant current sources limits the peak charge density for controlled power consumption. The input to devices is slew controlled for rising edge to generate the required charge density profile. This rising slew is exponential in nature and generated by RC circuit. Thus injected charge in to pads lowers the undershoot.



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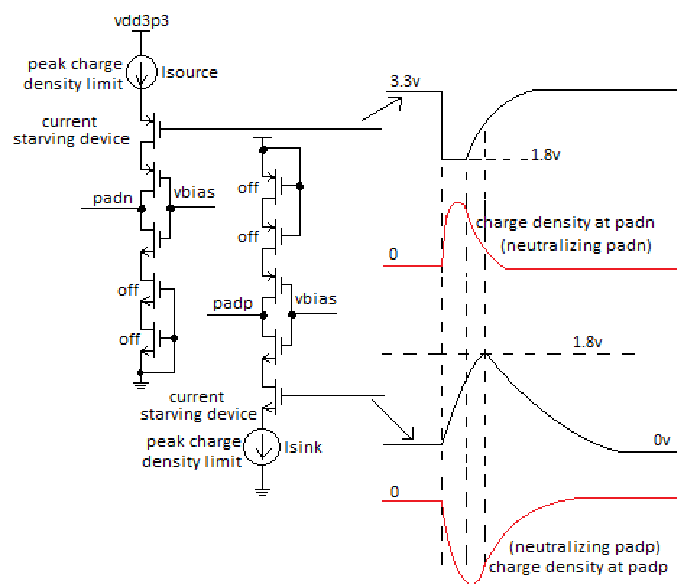

b)

Fig. 4. Implementation of (a) scenario-1 and (b) scenario-2 circuit.

<u>Scenario-2:</u> (padp = 0→1, padn =0)

As shown in fig. 3 b) the FSM part of this invention detects the SE0 condition of USB2 protocol where single edge transition occurs at the beginning of packet. Upon SE0 state detection it asserts start signal high. This start signal enables charge injection & drain circuit. The charge injection & drain circuit detects rising edge on padp and asserts end signal high. The controlled amount of charge is drained from padp and injected in padn lowering the overshoot and undrshoot respectively. Once charge injection and drain action is over it asserts end signal low. This in turn causes start signal to go low disabling the charge injection & drain circuit. The total amount of charge injected/drained can be found by integrating charge density function. This can also be given as charge distribution function with respect to time. The final steady state value of this function is the total amount of charge injected/drained as shown in fig. 3 b). The toal amount of charge injected/drained can be controlled by peak current limiter and charge injection window length. The exact nature of charge density is controlled by controlling rise and fall slew at input of current starved devices. This input is exponential in nature and derived from output of RC circuit.

The charge injection & drain mechanism is as illustrated in fig. 4 b) where Isource and Isink are the constant current source and sink respectively. These sources limits the peak charge density for controlled power consumption. The input signals slew for current starving devices are exponential in nature and are adjusted by RC charging and discharging circuits. The slew timing is designed such a way that required charge injection & drain profile can be generated to partially neutralize the pad.

Under both scenarios the charge density and distribution function can be given by,

$$\text{Charge density function, } i(t) = \frac{dq}{dt}$$

$$\text{Charge distribution function, } q(t) = \int_0^t i(t)dt = \int_0^t dq$$

The total amount of charge injected/drained can be computed as

$$\text{Total charge injected/drained} = \int_0^\infty i(t)dt = \int_0^\infty dq$$

Since controlled amount of charge is injected/drained it results in controlled power consumption. This invention addresses issue exactly where it is needed (i.e. circuit not active on every edge) hence it provides optimum power solution.

V. EOS Protection Circuit

The top level block diagram of EOS protection circuit is shown in fig. 5 a). It contains charge injection/drain block and finite state machine block. Further charge injection/drain block is expanded in fig. 5 b) where it contains sub-blocks, edge detection, logic circuit, charge injection/drain legs, RC based slew control and peak current limiter. The finite state machine block is sub divided in to SE0 detector, digital glitch filter and Mealy type finite state machine as shown in fig. 5 c). On the top hierarchy, padp and padn signal goes to charge injection/drain block and clock and enable signals act as input to finite state machine block. The output “end” from charge injection/drain block goes as input to finite state machine block and finite state machine output “start” feeds back to charge injection/drain block. The detailed circuit

schematic is as shown in fig. 9. The circuit operation is as explained below in reference to two different scenarios.

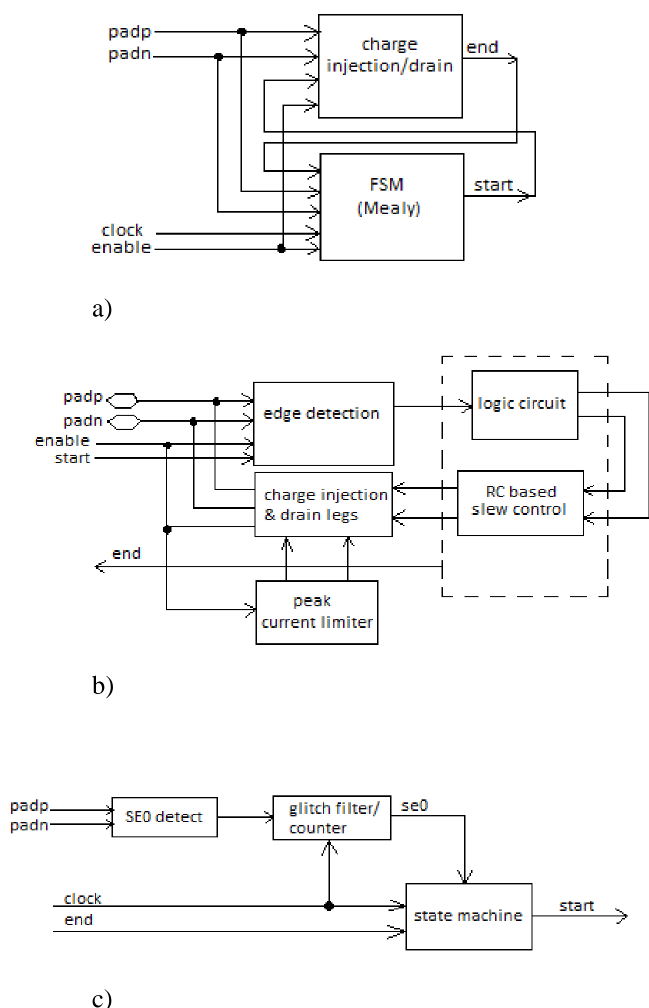

Fig. 5. (a) Top level block diagram of EOS protection circuit, (b) block diagram of charge injection/drain circuit, and (c) SE0 detect and finite state machine block diagram.

<u>Scenario-1</u>: (padp = 1→0, padn =0)

In this scenario padn signal is low and padp signal transitioning from high to low is detected by low threshold detectors. The low threshold detectors are basic inverters tuned to threshold values which are very low. The detector on padp has threshold of Vt1 and detector on padn has threshold value of Vt2. Here Vt2 is designed to be less than Vt1. The low threshold is achieved by making PMOS device weaker than NMOS device. Vt2 < Vt1 is ensured by making PMOS of detector-2 much weaker than PMOS of detector-1 and NMOS of detector-2 much stronger than NMOS of detector-1. Output of these detectors go low when signal goes above these threshold values. padp' and padn' are the inverted output of these signals as shown in fig. 3 a). The OR logic of these signals padp' and padn' goes low when padn is low and padp also goes low (crosses Vt1). XNOR logic of this signal with its delayed version gives output low. This is the window where charge injection & drain circuit is enabled and charge injection in to padp and padn is done to partially neutralize the pads. This in turn lowers undershoot. Here very precise detection of threshold values (~400mV) is not required and hence low power inverter based detectors are used.

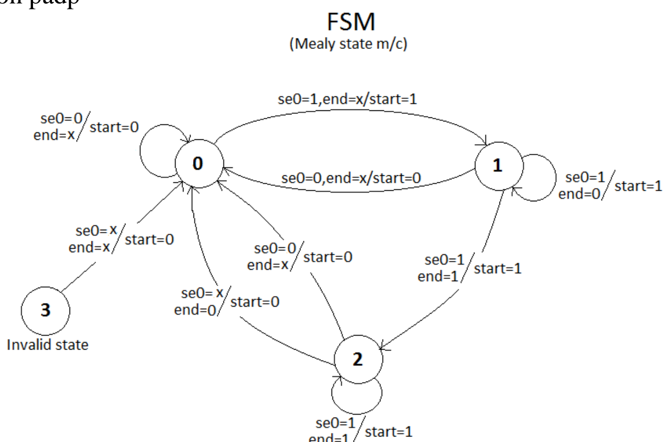

Fig. 6. State diagram of Mealy type finite state machine.

<u>Scenario-2:</u> (padp = 0→1, padn =0)

The FSM part of this invention detects the SE0 state in USB2 protocol by detecting padp = padn = 0 and asserts start signal high enabling charge injection & drain circuit. Charge injection & drain circuit detects the rising edge and creates a required window to inject/drain the charge in to/from padn/padp. This window is defined by end signal which goes high when lower threshold of edge is detected and goes low when charge injection & drain action is over. Charge injection & drain circuit asserts end signal low after injecting and draining the charge. This signal goes as input to FSM which in turn de-asserts the start signal to charge injection circuit disabling it. The timing diagram is as shown in fig. 3 b). The state machine design is based on state diagram described in fig. 6. This state machine has two inputs, 'se0' and 'end' and total 4-states with one invalid state. The output of state machine, 'start' depends upon present state and present inputs (Mealy type) [2]. There is a possibility of state machine entering in to invalid state due to glitch/noise or power ramp up. Under such circumstances the state machine brings itself back to valid state from invalid state as shown in fig. 6. This state machine asserts start signal high only when it detects SE0 state and de-asserts start signal when end signal goes low after charge injection & drain. As shown in fig. 9 the finite sate machine takes in stepped down padp and padn signals and detects SE0 state by detecting both padp = padn =0 levels. The two bit counter is used to count clock pulses until count reaches to $(11)_2$. This ensures that padp = padn =0 for long enough time and indeed its SE0 state. This removes glitches and avoids false SE0 detection hence can be called as digital glitch filter. When Charge injection & drain circuit is enabled, the comparator output goes high when rising edge occurs on padp. This comparator is folded cascode architecture with differential inputs and single ended output [3] [4]. The stepped down padp and padn signals goes as input to this comparator. The input devices are purposefully skewed so that output switches high when padp signal goes above padn signal by ~100mv. The differential input comparator architecture is used to make design more robust against input common mode noise. The upper threshold of rising edge on padp is detected at ~2.5V by hysteresis circuit. The upper threshold detection is necessary

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due to large range of rise time specification in Full speed (FS) mode of USB2 protocol. The rise time can be from 4ns to 20 ns in FS mode of USB2. These threshold circuits help to create window for charge injection & drain. Inverter based delay line is used to stretch this window further by some margin since overshoot lasts for ~5ns on padp after upper threshold detection. The charge injection & drain mechanism is as illustrated in fig. 4 where Isource and Isink are the constant current source and sink respectively. These sources limits the peak charge density. The input signal slew for current starving devices is adjusted by RC based charging and discharging circuits. The slew timing is designed such a way that required charge injection & drain profile can be generated to partially neutralize the pad. The capacitors in RC circuit are implemented as MOS caps and resistors by poly. The poly resistor variation is minimized by six bit calibration code. This improves precision of charging and discharging time bases generated by RC circuits. The peak injected & drained charge density becomes very high under fast corner and damps the overshoot to very low value. This unnecessarily increases power consumption and results in overdesign. This invention limits the peak current optimizing design for power consumption. The peak current limit circuit is basic current mirror circuit which takes in constant current and mirrors to charge injection & drain legs so that peak current never exceeds certain value under fast process corner. The charge injection & drain circuit uses level shifter to shift input signalling levels from 0V ->1.8V to 1.8V -> 3.3V for PMOS devices comprising charge injection leg. This level shifting is necessary because the devices used are 1.8V devices in 3.3V domain.

Power advantage:

USB2.0 specification [5] defines FS frame interval to be 1ms and USB2.0 FS speed = 12Mbps [UI=83.33ns] => 1ms/83.33ns = 12000 bits/frame

USB2.0 spec, max transfers/frame = 150

Hence 150 EOP events in 1ms frame (OS/US happens only during EOP).

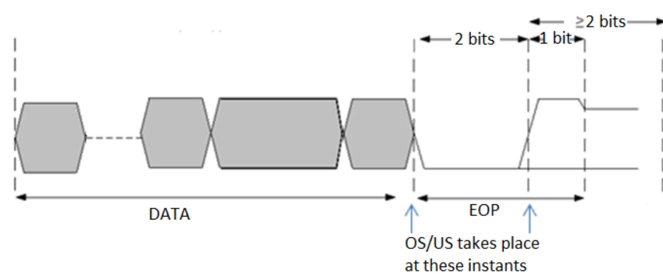

Fig. 7. USB2.0 FS data packet format.

i.e. 150 EOP events for 12000 bits => 1-EOP/80bit

Total active power consumption of this EOS protection circuit is 4.6mW under worst case PVT. The comparator is the only static power consuming block which consumes 0.2mW of power. Remaining 4.4mW of switching/dynamic power is consumed by state m/c and other sub blocks.

Hence 1-EOP/80 bits => 4.6mW/80bits => 57.5uW/bit

Assume 1-EOP/1000bits => 4.6mW/1000bits => 4.6uW/bit

This unique combination of analog, digital components and intelligence (FSM) differentiates it from conventional architectures. The added intelligence (FSM) saves significant amount of power since it enables circuit only when required.

VI. Simulation Results

A test set up shown in fig. 1 a) is prepared with appropriate SPICE models for different components [6] and simulations are run. The test set up is comprised of

1. TX modelled as ideal pulse generator and 45Ω impedance with +/-5% tolerance.
2. Short traces modelled by transmission line model
3. USB connector model
4. Choke model
5. Long, 14-inch trace modelled by transmission line model
6. RX modelled by 10pF in parallel with 15K-Ohm
7. EOS Protection Circuit in Intel 22nm process

Fig. 8 a) shows overshoot and undershoot caused by on board choke during SE0 EOP window in full speed mode. The observed overshoot is 4.2V and undershoot is -0.6V. Fig. 8 b) shows reduced overshoot and undershoot by proposed EOS protection circuit. In typical conditions overshoot and undershoot is reduced to 3.3V and -0.24V respectively. Fig. 10 shows worst case, across all PVT conditions overshoot and undershoot reduced as low as 3.7V and -0.34V respectively.

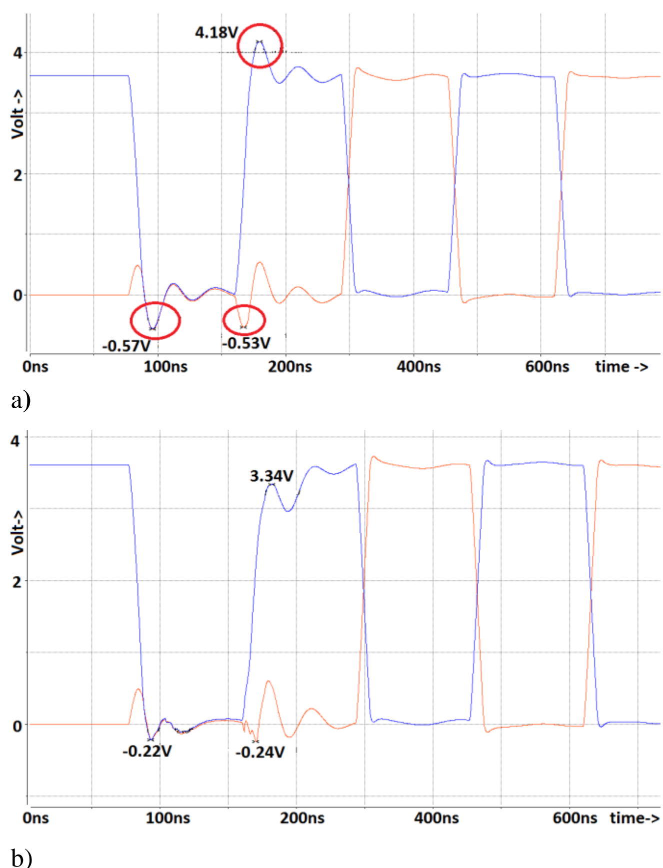

Fig. 8. (a) Typical simulation result without EOS protection circuit, (b) typical simulation result with EOS protection circuit.

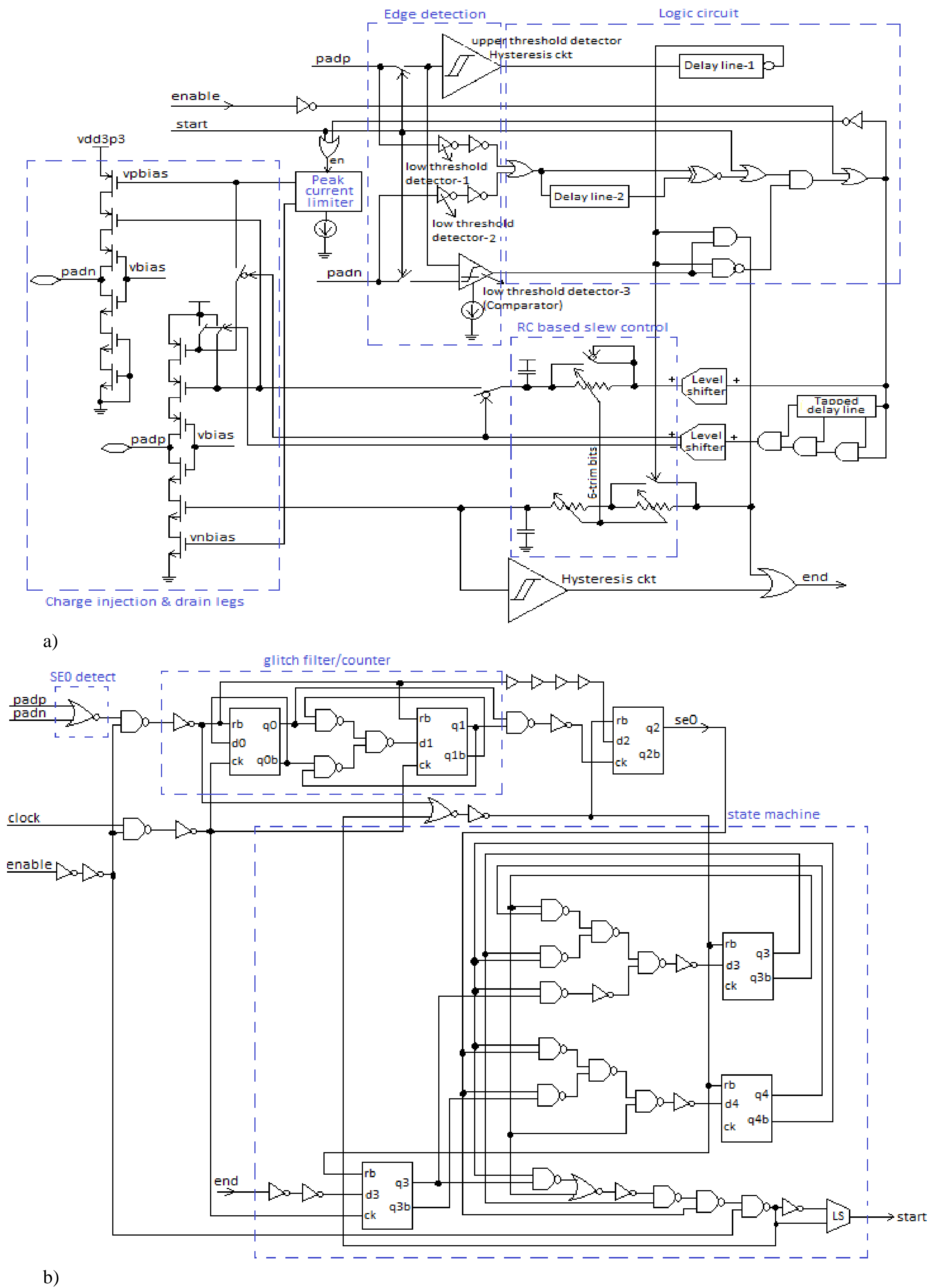

Fig. 9. (a) Charge injection and drain circuit and (b) Mealy type finite state machine.

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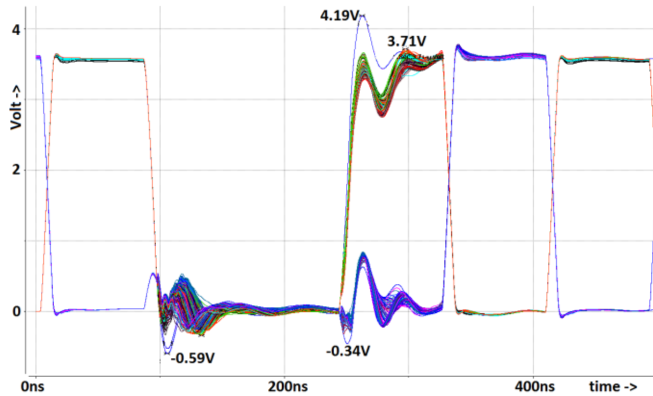

Fig. 10. PVT simulation result with EOS protection circuit.

PVT conditions consider all 15 corners, ±10% variation on 1.8V & 3.3V supply, and Temperature variation from -40°C to 125°C.

VII. Conclusion

This paper demonstrates design solution to address emerging issues with advanced sub-micron process technology. It uses some intelligence to detect the EOS issue and addresses exactly where and when it's needed. This makes it very low power design. This EOS protection circuit can be used for future submicron technologies like 14nm, 10nm and onwards.

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