Proceedings of the International MultiConference of Engineers and Computer Scientists 2015 Vol II,
IMECS 2015, March 18 - 20, 2015, Hong Kong

A Closed-Loop High-Gain Multiphase-Switched-Capacitor-Inductor Step-Up DC-DC Converter

Yuen-Haw Chang and Chen-Han Tsai

***Abstract*—A closed-loop scheme of a high-gain multiphase-switched-capacitor-inductor (MSCI) converter is proposed by using a phase generator and a pulse-width-modulation-based (PWM-based) gain compensator for step-up DC-DC conversion and regulation. In the power part of MSCI, there is a 3-stage serial-parallel switched-capacitor (SC) circuit plus combining a switched-inductor (SI) resonant booster. Based on the scheduled multiphase operating cyclically, the maximum step-up gain can reach to 8/(1-D), where D is the duty cycle of PWM, i.e. the MSCI can boost the output Vo up to 32 times voltage of source Vs when D=0.75. Further, the PWM technique is adopted not only to enhance output regulation for the compensation of the dynamic error between the practical and desired outputs, but also to reinforce output robustness against source or loading variation. Finally, the closed-loop MSCI is designed by OrCAD SPICE, and is simulated for some cases: steady-state and dynamic responses (source/loading variation). All results are illustrated to show the efficacy of the proposed scheme.**

***Index Terms*— high-gain, multiphase-switched-capacitor-inductor, step-up converter, pulse-width-modulation.**

I. Introduction

Recently, with the rapid development of power electronics technology, step-up DC-DC converters are emphasized more and more widely for the electricity-supply applications, such as photovoltaic system, fuel cell, and X-ray systems. Generally, these power electronics converters are always asked for a small volume, a light weight, a high efficiency, and a better regulation capability.

Based on the structure of charge pump, an SC converter is one of the good solutions to low power and high gain DC-DC conversion. The advantage is that this kind of SC converters uses semiconductor switches and capacitors only. However, most SC circuits have a voltage gain proportional to the number of pumping capacitors. In 1976, Dickson charge pumping was proposed based on a diode-chain structure of pumping capacitors [1]. It provides voltage gain proportional to the stage number of pumping capacitor, and the detailed dynamic model and efficiency analysis were discussed [2]. But, its drawbacks include the fixed voltage gain and the larger device area. In 1993, Ioinovici *et al.* suggested a voltage-mode SC with two symmetrical capacitor cells working complementarily [3]. In 1997, Zhu and Ioinovici performed a comprehensive steady-state analysis of SC [4]. In 2009, Tan *et al.* proposed a low-EMI SC by interleaving control [5]. In 2011, Chang proposed an integrated SC step-up/down DC-DC/DC-AC converter/inverter [6]-[7]. However, the drawback of this kind of SC converters is many pumping capacitor counts, especially for extending the stage a higher voltage gain.

Generally, a conventional SI booster consists of one magnetic inductor and one resonant capacitor, and it can provide the voltage gain of 1/1-D. But, the inductor may result in electromagnetic interference (EMI) problem. Here, for the boost-type converters, there are several topologies introduced as follows. (i) The quadratic cascade boost converter can provide a high voltage gain and this gain is squared times higher than that of the simple booster [8]-[9]. (ii) Based on the scheme of the simple booster, the fly-back converter uses one switch and coupled-inductors to achieve the high-gain conversion [10]-[11]. However, it often leads to the worst EMI problem due to coupled-inductor. (iii) The diode-clamped step-up converter can provide the voltage gain (proportional to the number of stage), and the stage count can be extended by adding capacitors and diodes [12]. But, it might result in the larger voltage-drop consumption due to the cut-in voltage of diodes connected in series.

According to the above descriptions, for achieving a compromise among volume size, component count, and voltage gain, the high-gain MSCI converter is proposed here by utilizing the contents of [13]-[14] for the closed-loop step-up DC-DC conversion and regulation.

II. Configuration of MSCI

Fig. 1 shows the overall circuit configuration of the closed-loop multiphase-switched-capacitor-inductor (MSCI) step-up DC-DC converter, and it contains two major parts: power part and control part for achieving the closed-loop high-gain step-up DC-DC conversion and regulation.

Manuscript received December 3, 2014. This work is supported in part by Ministry of Science and Technology of Taiwan, R.O.C., under Grant MOST 103-2221-E-324-039.

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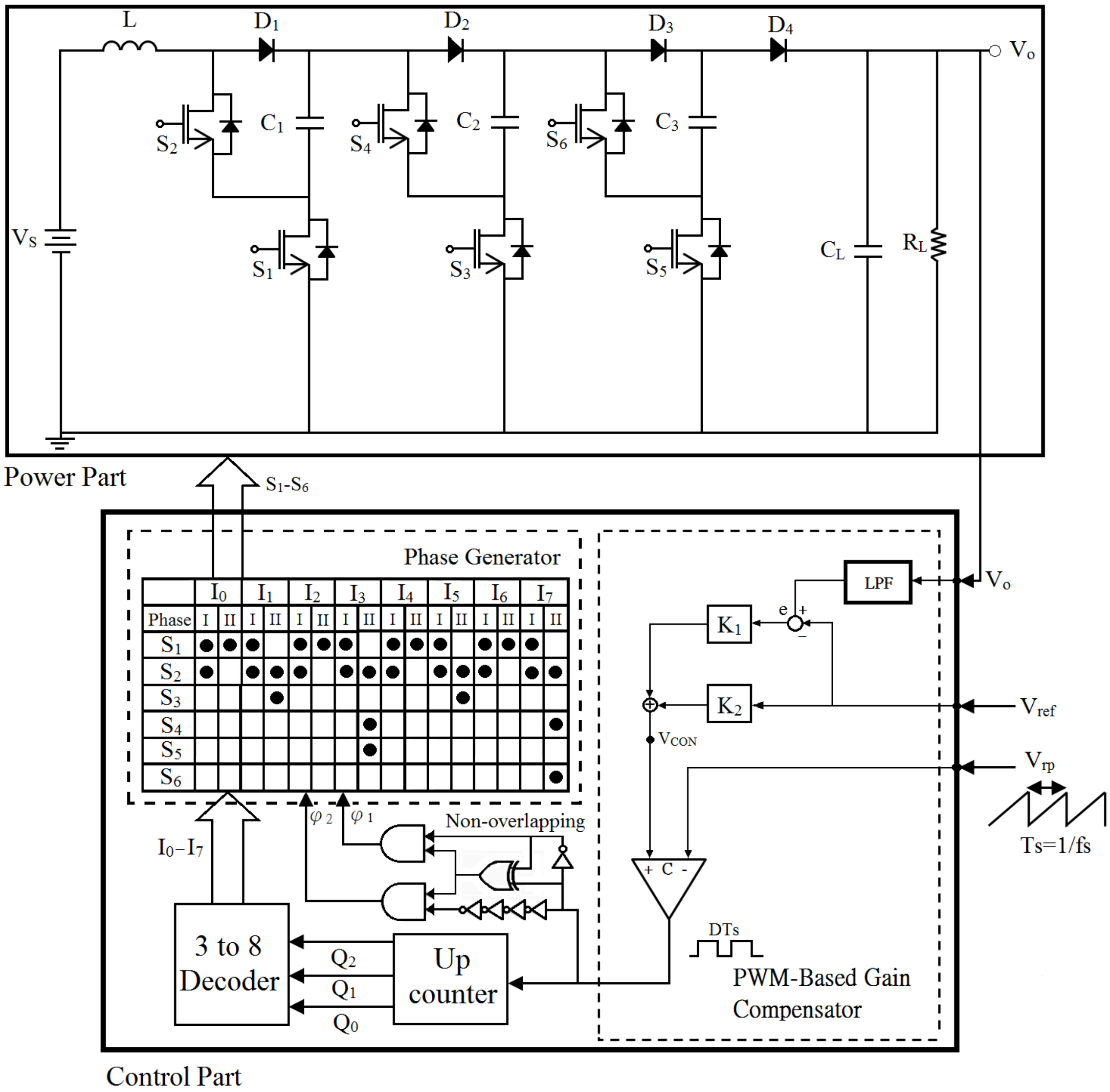


Fig. 1. Configuration of the closed-loop MSCI.

A. Power part

The power part of MSCI is shown in the upper half of Fig.1, and is composed of a multiphase serial-parallel switched-capacitor circuit plus combining a switched-inductor booster. The converter consists of one inductor (L), six switches (S_1-S_6), three pumping capacitors (C_1-C_3), one output capacitor (C_L) and four diodes (D_1-D_4), where each capacitor has the same capacitance C (C_1=C_2=C_3=C). Fig. 2 shows the theoretical waveforms of MSCI in one switching cycle T_S (T_S=1/fs, fs: switching frequency). A cycle T_S includes eight steps (Step I_0-I_7), and each step has two phases (Phase I and Phase II) with the different time duration: DT_S and (1-D)T_S, where D is the duty cycle of PWM control. The operations for Step I_0-I_7 are described as follows.

(i) Step I_0:

(a)Phase I: Let S_1, S_2 turn on, and the others be off. The diodes D_1-D_4 are all off. The current-flow path is shown in Fig. 3(a). The inductor L is charged by source V_S, and the current of L is raising just like the waveform of i_L as in Fig. 2.

(b)Phase II: Let S_1 turn on, and the others be off. The diodes D_1 is on, and D_2-D_4 are all off. The current-flow path is shown in Fig. 3(b). The capacitor C_1 is charged by Vs in series together with the inductor voltage V_L, i.e. transferring the previous energy stored in L into C_1. Thus, the maximum steady-state voltage of C_1 can reach towards the value of Vs/(1-D).

(ii) Step I_1:

(a)Phase I: The operation is totally identical to Phase I of Step I_0.

(b)Phase II: Let S_2, S_3 turn on, and the others be off. The diode D_2 is on, and D_1, D_3, D_4 are off. The

ISBN: 978-988-19253-9-8
ISSN: 2078-0958 (Print); ISSN: 2078-0966 (Online)

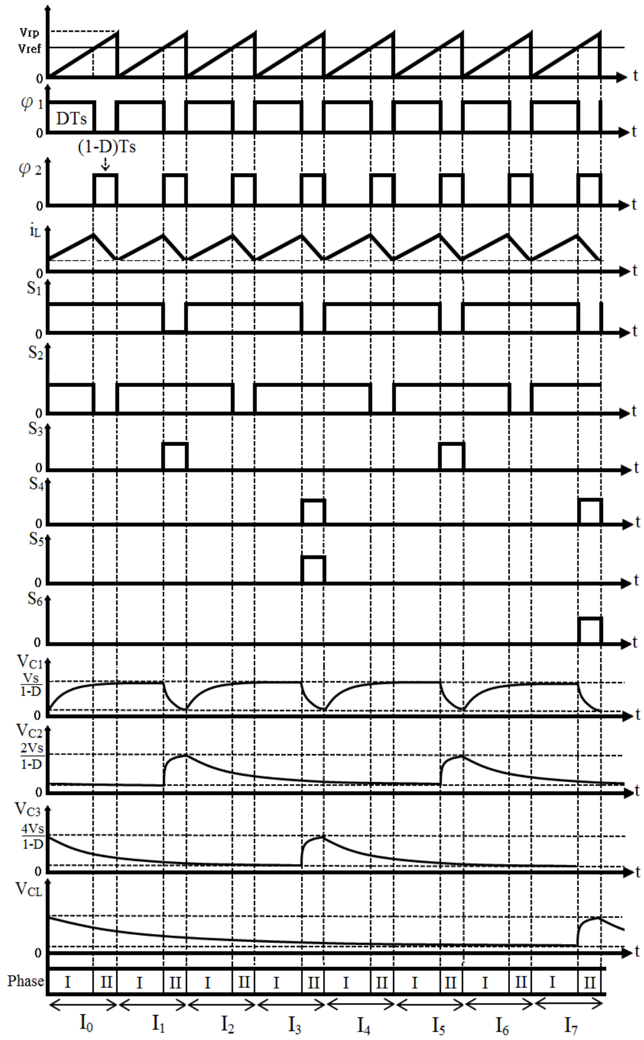


Fig.2. Theoretical waveforms of MSCI.

TABLE I
Circuit parameters of MSCI.

Supply source (Vs)	5V
Pumping capacitor (C_1~C_3)	20uF
Output capacitor (C_L)	200uF
Inductor (L)	100mΩ
Switching frequency (fs)	100kHz
Diodes: D_1~D_4	120NQ045
ON-state resistance of MOSFETs (Ron)	0.03Ω
Load resistor (R_L)	500Ω
Gain Compensation (K_1, K_2)	K_1=20, K_2=0.7

current-flow path is shown in Fig. 3(c). The capacitor C_2 is charged by Vs in series together with V_L and V_{C1}, i.e. transferring the previous energy stored in L and C_1 into C_2. Thus, the maximum steady-state voltage of C_2 can reach towards the value of 2Vs/(1-D).

(iii)Step I_2 :

The operations of Phase I and Phase II are totally identical to Step I_0.

(iv)Step I_3 :

(a)Phase I: The operation is totally identical to Phase I of Step I_0.

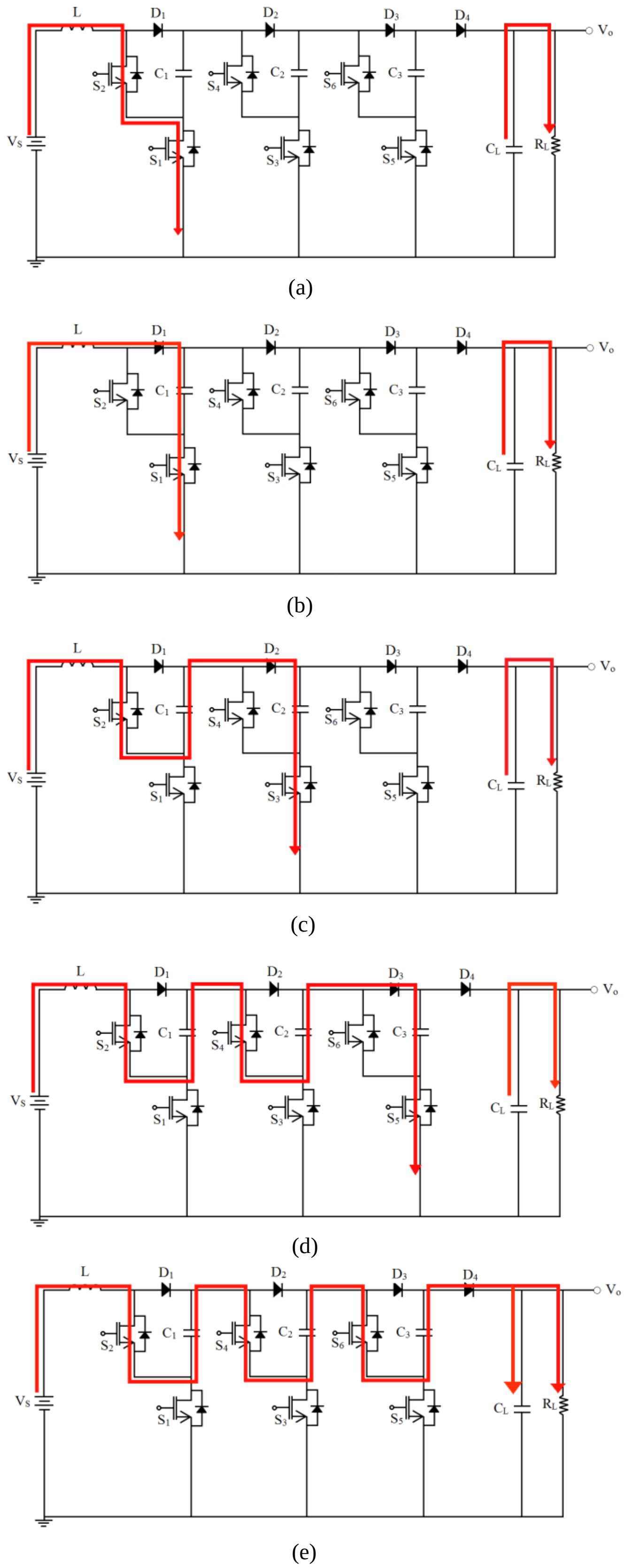


Fig. 3. Topologies for (a)Phase I of I_0-I_7; (b)Phase II of I_0, I_2, I_4, I_6; (c)Phase II of I_1, I_5; (d)Phase II of I_3; (e)Phase II of I_7.

(b)Phase II: Let S_2, S_4, S_5 turn on, and others be off. The diode D_3 is on, D_1, D_2, D_4 are all off. The current-flow path is shown in Fig. 3(d). The capacitor C_3 is charged by Vs in series with

V_L , V_{C1} and V_{C2} together, i.e. transferring the previous energy stored in L, C_1, C_2 into C_3 Thus, the maximum steady-state voltage of C_3 can reach towards the value of 4Vs/(1-D).

(v)Step I_4 :

The operations of Phase I and Phase II are totally identical to Step I_0.

(vi)Step I_5 :

The operations of Phase I and Phase II are totally identical to Step I_1.

(vii)Step I_6 :

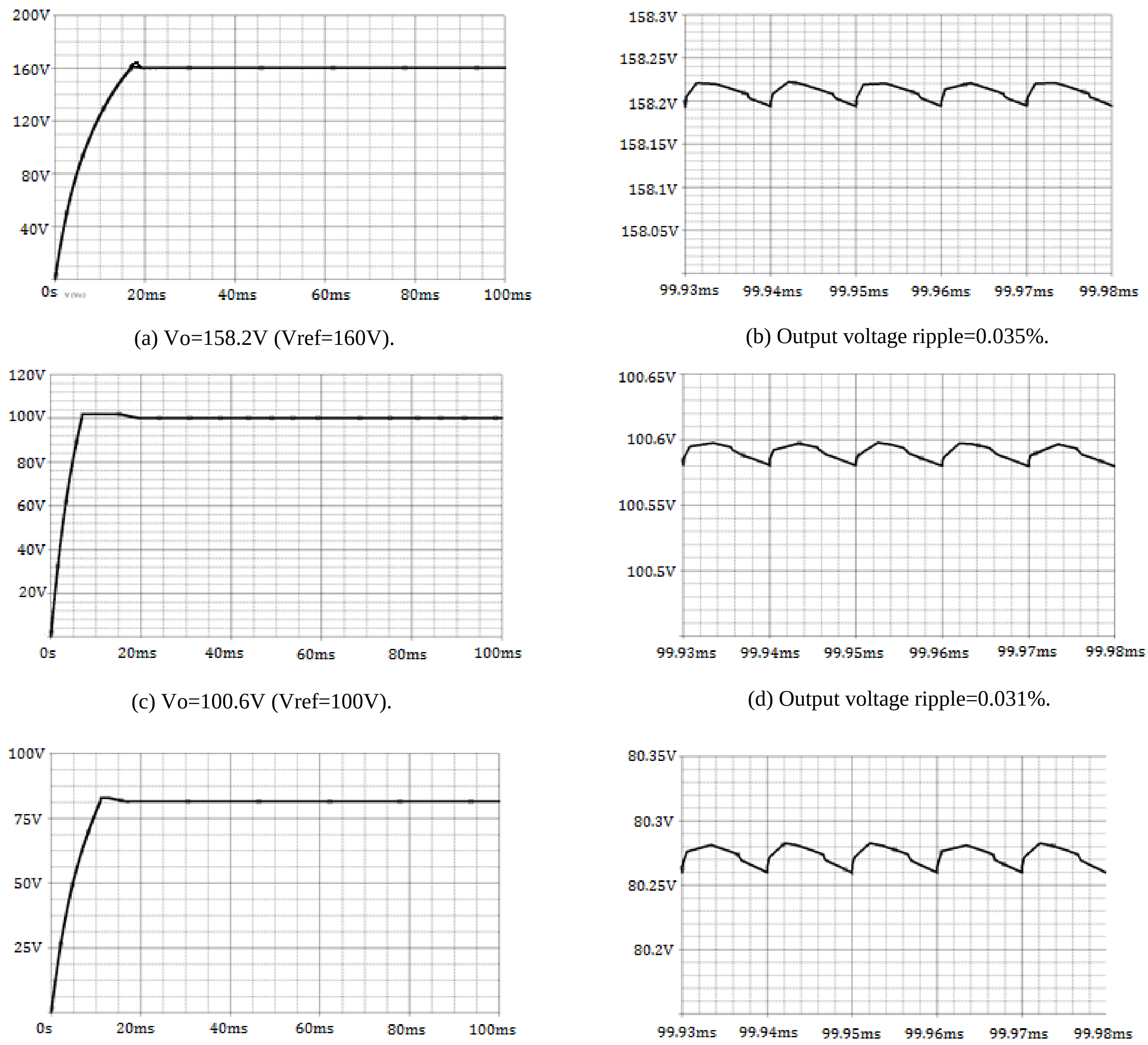
The operations of Phase I and Phase II are totally identical to Step I_2.

(viii)Step I_7 :

(a)Phase I: The operation is totally identical to Phase I of Step I_0.

(b)Phase II: Let S_2, S_4, S_6 turn on, and the others be off. The diode D_4 is on, and D_1-D_3 are all off. The current-flow path is shown in Fig. 3(e), and is going from source Vs, through L, C_1, C_2, C_3, to output capacitor C_L and load R_L. This topology has the connection in series of Vs, V_L, V_{C1}, V_{C2}, and V_{C3} in order to provide a higher voltage for transferring the energy into the output terminal (C_L and R_L).

Based on the cyclical operations of Step I_0-I_7, the overall step-up gain can reach to the value of $2^3/(1\text{-}D)$ theoretically. Extending the capacitor count, the gain can be boosted into the value of $2^n/(1\text{-}D)$, where n is the number of pumping capacitors.



(a) Vo=158.2V (Vref=160V).

(b) Output voltage ripple=0.035%.

(c) Vo=100.6V (Vref=100V).

(d) Output voltage ripple=0.031%.

(e) Vo=80.26V (Vref=80V).

(f) Output voltage ripple=0.025%.

Fig. 4. Steady-state responses of MSCI.

ISBN: 978-988-19253-9-8
ISSN: 2078-0958 (Print); ISSN: 2078-0966 (Online)

B. *Control part*

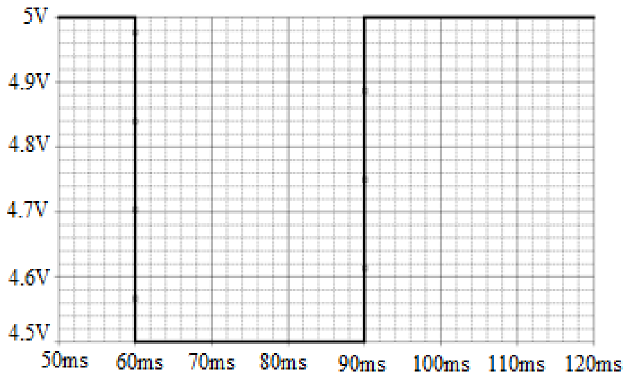
The control part of MSCI is shown in the lower half of Fig.1. It is composed of low-pass filter (LPF), a PWM-based gain compensator, an up counter, a 3 to 8 decoder and phase generator. From the controller signal flow, the feedback signal Vo is fed back into the OP-amp LPF for high-frequency noise rejection. Next, the control signal Vcon (related to the error signal e=Vref-Vo via gains K_1 and K_2) is compared with the ramp Vrp to generate the duty-cycle signal DTs of PWM. And then, the signal DT_S is sent to the non-overlapping circuit for producing a set of non-overlapping phase signals: φ 1 and φ 2 for the control of Phase I and II. Also, the signal DT_S is sent to the up counter and 3 to 8 decoder for obtaining a set of step signals: I_0, I_1, I_2, I_3, I_4, I_5, I_6, and I_7 for the driver of multiphase operation as mentioned above. With the help of these signals: φ 1, φ 2, and I_0-I_7, the phase generator (realized by digital logic gates) can generate the driver signals of switches S_1-S_6 just like the waveforms of Fig. 2. The main goal is to generate the driver signals of these MOSFETs for the different topologies as in Fig. 3(a)-(e), and further the closed-loop control can be achieved via the PWM-based compensator and phase generator in order to improve the regulation capability of this converter.

III. EXAMPLES OF MSCI

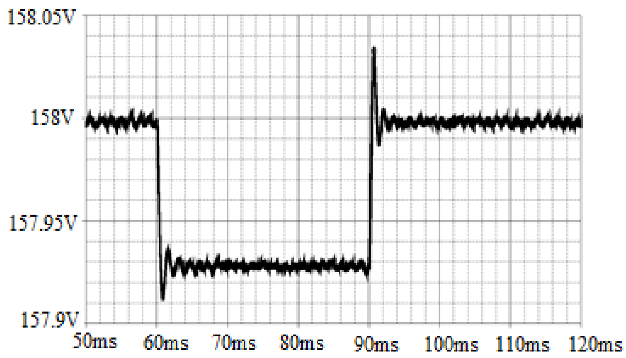
In this section, based on Fig. 1, the closed-loop proposed converter is designed and simulated by OrCAD SPICE tool. The results are illustrated to verify the efficacy of the proposed converter. In this MSCI, the maximum step-up gain can reach to 8/(1-D), where D is the duty cycle f PWM, i.e. the maximum output voltage is reaching about 160V when D=0.75 and Vs=5V. This converter is preparing to supply the load R_L=500Ω, and the relevant circuit parameters are listed in Table I. For checking closed-loop performances, some cases will be simulated and discussed, including: (i) steady-state responses, and (ii) dynamic responses (source variation/ loading variation).

(i) Steady-state responses:

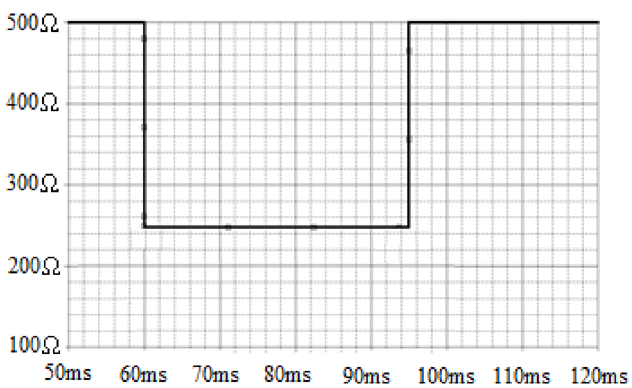
The closed-loop MSCI converter is simulated for Vref=160V/100V/80V respectively, and then these output results are obtained as shown Fig. 4(a)-(b) / Fig. 4(c)-(d) / Fig. 4(e)-(f). In Fig. 4 (a), it can be found that the settling time about 20ms, and the steady-state value of V_O is really reaching 158.2V, and the converter is stable to keep V_O following Vref (160V). In Fig. 4 (b), the output ripple percentage is measured as rp=$\Delta V_O/V_O$=0.035%, and the power efficiency is obtained as η =98.8%. In Fig. 4(c), it can be found that the settling time is smaller than 20ms, and the steady-state value of V_O is really reaching 100.6V, and the converter is stable to keep V_O following Vref (100V). In Fig. 4(d), the output ripple percentage is measured as rp=$\Delta vo/V_O$= 0.031%, and the power efficiency is obtained as η=99.1%. In Fig. 4(e), it is found that the settling time is smaller than 20ms, and the steady-state value of V_O is really reaching 80.26V, and the converter is stable to keep V_O following Vref (80V). In Fig. 4(f), the output ripple percentage can be easily found as rp = $\Delta vo/V_O$=0.025%, and the power efficiency is obtained as η= 99.4%. These results show that this closed-loop step-up converter has a high voltage gain and a good steady-state performance.



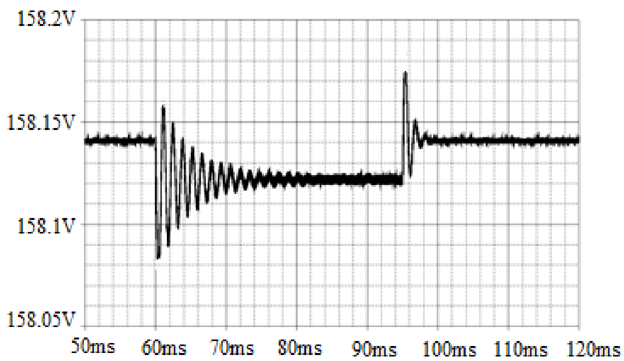
(a) Source: Vs=5V→4.5V→5V.



(b) Output:Vo (Vref=160V).



(c) Load R_L=500Ω→250Ω→500Ω.



(d) Output:Vo (Vref=160V).

Fig. 5. Dynamic responses of MSCI.

(ii) Dynamic responses:

Since the voltage of battery is getting low as the battery is working long time, or the bad quality of battery results in the impurity of source voltage, such a voltage variation must be considered.

(a) Case I:

Assume that source voltage Vs is normally at DC 5.0V, and then it has a voltage instant drop: 5.0V→4.5V→5.0V as in Fig. 5(a). Obviously, V_O is still keeping on about 158V (Vref=160V) as shown in Fig. 5(b), even though the disturbed source Vs is lower than normal value of 5.0V.

(b) Case II:

Assume that R_L is 500Ω normally, and it changes from 500Ω to 250Ω on 60 ms. After a short period of 35ms, the load recovers from 500Ω to 250Ω, i.e. R_L = 500Ω→250Ω→500Ω as in Fig 5(c). Fig. 5(d) shows the transient waveform of V_O at the moment of loading variations. It is found that V_O has a small drop (0.1V), and the curve shape becomes thicker during the heavier load, i.e. the output ripple becomes bigger at this moment. But, Vo is still following Vref (Vref=160V), even the double loading is happening.

These results show that the closed-loop MSCI has the good output robustness to source/loading variation.

IV. CONCLUSIONS

A closed-loop scheme of a high-gain MSCI converter is proposed by using the phase generator and PWM-based gain compensator for step-up DC-DC conversion and regulation. The advantages of the proposed scheme are listed as follows. (i) By using the multiphase operation of MSCI, the large voltage conversion ratio can be achieved with 6 switches, one inductor and 3 pumping capacitors for a step-up gain of 32 or higher. (ii) For the higher step-up gain, it is easy to be realized through extending the number of stage (i.e. the number of pumping capacitor). (iii) The PWM technique is adopted here not only to enhance the output regulation capability for the different desired output, but also to reinforce the output robustness against source/loading variation. At present, the prototype circuit of this converter is being implemented in the laboratory, and then some experimental results will be measured for the verification of the proposed converter.

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ISBN: 978-988-19253-9-8
ISSN: 2078-0958 (Print); ISSN: 2078-0966 (Online)