A Closed-Loop High-Gain Switched-Capacitor-Inductor-Based Boost DC-AC Inverter

Yuen-Haw Chang and Yu-Kai Lin

***Abstract*—A closed-loop scheme of a high-gain switched-capacitor-inductor-based (SCI-based) boost DC-AC inverter is proposed by combining a phase generator and sinusoidal pulse-width-modulation (SPWM) controller for the step-up inversion and regulation. The power part is composed of two cascaded sub-circuits, including (i) a SCI booster with one inductor, and 4 pumping capacitors, and 7 switches controlled by phase generator, and (ii) a H-bridge DC-link inverter with 4 switches controlled by SPWM, so as to obtain a steady-state voltage range: $+4Vs/(1-D_0)$~ $-4Vs/(1-D_0)$ for a DC-AC conversion, where D_0 is the duty cycle of charging the inductor. The maximum output voltage can reach 12.9 times voltage of source Vs while D_0=0.69. Here, the SPWM is employed to enhance regulation capability for the different output amplitude and frequency, as well as robustness to source/loading variation. Finally, the closed-loop SCI-based inverter is designed and simulated by OrCAD SPICE for some cases: steady-state and dynamic responses. All results are illustrated to show the efficacy of the proposed scheme.**

***Index Terms*— switched-capacitor-inductor (SCI), boost DC-AC inverter, sinusoidal pulse-width-modulation (SPWM).**

I. Introduction

In recent years, due to the popularity of mobile devices, e.g. digital camera, e-book, smart phone, notebook, and pad …etc., the power modules of these products always ask for some good characteristics: small volume, light weight, higher efficiency, and better regulation capability. Generally, the traditional power converters have a large volume and a heavy weight because of magnetic elements. Therefore, more manufactures and researchers pay much attention to this topic, and ultimately, requiring DC-DC/DC-AC converters realized on a compact chip by mixed-mode VLSI technology.

The switched-capacitor (SC) power converter has received more and more attention because it has only semiconductor switches and capacitors. Thus, this kind of SC converters is one of the good solutions for low-power and high gain DC-DC/DC-AC conversion. Unlike the traditional converter, the SC converter needs no magnetic element, so they always have the small volume and light weight. The SC converter is usually designed for an output higher than supply voltage or a reverse-polarity voltage. This function fits many applications, e.g. drivers of electromagnetic luminescent (EL) lamp, white light emitting diode (WLED), op-amp, and LCD. Up to now, the various SC types have been suggested for power conversion. Now, various SC types have been suggested and the well-known topologies are described as follows. In 1976, Dickson charge pumping was proposed based on a diode-chain structure via pumping capacitors [1]. It provides voltage gain proportional to the stage number of pumping capacitor, and the detailed dynamic model and efficiency analysis were discussed [2]. But, its drawbacks include the fixed voltage gain and the larger device area. In 1990, the first SC step-down converters were proposed by Japan researchers [3], and their idea is to switch MOSFETS cyclically according to 4 periods of capacitors charging/ discharging for step-down conversion. In 1993, Ioinovici *et al.* suggested a voltage-mode SC with two symmetrical capacitor cells working complementarily [4]. In 1997, Zhu and Ioinovici performed a comprehensive steady-state analysis of SC [5]. In 2009, Tan *et al.* proposed a low-EMI SC by interleaving control [6]. In 2004, Chang proposed the design and analysis of power-CMOS-gate-based SC boost DC-AC inverter [7]. In 2007, Chang proposed a CPLD-based implementation of SC step-down DC-DC converter for multiple output choices [8]. In 2010, Hinago and Koizumi proposed a single-phase multilevel inverter using switched series/parallel DC voltage sources based on multiple independent voltage sources in order to reach the higher number of levels so as to reduce the THD value [9]. In 2011-2013, Chang *et al.* proposed a series of multistage/ multiphase SC step-up/down DC-DC/DC-AC converter/ inverter [10-13]. In this paper, the authors make a attempt on combining SC circuit with one inductor to propose a closed-loop SCI-based boost DC-AC inverter for a higher gain under a fewer element count.

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II. Configuration of SCI-Based Inverter

Fig.1 shows the configuration of the closed-loop switched-capacitor-inductor-based boost DC-AC inverter (SCI-based inverter) proposed, and and it contians two major parts: power part and control part for achieving the closed-loop high-gain step-up DC-AC conversion and regulation. The discussions are as follows.

A. Power Part

The power part of this inverter as shown in the upper half of Fig. 1 is composed of a switched-capacitor-inductor booster and a DC-link inverter cascaded in connection between

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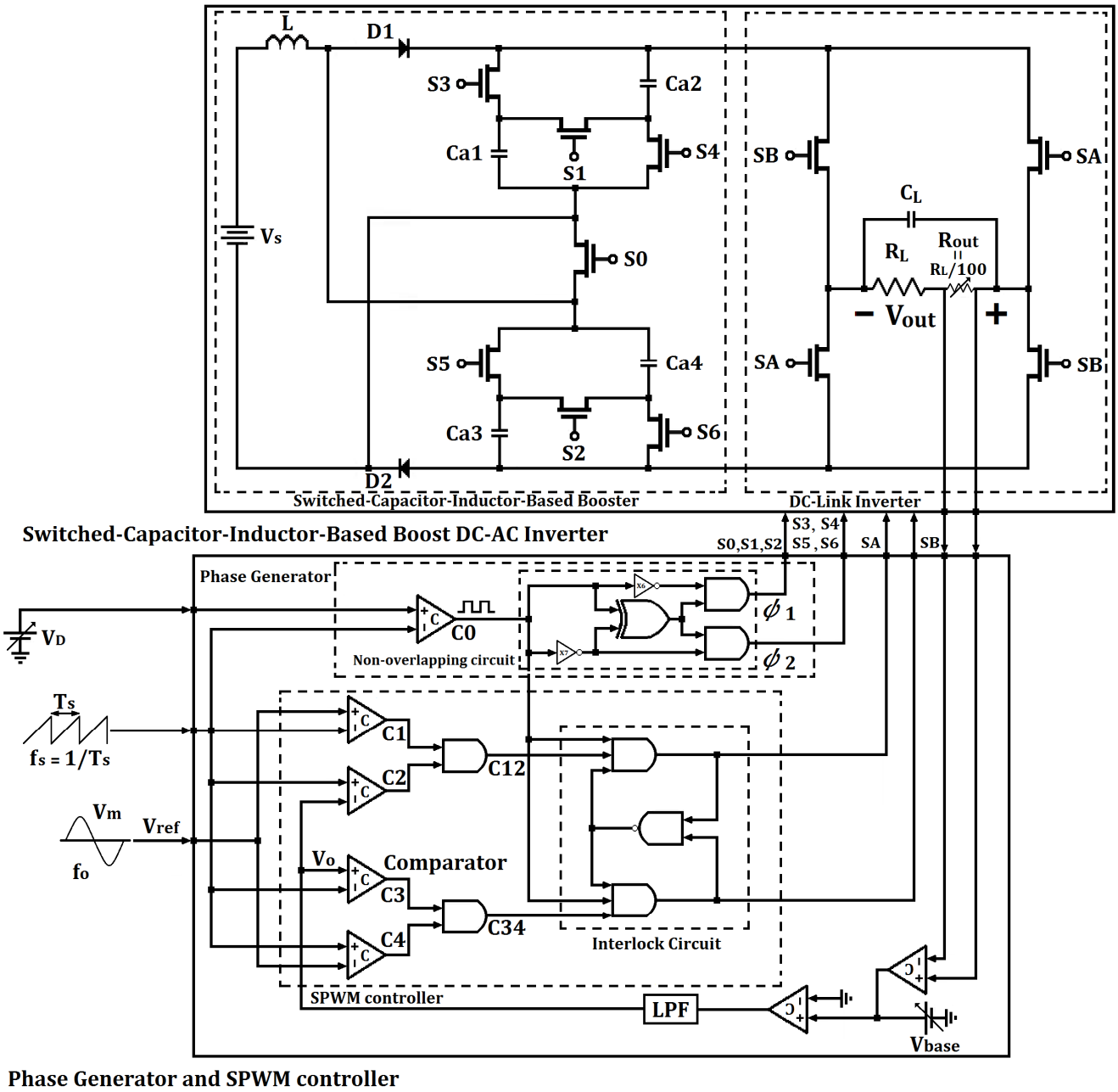

Fig. 1. Configuration of closed-loop SCI-based boost DC-AC inverter.

supply source V_S and output V_{out} for DC-AC power conversion. The SCI booster (front-stage) consists of one inductor (L), seven switches (S0-S6), four pumping capacitors (Ca1-Ca4),one output capacitor C_L and 2 diodes, where each capacitor has the same capacitance Ca (Ca1= Ca2= Ca3= Ca4= Ca). The main function of this booster is to obtain a voltage of $4Vs/(1-D_0)$ at most, where D_0 is the duty cycle of charging L. The DC-link (rear-stage) includes four switches (SA-SB), and its main function is to invert this voltage for reaching the AC output. Thus, this power part can provide the output range of $+4Vs/(1-D_0)$~ $-4Vs/(1-D_0)$ V_S for realizing DC-AC conversion. Fig. 2 shows the theoretical waveforms of these switches S0-S6, SA, SB, comparator signals C1-C4, C12, C34, and V_{out} within a output cycle T_o (T_o=1/ f_o, f_o is the frequency of desired output V_{ref}). As in Fig.2, an output cycle T_o contains 20 (or above) switching cycle T_S (T_S=1/ f_S where f_S is the switching frequency of ramp for SPWM), and each T_S has two phases: Phase I, II with the different durations D_0T_S and $(1-D_0)T_S$. The detailed operations are discussed below.

1) Phase I:

During this time interval, S0, S1, S2 turn on and S3, S4, S5, S6 turn off. Then, the diodes D_1, D_2 are off. The inductor L is charged by source V_S, and the current of L is getting for a lift just like the waveform of i_L in Fig.2.

(i) While SA is on:

The relevant topology is shown in Fig. 3(a). The capacitors Ca1-Ca4 are discharged in series connection to supply the energy to C_L and R_L (Output range: 0~$+4Vs/(1-D_0)$).

(ii) While SB is on:

The relevant topology is shown in Fig. 3(b). The

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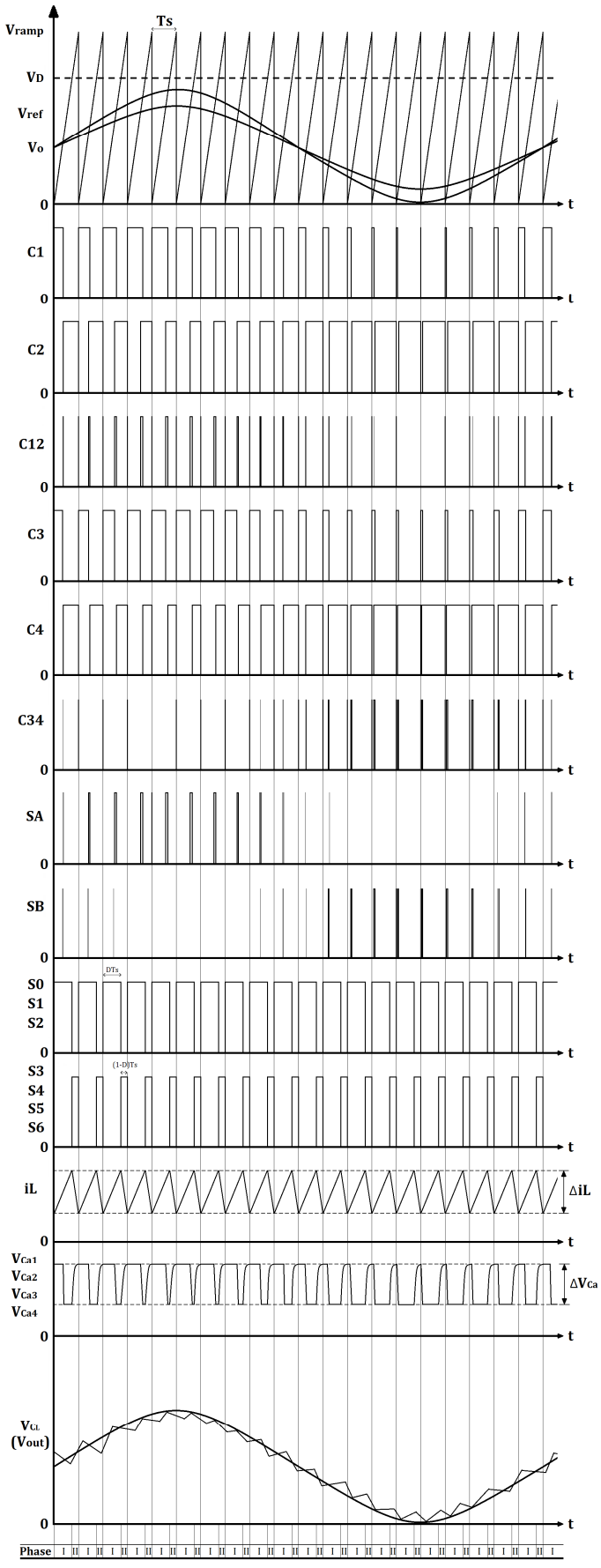

Fig. 2. Theoretical waveforms of the proposed inverter.

capacitors Ca1-Ca4 are discharged in series connection to supply the energy to C_L and R_L. (Output range: 0~-4Vs/(1-D_0))

2) Phase II:

During this time interval, S3, S4, S5, S6 turn on and S0, S1, S2, SA ,SB turn off. The relevant topology is shown in Fig. 3(c). Then, the diodes D_1, D_2 are on. The inductor L is discharged in series together with V_S to transfer the stored energy to capacitors Ca1-Ca2 and Ca3-Ca4 in parallel.

Based on the cyclical operations of Phase I and II, the overall step-up gain can reach to the value of 4/(1-D_0) theoretically. By extending capacitor count, it is reasonable that the gain can be boosted into the value of n/(1-D_0), where n is the number of pumping capacitors.

B. Control Part

The control part of SCI-based inverter is composed of a phase generator and SPWM as in the lower half of Fig. 1. The operations of these two blocks are discussed as follows.

1) Phase generator:

First, an adjustable voltage VD is compared with a ramp function to generate a non-symmetrical clock signal C0. And then, this clock is sent to the non-overlapping circuit so as to obtain a set of non-overlapping phase signals φ1, φ2 for the driver signals of S0-S2, S3-S6. Here, φ1 is the driver signal of switch S0 for charging L. Thus, D_0 is exactly the on-time ratio (duty cycle) of φ1, and D_0Ts of Phase I can be regulated by the value of VD. The main goal is to generate the driver signals of MOSFETs for the different topologies as in Fig. 3(a)-(c).

2) SPWM:

From the controller signal flow, the signal V_o is fed back into the OP-amp low-pass filter (LPF) for high-frequency noise rejection. Next, the filtered signal V_o is compared with the desired output V_{ref} via 4 comparators, and following by using logic-AND to produce a set of control signals C12, C34 for realizing SPWM. When e>0 and |e| is raising (e=V_{ref}-V_o), the pulse width of C12 is getting bigger. When e<0 and |e| is raising, the pulse width of C34 is getting bigger. And then, via the interlock circuit (avoid SA and SB being 1 simultaneously) plus coming into the phase of D_0, SA and SB can be obtained for the SPWM control, and the main goal is to keep V_o on following V_{ref} (sinusoidal reference) to enhance the regulation capability of this proposed inverter. Next, based on V_o and V_{ref}, the relevant rules of producing the control/ driver signals are summarized as below.

1) φ1,φ2: non-overlapping anti-phase signals from C0;

S0= φ1; S1=φ1; S2=φ1;

S3=φ2; S4=φ2; S5=φ2; S6=φ2;

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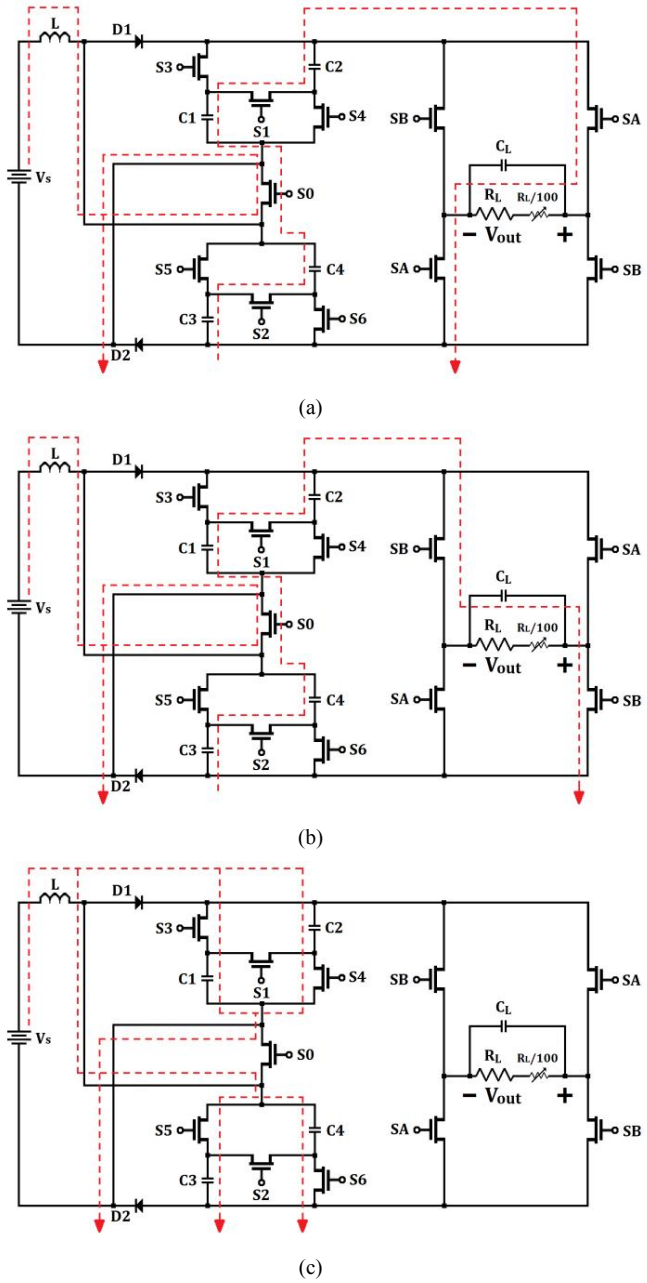

Fig. 3. Topologies of the proposed inverter for
(a) Phase I (SA:on); (b) Phase I (SB:on); (c) Phase II.

2) If V_D>V_{ramp}, then C0=1; If V_D<V_{ramp}, then C0=0.

3) If V_{ref}>V_{ramp}, then C1=1; If V_{ref}<V_{ramp}, then C1=0;

If V_{ramp}>V_o, then C2=1; If V_{ramp}<V_o, then C2=0;

If V_o>V_{ramp}, then C3=1; If V_o<V_{ramp}, then C3=0;

If V_{ref}>V_{ramp}, then C4=1; If V_{ref}<V_{ramp}, then C4=0;

4) If both C1 and C2 are 1, then C12=1 (otherwise C12=0);
If both C3 and C4 are 1, then C34=1 (otherwise C34=0);

5) SPWM control signals: (^: logic-AND)
SA= C12 ^ C0, for V_{ref}>V_o;
SB= C34 ^ C0, for V_{ref}<V_o;

III. Examples of SCI-Based Inverter

In this paper, the switched-capacitor-inductor-based boost DC-AC inverter is simulated by OrCAD, and all the parameters are listed in Table I. There are totally 3 cases discussed for steady-state responses and 3 cases for dynamic responses. Then, these results are illustrated to verify the efficacy of the proposed inverter.

1) Steady-state responses:

Case 1: f_o =60 Hz, V_m =165V, R_L =1kΩ

Let the supply source V_S be DC 12V, load R_L be 1kΩ, and the peak value and output frequency of V_{ref} are V_m =165V, f_o=60Hz. The waveform of V_{out} is obtained as in Fig. 4(a). V_{out} has the peak value of 154.62V, and the practical output frequency is about 60Hz. The efficiency is 76.2% and THD is 2.085%.

Case 2: f_o =50 Hz, V_m =165V, R_L =1kΩ

Let the supply source V_S be DC 12V, load R_L be 1kΩ, and the peak value and output frequency of V_{ref} are V_m=165V, f_o =50Hz. The waveform of V_{out} is obtained as in Fig. 4(b). V_{out} has the peak value of 154.62V, and the practical output frequency is about 50Hz. The efficiency is 76.2%, and THD is 2.043%.

Case 3: f_o =60 Hz, V_m =150V, R_L =1kΩ

Let the supply source V_S be DC 12V, load R_L be 1kΩ, and the peak value and output frequency of V_{ref} are V_m =150V, f_o =60Hz. The waveform of V_{out} is obtained as in Fig. 4(c). V_{out} has the peak value of 145.5V, and the practical output frequency is about 60Hz. The efficiency is 71.01%, and THD is 1.282%.

2) Dynamic responses:

Since the voltage of battery is getting low as the battery is working long time, or the bad quality of battery results in the impurity of source voltage, such a variation of source voltage V_S variation must be considered, as well as variation of load R_L or/and reference V_{ref} (frequency f_o or amplitude V_m).

Case 1: V_S variation

Assume that V_S is normally at DC 12V, and then it has an instant voltage jump of 12V→11V on 350ms (V_{ref}: f_o=60Hz, V_m=150V). The waveform of V_{out} is shown as in Fig. 5(a). Obviously, V_{out} has a slight decrease but it still can be working on the amplitude of about 140V (i.e. 100V(RMS)), even though V_S is lower than normal 12V.

Case 2: R_L variation

Assume that R_L is 1kΩ normally, and it suddenly changes from 1kΩ to 500Ω on 350ms (V_{ref}: f_o =60Hz, V_m =150V). Fig. 5(b) shows the transient waveform of V_{out} at the moment of loading variation. Obviously, V_{out} has a small drop but V_{out} can still be following V_{ref}.

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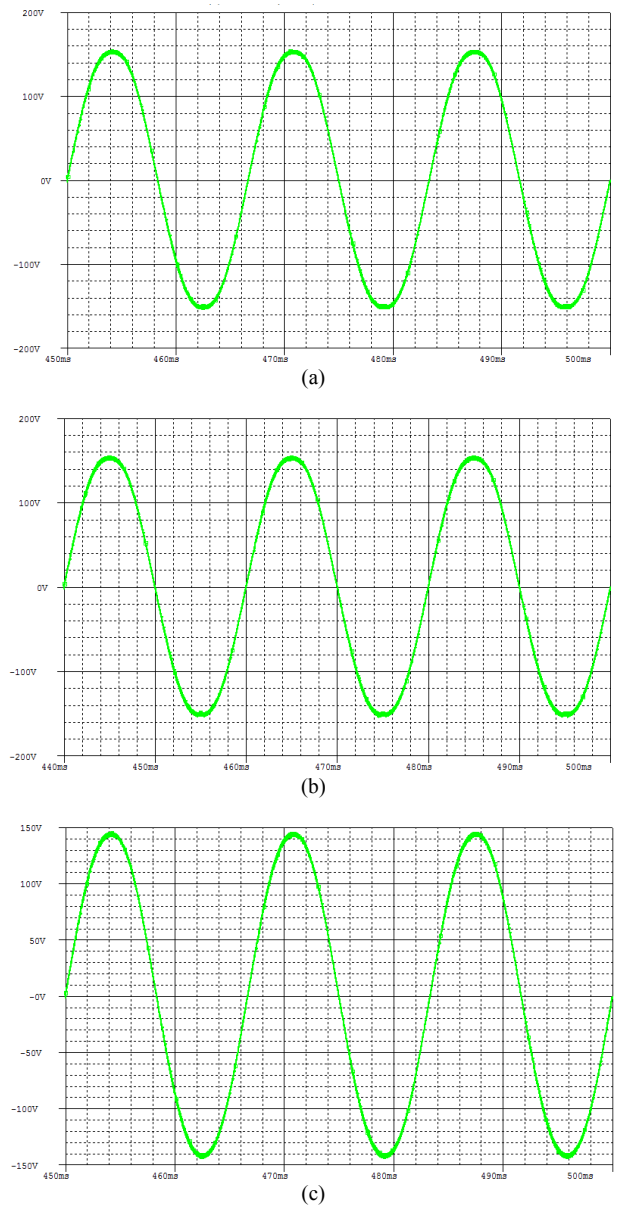

Fig. 4. Output Vout for Vref: (a) f_o =60 Hz, V_m =165V, R_L=1kΩ; (b) f_o =50 Hz, V_m =165V, R_L =1kΩ; (c) f_o =60 Hz, V_m =150V, R_L=1kΩ.

Case 3: f_o variation

Assume that the frequency f_o of Vref is 60Hz normally, and it suddenly changes from 60Hz to 20Hz. After a period of 350ms, the frequency recovers from 20Hz to 60Hz. Fig. 5(c) shows the transient waveform of V_{out} at the moment of variation: f_o =20Hz→60Hz. Obviously, V_{out} is still able to follow Vref even the frequency of V_{ref} changes.

Case 4: V_m variation

Assume that V_m is 150V normally, and it changes from 150V to 75V. After a period of 350ms, the V_m recovers from 75V to 150V. Fig. 5(d) shows the transient waveform of V_{out} at the moment of variation: V_m=75V→150V. Obviously, V_{out} is still able to follow Vref even the amplitude of the desired V_{ref} changes.

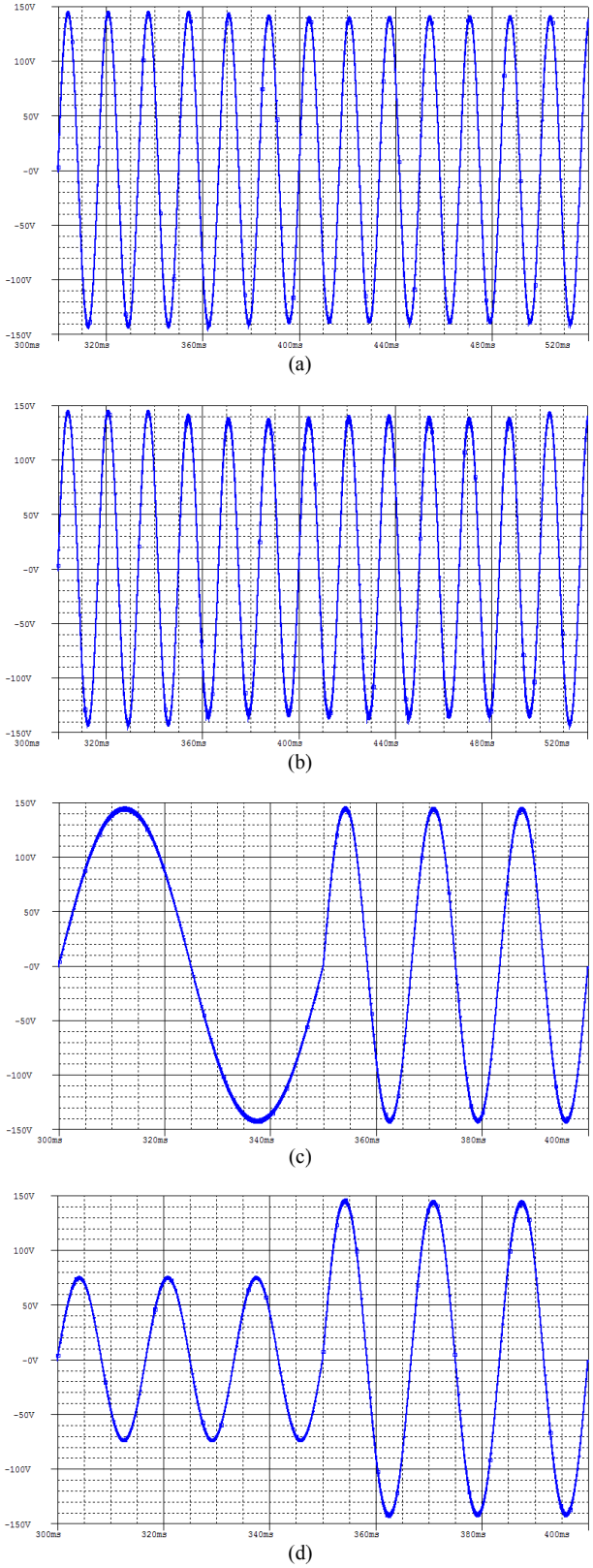

Fig. 5. Output Vout for (a) V_S variation; (b) R_L variation; (c) f_o variation; (d) V_m variation.

According to the above results, it is obvious that V_{out} is following V_{ref} for the cases, including V_S source variation, R_L loading variation, f_o frequency variation, V_m amplitude variation. These results show that this proposed inverter has a good closed-loop dynamic performance.

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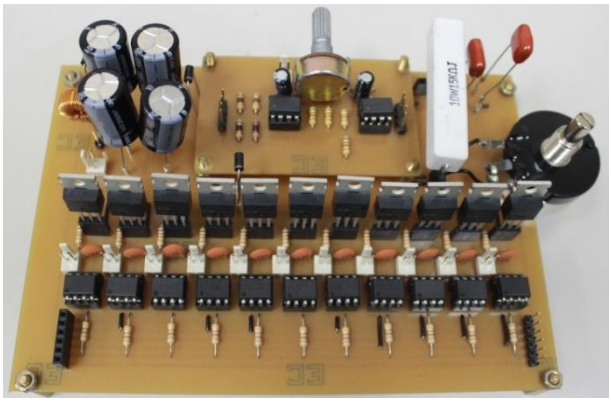
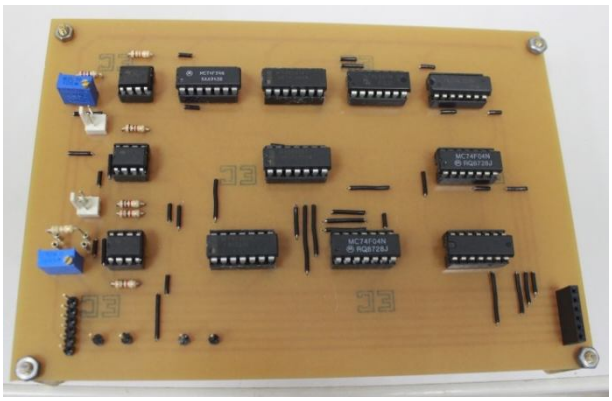
TABLE I
Circuit parameters of SCI-based inverter.

Supply source (V_S)	12V
Pumping capacitor (Ca1-Ca4)	500uF
Output capacitor (C_L)	1uF
Power MOSFETs (S0-S2)	IRF253
Power MOSFETs (S3-S6), SA, SB	ASW
On-state resistor of MOSFETs (S3-S6)	20mΩ(ASW)
On-state resistor of MOSFETs (SA, SB)	1.5Ω(ASW)
Diode (D)	D1N5822
Load resistor (R_L)	1kΩ
Switching frequency (f_S)	50kHz
Output frequency (f_o)	60Hz



(a)



(b)

Fig. 6. Prototype circuit of the proposed inverter:
(a) power part; (b) control part.

IV. Conclusion

A closed-loop high-gain SCI-based boost DC-AC inverter is proposed by combining a phase generator and SPWM controller for the step-up inversion and regulation. Finally, the closed-loop SCI-based inverter is designed and simulated by OrCAD SPICE for some cases: steady-state and dynamic responses. Besides, the further advantages of the scheme are listed as follows. (i) This SCI-based inverter needs just one magnetic element (inductor). Except this, other components (i.e. SC) will be able to be made in IC fabrication future. (ii) This proposed inverter can provide the voltage gain of $4/(1-D_0)$ at most just with 4 pumping capacitors plus one inductor. (iii) For a higher gain, it can be realized with extending the number of pumping capacitors. (iv) The SPWM technique is adopted not only to enhance output regulation capability for the different desired output, but also to reinforce the output robustness against source/loading variation. At present, the prototype circuit of this inverter is implemented in the laboratory as shown in the photo of Fig. 6. Some experimental results will be obtained and measured for the verification of the proposed inverter.

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