Generalized Impedance Function Simulator Using Voltage Differencing Buffered Amplifiers (VDBAs)

Pratya Mongkolwai and Worapong Tangsrirat, *Member, IAENG*

***Abstract*— A circuit topology for simulating grounded inductor, capacitance multiplier and frequency-dependent negative resistor (FDNR) depending on the passive component choice is presented. The presented general impedance function simulator employs two voltage differencing buffered amplifiers (VDBAs) and three various passive components. The realized equivalent impedance values can be tuned electronically via the transconductance gains of the VDBAs. The simulator does not need any component matching constraints, and also exhibits low active and passive sensitivities. To verify the theory and to exhibit the circuit performance, computer simulation results using PSPICE are provided.**

***Keywords*—Voltage Differencing Buffered Amplifier (VDBA), impedance simulator; immittance function; electronically tunable**

I. INTRODUCTION

GENERALIZE impedance function simulators such inductance simulation, capacitance multiplier of frequency-dependent negative resistor (FDNR) are essential active element blocks for the design of active network synthesis, especially for active filter and sinusoidal oscillator of cancellation parasitic elements. During the past few years, many attempts to realize general impedance function simulators have been presented [1]-[11]. However, they still suffer from the following weakness. For example, the works of [1]-[7] use three or more active devices. In [2]-[6], [8]-[11], they cannot be adjusted electronically.

Very recently, a new active element called the voltage differencing buffered amplifier (VDBA) was introduced [12]-[16]. Although many topologies for realizing impedance and immittance function simulators have been reported in the literature, little attention has been paid for implementing such type simulator topologies by employing VDBAs as active elements. In this paper, an actively generalized impedance function simulator topology using two VDBAs and three passive elements is presented. The presented simulator can simulate a grounded inductor, capacitance multiplier, and FDNR depending on the selection of passive components. All the realized impedance values can be adjusted electronically by means of transconductance gains of the VDBAs. The simulator does not require critical active and passive component matching conditions and/or cancellation constraints for its realization. Although the proposed simulator contains a floating capacitor, it can easily be realized even in recent integrated circuit technology of a decade ago with a CMOS process, which provides a second poly layer [17]. The non-ideal analysis and the sensitivity study of the proposed circuit are investigated in detail. Some simulation results are used to support the theoretical analysis.

Manuscript received August 28, 2015; revised January 18, 2016.

Pratya Mongkolwai is with the Faculty of Engineering, Rajamangala University of Technology Rattanakosin (RMUTR), Nakhon Pathom, 73170, Thailand. (e-mail: m.pratya@gmail.com).

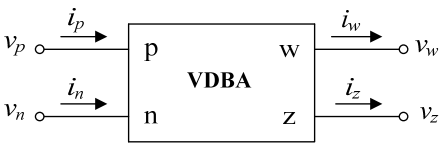
Worapong Tangsrirat is with the Faculty of Engineering, King Mongkut's Institute of Technology Ladkrabang (KMITL), Chalongkrung road, Ladkrabang, Bangkok 10520, Thailand. (e-mail: worapong.ta@kmitl.ac.th).

II. THE VDBA

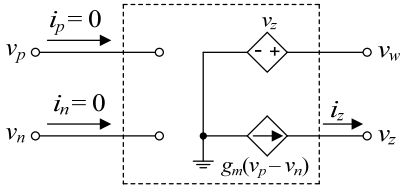
The VDBA is conceptually a cascade connection of the voltage-to-current converter (or trnasconductance amplifier) and the voltage follower. The VDBA symbol and its equivalent circuit are shown in Fig.1. Its corresponding relations can be expressed by the following equations :

$$i_p = i_n = 0, \quad i_z = g_m(v_p - v_n) \quad \text{and} \quad v_w = v_z \tag{1}$$

where g_m denotes the transconductance gain of the VDBA. respectively. According to eq.(1) and Fig.1(b), this device includes a pair of high-impedance voltage inputs (v_p and v_n), a high-impedance current output (i_z) and a low-impedance voltage output (v_w).



(a)



(b)

Fig.1 VDBA.

(a) schematic symbol (b) equivalent circuit

ISBN: 978-988-14047-6-3
ISSN: 2078-0958 (Print); ISSN: 2078-0966 (Online)

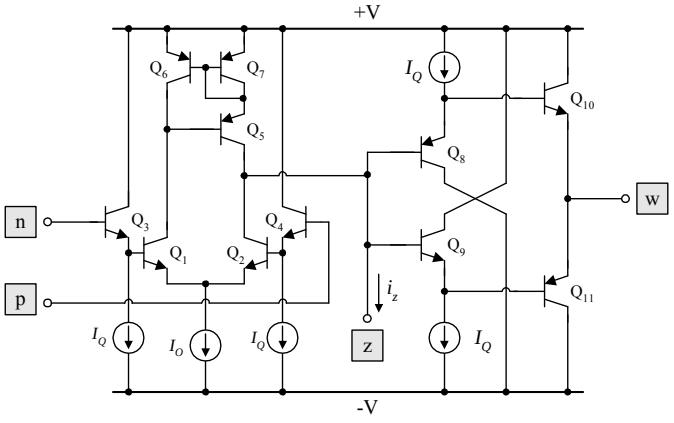


Fig.2 Bipolar implementation of the VDBA [16].

The possible bipolar implementation of the VDBA is shown in Fig.2 [16]. The circuit consists of the transconductance amplifier (Q_1-Q_7) followed by the unity-gain voltage amplifier (Q_8-Q_{71}). The transconductance gain (g_m) of the VDBA shown in Fig.2 can be written as :

$$g_m = \frac{I_O}{2V_T} \qquad (2)$$

where V_T is the thermal voltage that is equal to 26 mV at 27°C

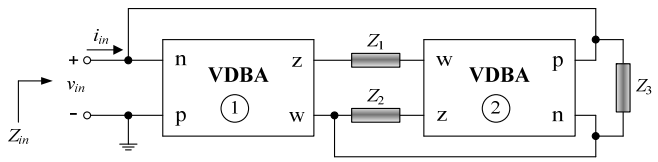


Fig.3 Proposed general impedance simulator.

III. Proposed Configuration

The proposed configuration for simulating general impedance functions is shown in Fig.3. It is realized by using VDBAs as active components. Straightforward analysis of the proposed configuration in Fig.3 gives the following input impedance :

$$Z_{in} = \frac{v_{in}}{i_{in}} = \left(\frac{g_{m2}}{g_{m1}}\right)\left(\frac{Z_2 Z_3}{Z_1}\right) \qquad (3)$$

where g_{mi} represents the gain parameter g_m of the i-th VDBA (i = 1, 2). From eq.(3), it is essential to note that the magnitude of the impedance Z_{in} can be tuned electronically through the transconductance ratio g_{m2}/g_{m1}. Also note from eq.(3) that by appropriately selecting the choice of the passive impedance (Z_1, Z_2 and Z_3), the proposed circuit in Fig.3 can simulate a grounded inductor, capacitance multiplier and FDNR as in the following details :

(1) If $Z_1 = 1/sC_1$, $Z_2 = R_2$ and $Z_3 = R_3$ are selected, a grounded inductance simulator can be realized as :

$$Z_{in} = sL_{eq} = s\left(\frac{g_{m2}R_2R_3C_1}{g_{m1}}\right) \qquad (4)$$

where the realized equivalent inductance is equal to

$$L_{eq} = \frac{g_{m2}R_2R_3C_1}{g_{m1}} \qquad (5)$$

(2) If $Z_1 = R_1$, $Z_2 = 1/sC_2$ and $Z_3 = R_3$ are choosing, the input impedance from eq.(3) becomes :

$$Z_{in} = \frac{1}{sC_{eq}} = \frac{1}{s\left(\frac{g_{m1}R_1C_2}{g_{m2}R_3}\right)} \qquad (6)$$

which performs a grounded capacitance multiplier whose the realized equivalent capacitance is given by :

$$C_{eq} = \frac{g_{m1}R_1C_2}{g_{m2}R_3} \qquad (7)$$

(3) Finally, by taking $Z_1 = R_1$, $Z_2 = 1/sC_2$ and $Z_3 = R_3$, an electronically tunable FDNR is implemented with the following input impedance :

$$Z_{in} = \frac{1}{s^2D_{eq}} = \frac{1}{s^2\left(\frac{g_{m1}R_1C_2C_3}{g_{m2}}\right)} \quad . \qquad (8)$$

In eq.(8), the D_{eq}–element value is obtained as :

$$D_{eq} = \frac{g_{m1}R_1C_2C_3}{g_{m2}} \qquad (9)$$

IV. Non-Ideal Case

In case of the non-ideal characteristic condition, the VDBA terminal relations from eq.(1) can be rewritten as :

$$i_z = \alpha g_m(v_p - v_n) \quad \text{and} \quad v_w = \beta v_z \qquad (10)$$

where $\alpha = 1 - \varepsilon_g$, and $|\varepsilon_g| << 1$ denotes the transconductance error, and $\beta = 1 - \varepsilon_v$, and $|\varepsilon_v| << 1$ denotes the voltage tracking error of the VDBA, respectively. Taking into account the VDBA non-ideality, an input impedance of the configuration in Fig.3 can be modified as :

ISBN: 978-988-14047-6-3
ISSN: 2078-0958 (Print); ISSN: 2078-0966 (Online)

$$Z_{in} = \left(\frac{\alpha_2 \beta_2 g_{m2}}{\alpha_1 g_{m1}} \right) \left(\frac{Z_2 Z_3}{Z_1} \right) \quad (11)$$

where α_i and β_i are the parasitic gains α and β of the i-th VDBA.

Normalized active and passive sensitivities of Z_{in} are calculates as :

$$S^{Z_{in}}_{\alpha_1, g_{m1}} = -S^{Z_{in}}_{\alpha_2, \beta_2, g_{m2}} = -1 \quad (12)$$

and

$$S^{Z_{in}}_{Z_1} = -S^{Z_{in}}_{Z_2, Z_3} = -1 \quad (13)$$

which are less than unity in magnitude. Therefore, the proposed simulator of Fig.3 exhibits low active and passive sensitivities.

V. Performance Verification by Simulations

To confirm the results of the theoretical analysis discussed above, the proposed general impedance function simulator of Fig.3 has been simulated with PSPICE program. For this purpose, the VDBA given in Fig.2 has been used. The PNP and NPN transistors in VDBA implementation were simulated using the typical parameters of bipolar transistor model PR100N (PNP) and NP100N (NPN). The DC supply voltages and bias currents were respectively selected as : +V = -V = 1.5V and I_Q = 50 μA.

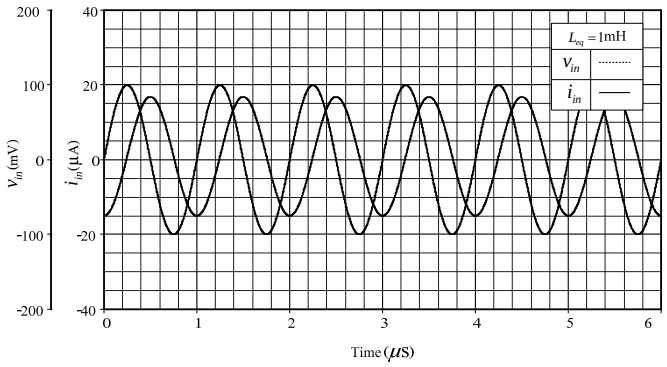
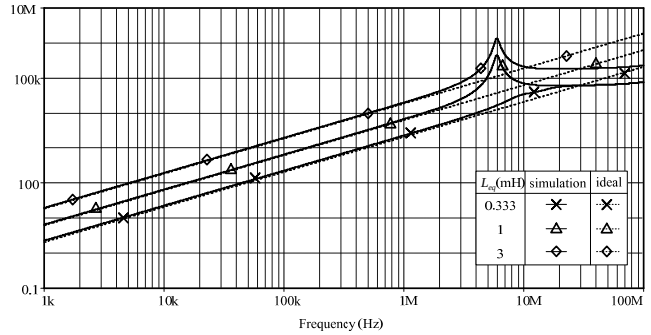
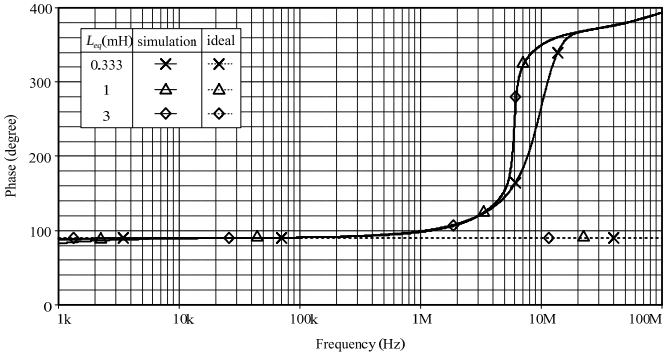


Fig.4 Time–domain responses for v_{in} and i_{in} of the proposed inductance simulator in Fig.3.



(a)



(b)

Fig.5 Ideal and simulated frequency responses of the impedance of the proposed inductance simulator in Fig.3.
(a) magnitude responses (b) phase responses

In case of the inductance simulator, the circuit of Fig.3 was realized by taking the following active and passive components : $g_{m1} = g_{m2} \cong 1.92$ mA/V ($I_{B1} = I_{B2} = 100$ μA), C_1 = 1 nF and $R_2 = R_3$ = 1 kΩ. With these component values, the value of the realized equivalent inductance is L_{eq} = 1 mH. Fig.4 shows the simulated transient responses of the input voltage (v_{in}) and input current (i_{in}) through the proposed inductor circuit of Fig.3 at the operating frequency f = 10 kHz. The simulation results indicate that v_{in} leads i_{in} by 90°, as expected. To further demonstrate the electronic tuning performance of the simulator, the transconductance parameters are adjusted as : g_{m1} = 5.77 mA/V, 1.92 mA/V and 1.92 mA/V, and g_{m2} = 1.92 mA/V, 1.92 mA/V and 5.77 mA/V, which results in L_{eq} = 0.333 mH, 1 mH and 3 mH, respectively. Fig.5 shows the ideal and simulated magnitude and phase responses of the input impedance of the grounded inductor in Fig.3. It appears, therefore, that the useful frequency range for the proposed inductance simulator is about 1 kHz to 2 MHz.

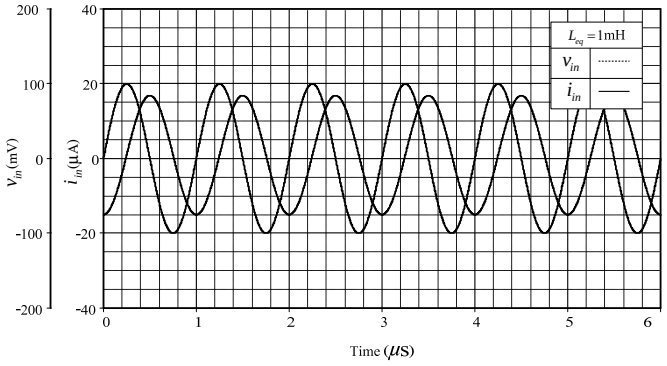
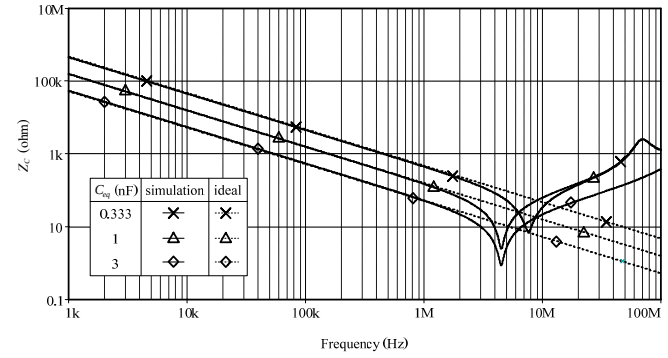


Fig.6 Time–domain responses for v_{in} and i_{in} of the proposed capacitance simulator in Fig.3.

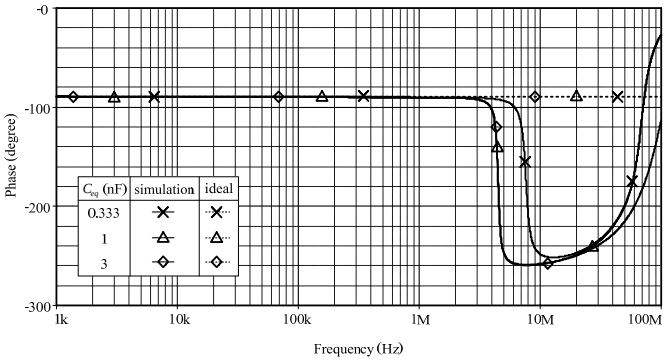
For the proposed capacitance simulator, the following active and passive components : : $g_{m1} = g_{m2}$ = 1.92 mA/V ($I_{B1} = I_{B2}$ = 100 μA), R_1 = 1 kΩ, C_2 = 1 nF, and R_3 = 1 kΩ are chosen, resulting in C_{eq} = 1 nF. Typical waveforms of v_{in} and i_{in} through the proposed capacitor circuit when a sinusoidal input voltage with 100 mV (peak) at f = 10 kHz was applied to the circuit are shown in of Fig.6. From the results, the

ISBN: 978-988-14047-6-3
ISSN: 2078-0958 (Print); ISSN: 2078-0966 (Online)

phase difference between v_{in} and i_{in} is approximately 90°. Furthermore, the impedance of the proposed floating capacitance simulator circuit in Fig.3 relative to frequency is shown in Fig.7. The VDBA's transconductances were varied as : g_{m1} = 1.92 mA/V, 1.92 mA/V and 5.77 mA/V, and g_{m2} = 5.77 mA/V, 1.92 mA/V and 1.92 mA/V, to obtain C_{eq} = 0.333 nF, 1 mH and 3 nF, respectively. Also note that the simulation results exhibited in Figs.6 and 7 are in close agreement with the calculated results.



(a)



(b)

Fig.7 Ideal and simulated frequency responses of the impedance of the proposed capacitance simulator in Fig.3.

(a) magnitude responses (b) phase responses

VI. Conclusions

In conclusions, this study describes an alternative topology for realizing an electronically controllable general impedance simulator topology, containing two VDBAs and three passive components. The simulator can realize grounded inductor, capacitance multiplier and FDNR by properly selecting the choice of the passive components. All of the realized impedance values are controllable electronically through the transconductance gains of the VDBAs.

Acknowledgment

This research work is supported by Faculty of Engineering, Rajamangala University of Technology Rattanakosin (RMUTR), Thailand.

References

[1] K. Pal, "Floating inductance and FDNR using positive polarity current conveyors", *Active and Passive Electronic Components*, vol.27, no.2, pp.81-83, 2004.

[2] E. Yuce, O. Cicekoglu, S. Minaei, "Novel floating inductance and FDNR simulator employing CCII+s", *J. Circuits, Syst., Comp.*, vol.15, no.1, pp.75-81, 2006.

[3] C. Psychalinos, K. Pal, S. Vlassis, "A floating generalized impedance converters with current feedback operational amplifiers, *Int. J. Electron. Commun. (AEU)*, vol.62, no.2, pp.81-85, 2008.

[4] B. Metin, S. Minaei, "Parasitic compensation in CCI-based circuits for reduced power consumption", *Analog Integr. Circ. Signal Process.*, vol.65, no.1, pp.157-162, 2010.

[5] R. A. Saad, A. M. Soliman, "On the systematic synthesis of CCII-based floating simulators", *Int. J. Circ. Theory Appl.*, vol.38, no.9, pp.935-967, 2010.

[6] A. M. Soliman, "Generation of generalized impedance converter circuits using NAM expansion", *Circuits Syst. Signal Process.*, vol.30, pp.1091-1114, 2011.

[7] A. Uygur, H. Kuntman, "Seventh-order elliptic video filter with 0.1 dB pass band ripple employing CMOS CDTAs", *Int. J. Electron. Commun. (AEU)*, vol.61, pp.320-328, 2007.

[8] A. Lahiri, "DO-CCII based generalized impedance converter simulates floating inductance, capacitance multipliers ans FDNR", *Australian J. Electrical Electron. Eng.*, vol.7, no.1, pp.15-20, 2010.

[9] E. Yuce, "On the impelementation of the floating simulators employing a single active device", *Int. J. Electron. Commun. (AEU)*, vol.61, no.7, pp.453-458, 2007.

[10] B. Metin, O. Cicekoglu, "A novel floating lossy inductance realization topology with NICs using current conveyors", *IEEE Trans. Circuits, Syst. II*, vol.56, pp.483-486, 2006.

[11] B. Metin, "Supplementary inductance simulator topologies employing single DXCCII", *Radioengineering*, vol.20, no.3, pp.614-618, 2011.

[12] F. Kacar, A. Yesil, A. Noori, "New CMOS realization of voltage differencing buffered amplifier and its biquad filter applications", *Radioengineering*, vol.21, no.1 , pp.333-339, 2012.

[13] R. Sotner, J. Jerabek, N. Herencsar, "Voltage differencing buffered/inverted amplifiers and their applications for signal generation", *Radioengineering*, vol.22, no.2, pp.490-504, 2013.

[14] N. Herencsar, S. Minaei, J. Koton, E. Yuce, K. Vrba, "New resistorless and electronically tunable realization of dual-output VM all-pass filter using VDIBA", *Analog Integr. Circ. Signal Process.*, vol.74, no.1, pp.141-154, 2013.

[15] K. L. Pushkar, D. R. Bhaskar, D. Prasad, "Voltage-mode new universal biquad filter configuration using a single VDIBA", *Circuits Syst. Signal Process.*, vol33, no.1, pp.275-285, 2014.

[16] W. Tangsrirat, O. Onjan, T. Pukkalanun, "SFG synthesis of general nth-order allpole voltage transfer functions using VDBAs and grounded capacitors", *Proc. JICTEE-2014*, Chiang Rai, Thailand, 5-8 March, pp.291-294, 2014.

[17] R. J. Baker, H. W. Li, D. E. Boyce, *CMOS Circuit Design, Layout and Simulation*, Chapter 7, IEEE Press, New York, 1998.