Hetero Gate Material and Dual Oxide Dopingless Tunnel FET

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***Abstract*— In this work, we propose a novel structure of dopingless tunnel field effect transistor (DL-TFET), employing hetero gate material and dual oxide. The two dimensional (2D) simulation studies have shown a significant improvement in the proposed device in comparison to conventional doping-less Tunnel FET (DL-TFET). It has been observed that the I_{ON} and I_{ON}/I_{OFF} of the proposed device have increased by ~65 times and ~74 times respectively in comparison to the conventional DL-TFET. Further, an improvement of ~38% in average subthreshold slope (SS_{avg}) is achieved in the proposed device in comparison to the conventional DL-TFET. The ac analysis has revealed that the cutoff frequency (f_T) of proposed device (103GHz) has increased by ~13 times in comparison to conventional DL-TFET (8GHz). Further, since the proposed device is doping less and is a charge plasma based structure, therefore, it is free from doping related issues and can be processed at low temperature.**

***Index Terms*— Band-to-band tunnelling (BTBT), Charge plasma, doping-less, hetero gate, TFET**

I. Introduction

THE driving force for the device performance enhancement in the last many decades has been the scaling of device dimensions. The scaling is a big factor in keeping Moore's law valid even today also. It has resulted in significantly improving the switching speed, packing density, functionality and cost of integrated circuits. However, scaling MOSFET dimensions below 32 nm technology node is very difficult due various short channel effects (SCE) [1, 4]. Due to these undesired effects, nano scaled devices face challenges like, high power consumption, difficulty in further scaling of supply voltage (V_{DD}) and increase in leakage current [3]. The reduction in V_{DD} needs the reduction in threshold voltage (V_t) of the device also, to maintain over drive factor high. This results in a significant increase in the leakage current, because subthreshold slope (*SS*) is not scalable in MOSFET. Reducing *SS* is a potential way to maintain the performance and can be done by changing the switching mechanism from thermionic emission to tunneling [4]. Various steep subthreshold slope devices have been reported in the literature [5, 6]. Among these devices Tunnel FET (TFET) shows the potential for low voltage operation. However there are various problems associated with TFET, like poor on current [9], ambipolar nature [7, 8] random doping fluctuations (RDF) [12] and requirement of abrupt junction.

In this work, we propose a new doping-less device which significantly addresses the above mentioned problems. The proposed device is a dopingless device, in which the source and drain regions are created by charge plasma concept [7, 13, 14,]. The charge plasma concept will eradicate the problems of RDF and abrupt junctions [15, 16, and 17]. In addition requirement for high temperature processing and ion implantation will be completely eliminated. Further, the proposed device is a double gate structure and employs dual gate oxide and dual gate material. The top gate consists of two gate oxides (HfO_2 and SiO_2) and two gate metals (with work-function 3.9eV and 4.5eV). Similar materials have been used for bottom gate also. The proposed device has been named as Hetero gate dual oxide doping-less tunnel FET (HG-DL-TFET). The simulation study has revealed that the proposed HG-DL-TFET outperforms the conventional doping-less in all respects. Both these devices have been compared using Atlas device simulator [10]. The comparative analyses show significant improvement in I_{ON} by 64 times, I_{ON}/I_{OFF} by 74 times and SS_{avg} by 38% for the proposed device in comparison to the conventional DL-TFET. Further, ac analysis has revealed that the f_T in the proposed HG-DL-TFET (103GHz) has increased by 13 times in comparison to conventional DL-TFET (≈8GHz) device.

This paper is divided into four sections. Section II discusses various device structures and parameters. The simulation results and discussion have been discussed in section III. The conclusion is given in section IV.

II. DEVICE SCHEMATICS AND PARAMETERS

The schematics of the conventional DL-TFET and the proposed HG-DL-TFET devices are shown in Figure 1. For the accurate comparative analysis same device parameters have been used in the proposed HG-DL-TFET device as has been used in DL-TFET [16]. The silicon film thickness (T_{si}) used is 10 nm. It has to be kept less than the Debye length (L_D), in order to keep induced carrier distribution uniform. The oxide thickness is different in different regions. Under source and drain electrodes, the oxide thickness is T_{ox1} = 0.4nm and T_{ox2}= 3nm respectively. In both these devices P^+ source and N^+ drain are created by charge plasma concept [13, 14]. For creating P^+ source and N^+ drain, metals with work-function 5.93eV and 3.9eV have been used respectively. The top and bottom gates are both dual metal gates and employ two metals with work functions 3.9eV and

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4.5eV. The gate with work function 3.9eV is acting as a tunneling gate, as shown in Figure 1.

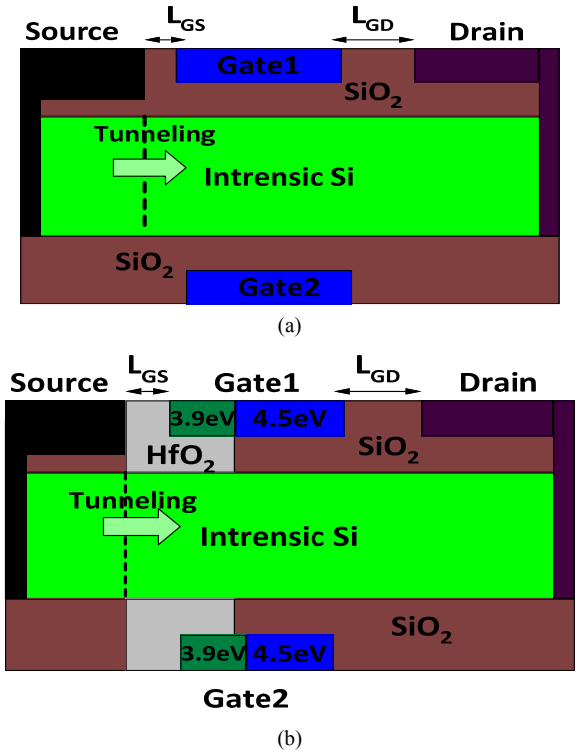

Fig. 1: Schematics of (a) conventional DL-TFET (b) proposed HG-DL-TFET

III. RESULTS AND DISCUSSION

The electron concentration variations along a horizontal cutline 1nm below the Si–SiO_2 interface in the proposed HG-DL-TFET in the OFF-state and ON-state conditions are shown in Figure 2. The same carrier concentration has been observed in conventional DL-TFET except electron concentration peak observed in HG-DL-TFET below low metal work-function gate as seen in Figure 2.

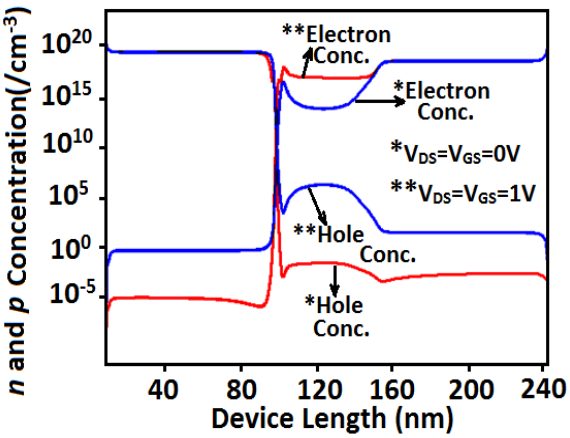

Fig. 2: Total carrier concentration in the proposed HG-DL-TFET device for different bias conditions

The energy band diagram of the conventional DL-TFET and proposed HG-DL-TFET are shown in Figure 3. Figure 3 shows a perfect alignment of valance and conduction bands in the ON state in both the devices.

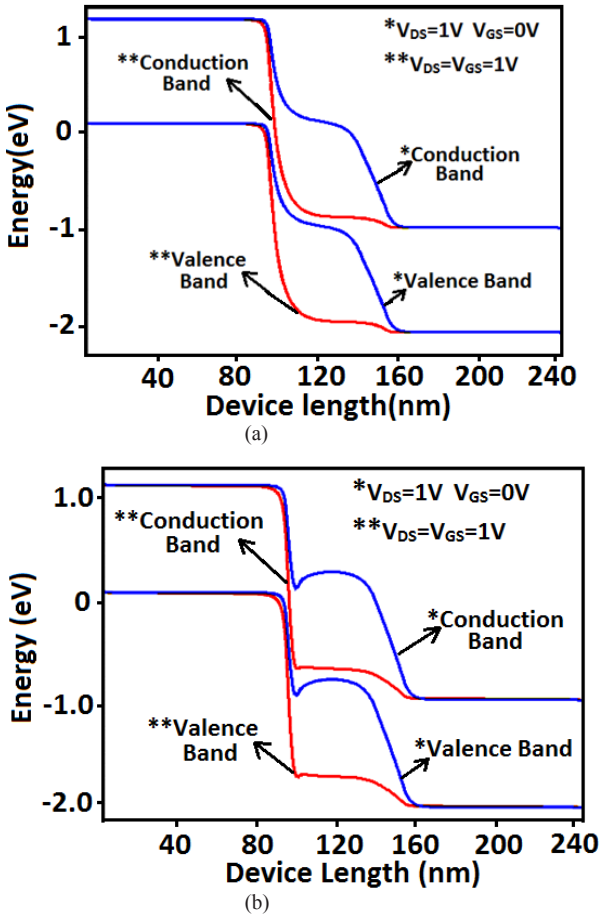

Fig. 3: Band diagrams of (a) conventional DL-TFET (b) the proposed HG-DL-TFET in the OFF-state (V_{GS} = 0V, V_{DS} = 1.0 V) and in ON-state (V_{GS} = V_{DS} = 1.0 V) conditions.

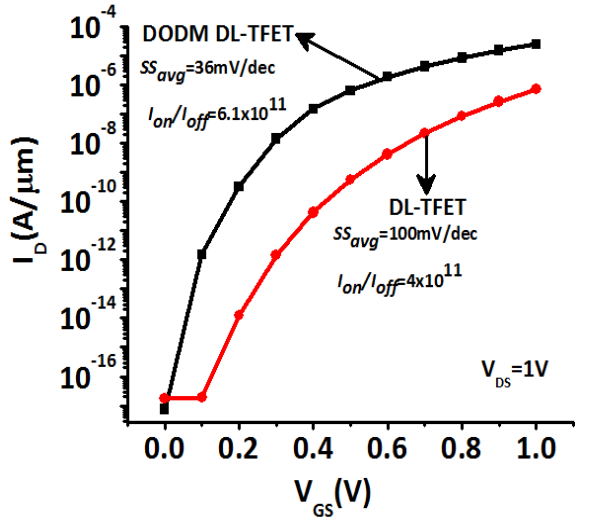

Fig. 4: Transfer characteristics of conventional DL-TFET and the proposed HG-DL-TFET devices.

It is clear from Figure 3 that the tunneling width in case of the proposed HG-DL-TFET has got reduced in comparison to the conventional DL-TFET device. The transfer characteristics of conventional DL-TFET and the proposed HG-DL-TFET devices are shown in Figure 4. These characteristics are obtained under equal threshold voltage condition corresponding to a current of 10^{-7} A/ μm for both the devices. It is clear from Figure 4 that the proposed device outperforms the conventional DL-TFET in many

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ways. It has been observed ON current and ON/OFF ratio has been increased by ~65 times and ~74 respectively. In addition to this SS_{avg} , which is very important for switching has got significant improvement of ~38% in the proposed HG-DL-TFET (37mV/dec) in comparison to conventional DL-TFET (90mV/dec). This improved performance in proposed HG-DL-TFET device can be attributed to high k gate dielectric (HfO_2) and low metal work-function used at the top of the tunnel junction. The combined effect of high k dielectric and low metal work-function results in high electric field at the tunneling junction, which in turn decreases tunneling width, as can be seen from Figure 3b. This decrease in tunneling width results in improved performance in HG-DL-TFET. Figure 5 shows that the f_T of the proposed HG-DL-TFET (103GHZ) has increased by ~13 times in comparison to (~7.77GHZ) devices. This increase in f_T is due to increase in the transconductance in the proposed device due effective modulation of tunneling width.

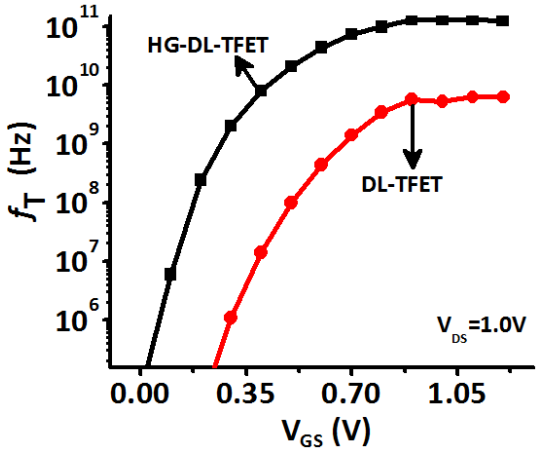

Fig. 5. Cutoff frequency (f_T) comparison of the proposed GEDL-TFET, DL-TFET and D-TFET devices

IV. CONCLUSION

A simulation study of novel HG-DL-TFET doping-less tunnel FET has been presented. The proposed device is double gate and using charge plasma concept for the creation of source and drain regions. The top as well as bottom gate consists of dual oxide and dual metal. Because two different gate oxides and gate metals have been used, the device has been named Hetero gate doping-less TFET. The use of low metal work-function and HfO_2 on the top of tunnelling junction results in improved performance. The proposed device has been compared with the conventional DL-TFET, a significant improvement has been achieved in all the parameters. The advantage of having steep subthreshold slope in the proposed device will result in scaling of V_{DD} without any performance loss**.** In addition to this, the proposed device will retain all the advantages of conventional device, like free from RDF, no need of high abrupt junctions and doesn't require high temperature annealing processes in its actual fabrication.

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