A High-Gain Switched-Coupled-Inductor Switched-Capacitor Step-Up DC-DC Converter

Yuen-Haw Chang and Jia-Syun Lin

Abstract—A closed-loop high-gain switched-coupled-inductor switched-capacitor (SCISC) converter is proposed by combining a sawtooth wave generator, pulse-width-modulation-based (PWM-based) compensator and non-overlapping circuit for step-up DC-DC conversion and regulation. The power part between source V_S and output V_O contains two sub-circuits: (i) a switched-coupled-inductor (SCI) booster circuit, and (ii) a three-stage switched-capacitor (SC) tripler circuit. With the help of a clamping capacitor and a coupled-inductor with the turn ratio n, this SCI booster can provide the voltage of $(2+n-D)/(1-D)V_S$ theoretically, where D means the duty cycle of the MOSFET. And then by using the SC tripler, the overall step-up gain can reach to $3(2+n-D)/(1-D)$ at most. Practically, this SCISC can boost the voltage gain up to 37 when D=0.6, n=4. Further, the PWM technique is adopted not only to enhance the output regulation for the compensation of the dynamic error between the practical and desired outputs, but also to reinforce output robustness against source or loading variation. Finally, the closed-loop SCISC is designed by OrCAD SPICE and simulated for some cases: steady-state and dynamic responses. All results are illustrated to show the efficacy of the proposed scheme.

***Index Terms*—high-gain, switched-coupled-inductor, switched-capacitor, pulse-width-modulation, step-up converter.**

I. Introduction

Recently, with the rapid development of power electronics, the step-up DC-DC converters are emphasized more widely for the electricity-supply applications, such as photovoltaic system, fuel cell, X-ray systems. General speaking, these power electronics converters are always required for a small volume, a light weight, a high efficacy, and a better regulation capability.

The switched-capacitor converter (SCC), possessed of the charge pump structure, is one of solutions to DC-DC power conversion because it has only semiconductor switches and capacitors. Unlike traditional converters, the inductor-less SCC has light weight and small volume. Up to now, many types have been suggested [1], [2], and some well-known topologies are presented, e.g. Dickson charge pump, Ioinovici SC. In 1976, Dickson charge pump was proposed with a two-phase diode-capacitor chain [3], [4], but it has the drawbacks of fixed gain and large device area. In the 1990s, Ioinovici proposed a SCC with two symmetrical capacitor cells, and presented a current-mode SCC [5], [6]. In 1997, Zhu and Ioinovici performed a comprehensive steady-state analysis of SCC [7]. In 1998, Mak and Ioinovici suggested a high-power-density SC inverter [8]. In 2004, Chang presented a current-mode SC inverter [9]. In 2009, Tan *et al.* proposed the modeling and design of SCC by variable structure control [10]. In 2011, Chang proposed an integrated step-up/down SCC (SCVM/SCVD) [11]. In 2013, Chang proposed a gain/efficiency-improved serial-parallel switched-capacitor converter (SPSCC) by combining an adaptive-conversion-ratio (ACR) and pulse-width-modulation (PWM) control [12]. In 2014, Chang proposed a high-gain switched-inductor switched-capacitor step-up DC-DC converter (SISCC) is proposed by phase generator and PWM control [13]. In 2015, Wu proposed a non-isolated high step-up DC-DC converter adopting switched-capacitor cell [14].

For a higher voltage gain, it is one of the good ways to utilize the device of coupled-inductor. Nevertheless, the stress on transistors and the volume of magnetic device might be considered. In 2011, Berkovich *et al.* proposed a switched-coupled inductor cell for DC-DC converter with very large conversion ratio [15]. In 2015, Chen *et al.* proposed a novel switched-coupled- inductor DC-DC step-up converter via adopting a coupled inductor to charge a switched capacitor for making voltage gain effectively increased. Not only lower conduction losses but also higher power conversion efficiency is benefited from a lower part count and lower turn ratio [16].

Based on the above descriptions, for achieving a compromise among volume size, component count, and voltage gain, the closed-loop SCISC is proposed here by combining the ideas of [11], [13], [14], [16] to realize a high-gain conversion as well as enhance the regulation capability.

II. Configuration of SCISC

Fig. 1 shows the overall circuit configuration of SCISC step-up converter, and it contians two major parts: power part and control part for achieving the high-gain step-up DC-DC conversion and closed-loop regulation. Fig. 2 shows the detailed circuit of the control part.

A. Power part

The power part of SCISC is shown in the upper half of Fig. 1 and it consists of two subcircuits: a switched-coupled-inductor booster and a three-stage SC doubler, connected in cascade between source *Vs* and output *Vo*. This converter contains one coupled-inductor (L_1, L_2) with the turn ratio $n=N_2/N_1$, four power switches (S_1-S_4), one clamping capacitor (C_1), three pumping capacitors (C_2-C_4), one output capacitor C_o and 8 diodes (D_1-D_8), where each

Manuscript received December 5, 2015. This work is supported in part by Ministry of Science and Technology of Taiwan, R.O.C., under Grant MOST 104-2221-E-324-015.

Yuen-Haw Chang and Jia-Syun Lin are with the Department and Graduate Institute of Computer Science and Information Engineering, Chaoyang University of Technology, Taichung, Taiwan, R.O.C. Post code: 413. (e-mail: cyhfyc@cyut.edu.tw, s10327610@gm.cyut.edu.tw).

ISBN: 978-988-14047-6-3
ISSN: 2078-0958 (Print); ISSN: 2078-0966 (Online)

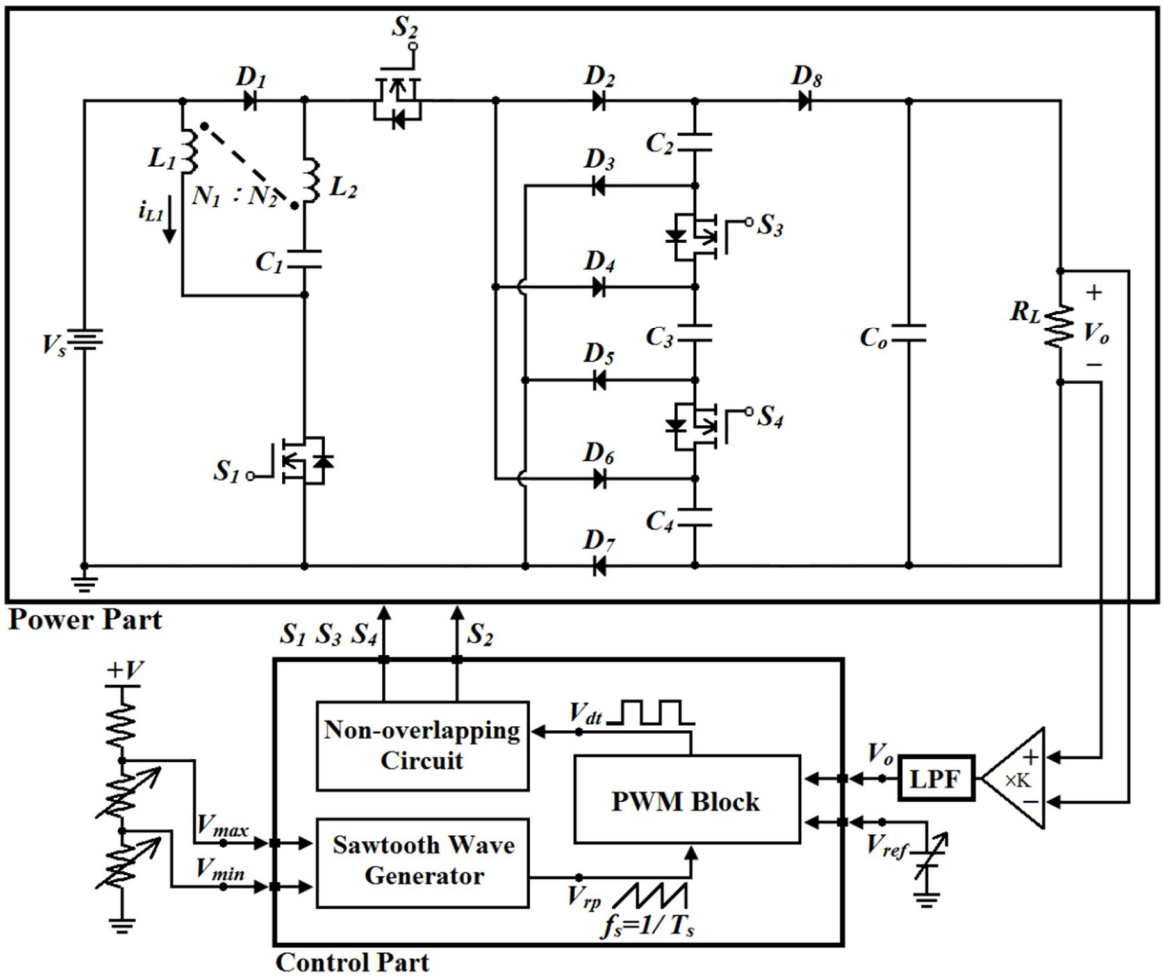

Fig. 1. Closed-loop configuration of SCISC.

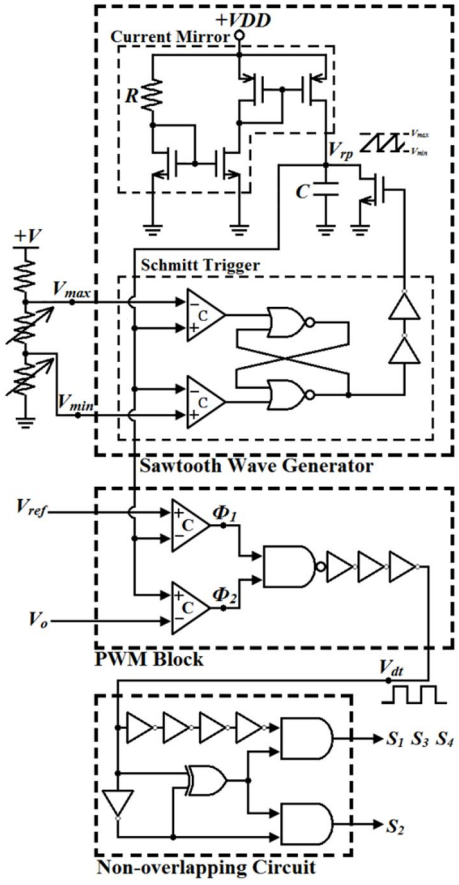

Fig. 2. Detailed circuit of control part.

capacitor of SC doubler has the same capacitance C (C_2=C_3=C_4=C). Fig. 3 shows the theoretical waveforms of SCISC in a switching cycle T_S (T_S=1/f_S, f_S: switch frequency). Each T_S contains two phases: Phase I and II. The operations for Phase I and II are described as follows.

(i) Phase I:

While V_{dt}=1 (PWM ON), turn on S_1, S_3, S_4, and turn off S_2. Then, the diodes D_1, D_8 are turned on, and D_2-D_7 are off. The current-flow path is shown as "---" in Fig. 4(a). The inductors L_1, L_2 and capacitor C_1 are charged in parallel by the source V_s. At the same time, C_2-C_4 are discharged in series to transfer the energy to output capacitor C_o and load R_L.

(ii) Phase II:

While V_{dt}=0 (PWM OFF), turn off S_1, S_3, S_4, and turn on S_2. Then, the diodes D_2-D_7 are turned on, and D_1, D_8 are off. The current-flow path is shown as "---" in Fig. 4(b). The capacitors C_2-C_4 are charged in parallel by the series voltages of inductors L_1, L_2 and capacitor C_1. Simultaneously, output capacitor C_o just stands alone to supply load R_L.

Based on the scheduled operations of Phase I and II cyclically, the overall step-up gain can reach the value of 3(2+n-D)/(1-D) theoretically. Extending the capacitor count, the gain can reach up to the value of m(2+n-D)/(1-D) where m is the number of pumping capacitors.

ISBN: 978-988-14047-6-3
ISSN: 2078-0958 (Print); ISSN: 2078-0966 (Online)

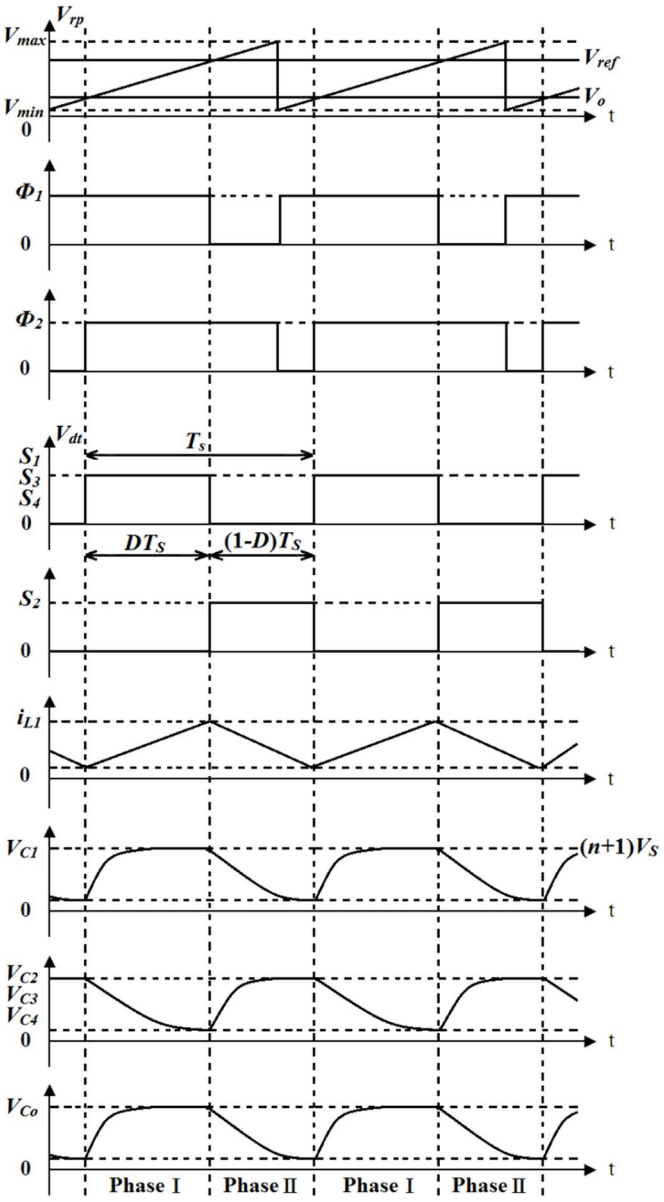

Fig. 3. Theoretical waveforms of SCISC.

B. *Control part*

The control part of SCISC is shown in the lower half of Fig. 1, and its detailed logic circuit is as in Fig. 2. It is composed of sawtooth wave generator, PWM block and non-overlapping circuit. In the sawtooth wave generator, first, a current mirror is employed for generating a constant current source to charge the capacitor C, and then voltage V_{rp} across this C is linearly increasing like a ramp. Next, V_{rp} is sent and compared with two external voltages V_{max} and V_{min} in the Schmitt trigger in order to keep the V_{rp} moving in the range between V_{max} and V_{min}, just like the waveforms as in Fig. 3. From the controller signal flow, the feedback signal Vo is sent into the OP-amp low-pass filter (LPF) for high-frequency noise rejection. The filtered signal Vo is compared with the desired output reference V_{ref} to produce the V_{dt} (D: duty cycle of signal V_{dt}) via the PWM block. And then, this duty-cycle signal is sent to the non-overlapping circuit for obtaining a set of non-overlapping phase signals so as to produce the driver signals of S_1-S_4 for the different topologies as in Fig. 4(a) and (b). The goal of PWM control is to keep V_o on following the different desired V_{ref} for better output regulation. In this paper, the closed-loop control will be achieved via the PWM-based compensator to improve the regulation capability of this converter.

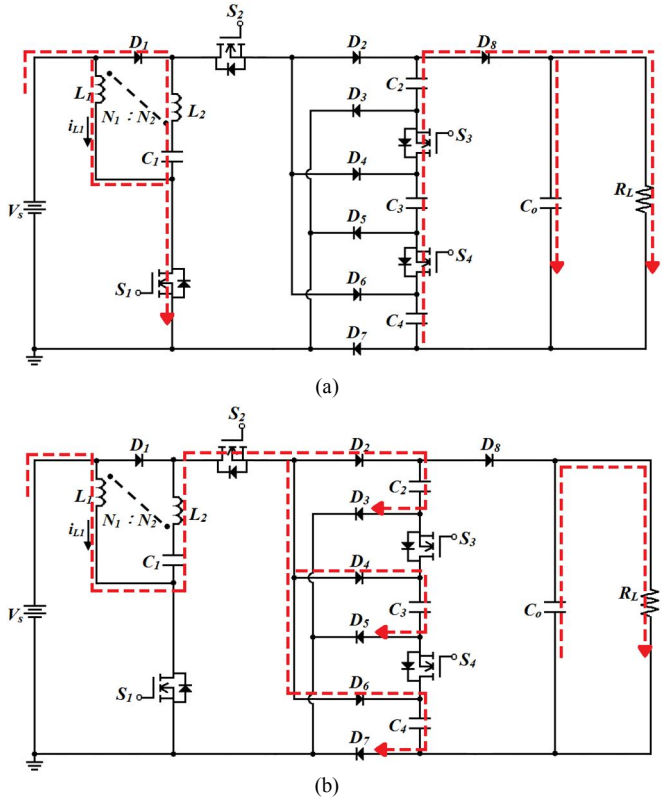

Fig. 4. Topologies for Phase (a) Ⅰ, and (b) Ⅱ.

Table Ⅰ. Component parameters of SCISC.

Supply source (Vs)	5V
Pumping capacitor (C_2~C_4)	10uF
Output capacitor (C_O)	50uF
Clamping capacitor (C_1)	50uF
Inductor (L_1, L_2)	L_1=100uH, L_2=1600uH (n=4)
Switching frequency (fs)	12.5kHz
Diodes : D_1~D_8	D1N5820
On-state resistance of MOSFETs (Ron)	50uΩ
Load resistor (R_L)	500Ω

III. EXAMPLES OF SCISCC

In this section, based on Fig. 1, this closed-loop converter is designed and simulated by OrCAD SPICE tool. The results are illustrated to verify the efficacy of the proposed converter. The component parameters of the proposed converter are listed in Table I. This converter is preparing to supply the standard load R_L=500Ω. For checking closed-loop performances, some topics will be simulated and discussed, including: (i) Steady-state responses (ii) Dynamic responses.

(i) Steady-state responses:

The closed-loop SCISC is simulated for V_{ref} = 190V / 180V / 170V respectively, and then these output results are obtained as shown in Fig. 5(a)-(b) / Fig. 5(c)-(d) / Fig. 5(e)-(f). In Fig. 5(a), it can be found that the settling time is about 40ms, and the steady-state value of V_O is really reaching 186.34V, and this converter is stable to keep V_O following V_{ref} (190V). In Fig. 5(b), the output ripple percentage is

ISBN: 978-988-14047-6-3
ISSN: 2078-0958 (Print); ISSN: 2078-0966 (Online)

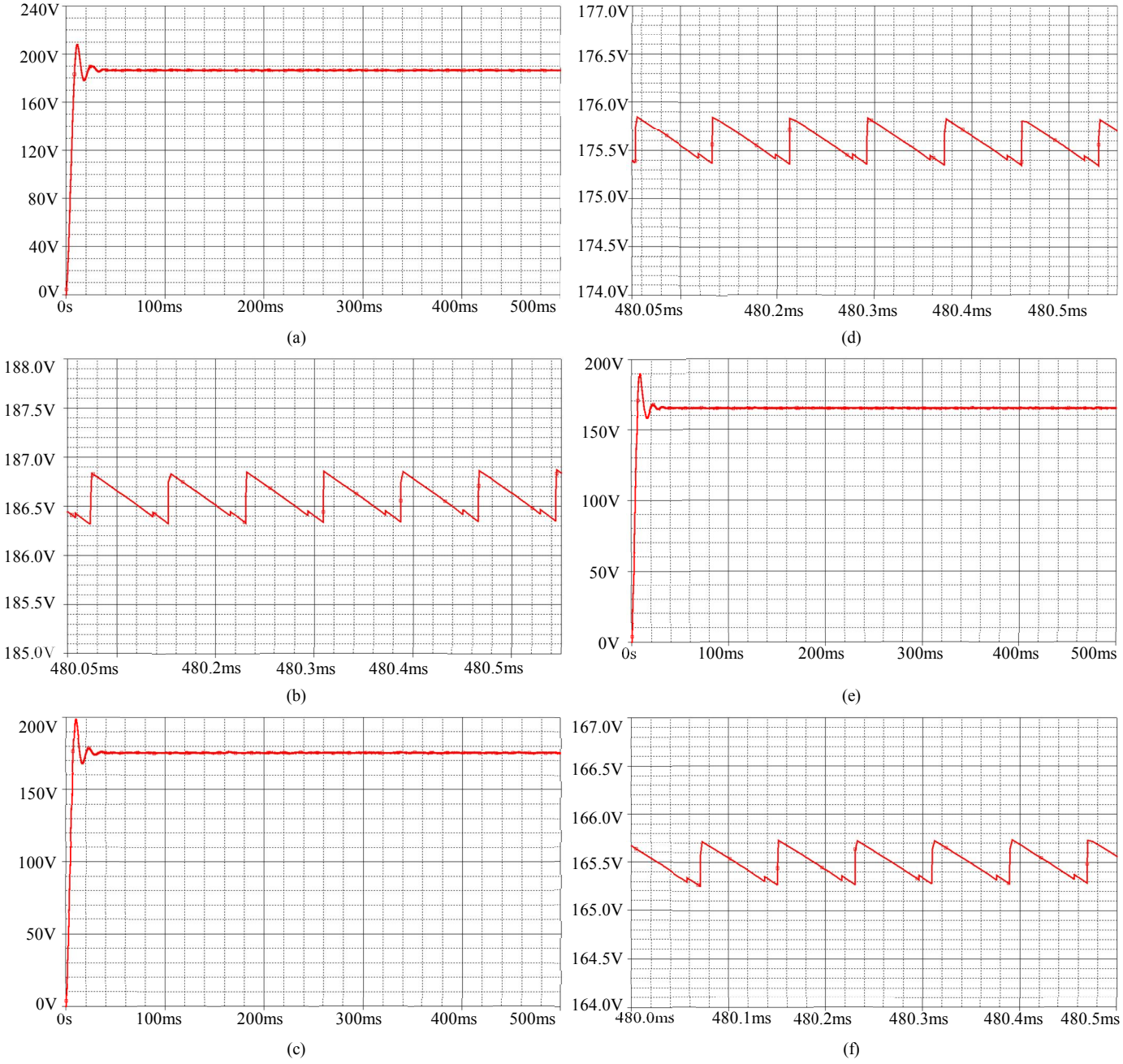

Fig. 5. Steady-state response of SCISC.
(a) V_O for V_{ref}=190V, (b) rp=0.265%, (c) V_O for V_{ref}=180V, (d) rp=0.256%, (e) V_O for V_{ref}=170V (f) rp=0.27%.

measured as rp = $\Delta v_o/V_O$ = 0.265%, and the power efficiency is obtained as η= 89.63%. In Fig. 5(c), the settling time is about 40ms, and the steady-state value of V_O is really reaching 175.397V. In Fig. 5(d), the output ripple percentage is measured as rp = $\Delta v_o/V_O$ = 0.256%, and the power efficiency is obtained as η= 91.1%. In Fig. 5(e), the settling time is about 40ms, and the steady-state value of V_O is really reaching 165.162V. In Fig. 5(f), the output ripple percentage is measured as rp = $\Delta v_o/V_O$ = 0.27%, and the power efficiency is obtained as η= 90.9%. These results show that the closed-loop SCISC converter has a high voltage gain and a good steady-state performance.

(ii) Dynamic responses:

Since the voltage of battery is getting low as the battery is working long time, or the bad quality of battery results in the impurity of source voltage, such a voltage variation should be considered as well as loading variation.

(a) Case Ⅰ: (source variation)

Assume that V_S is the DC value of 5.0V and extra plus a sinusoidal signal disturbance of $0.8V_{P\text{-}P}$ as in the Fig. 6(a), and then the waveform of V_o is obtained in the Fig. 6(b) (V_{ref}=190V). Clearly, by using the closed-loop control, V_o is still keeping on V_{ref} in spite of source disturbance.

(b) Case Ⅱ: (loading variation)

Assume that R_L is 500Ω normally, and it changes from 500Ω to 250Ω. After a short period of 100ms, the load recovers from 250Ω to 500Ω, i.e. R_L=500Ω→250Ω→500Ω as in Fig. 6(c). Fig. 6(d) shows the transient during waveform of V_O at the moment of loading

ISBN: 978-988-14047-6-3
ISSN: 2078-0958 (Print); ISSN: 2078-0966 (Online)

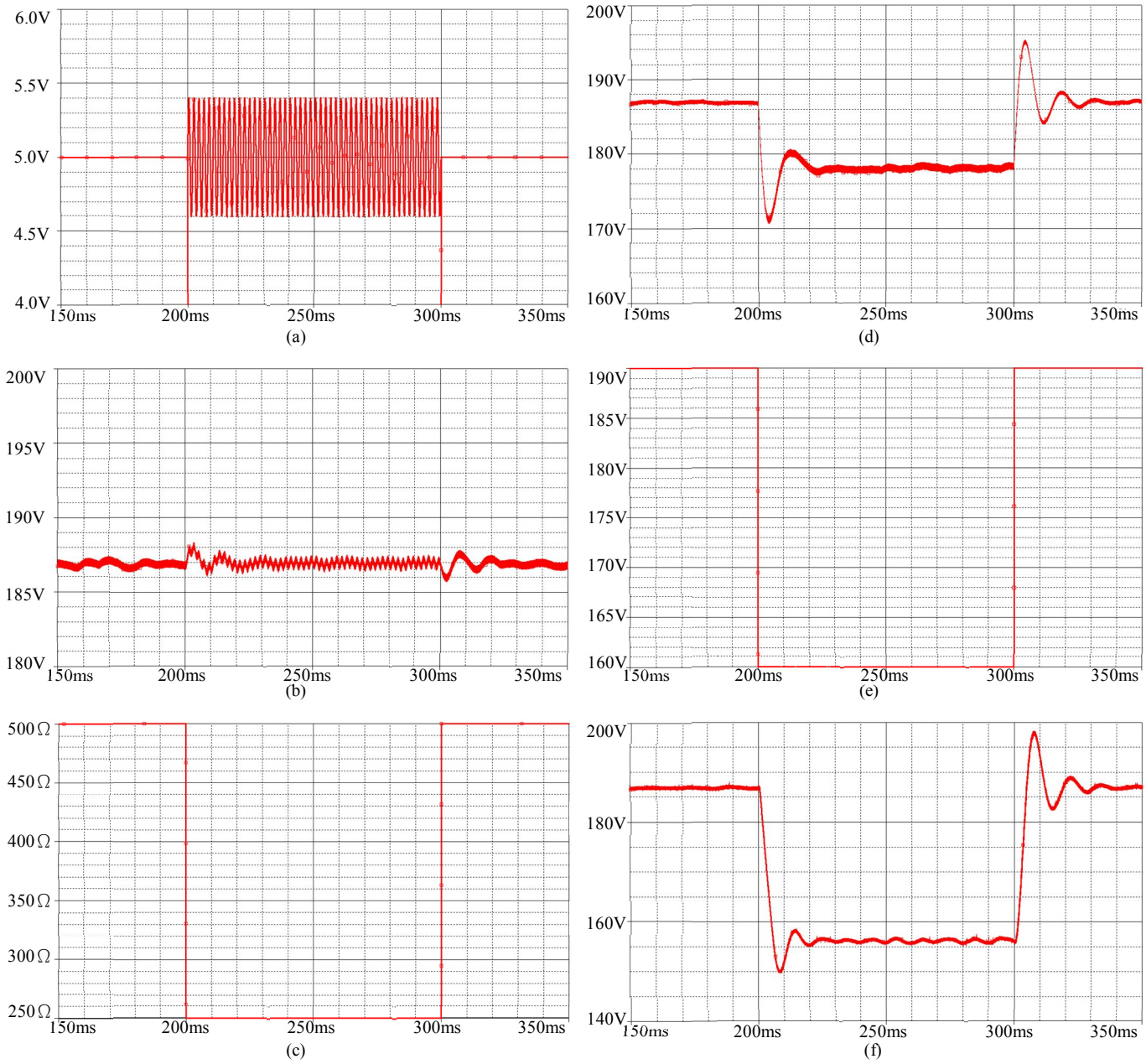

Fig. 6. Dynamic response of SCISC.
(a) V_S=5+sin(2π×1000t) V (b) V_O (Case Ⅰ), (c) R_L=500Ω→250Ω→500Ω, (d) V_O (Case Ⅱ), (e) V_{ref}=190V→160V→190V, (f) V_O (Case Ⅲ).

variations. It is found that V_o has a small drop (8V) at R_L : 500Ω→250Ω (increase 50% of loading). The curve shape becomes thicker the heavier load, i.e. the output ripple becomes bigger at this moment.

(c) Case Ⅲ: (reference variation)

Assume that V_{ref} is 190V normally, and it suddenly changes from 190V to 160V. After a short period of 100ms, the V_{ref} recovers from 160V to 190V, i.e. V_{ref}=190V → 160V → 190V as in Fig. 6(e). The waveform of V_O is obtained in the Fig. 6(f). It is found that V_O is still following V_{ref} via the closed-loop compensation, even though V_{ref} has a drop/jump of about 30V.

These results show that the closed-loop SCISC has the good output regulation capability to source/loading variations, as well as reference variation.

IV. Conclusions

A closed-loop high-gain SCISC converter is proposed by combining a sawtooth wave generator, PWM-based compensator and non-overlapping circuit for step-up DC-DC conversion and regulation. The advantages of the proposed scheme are listed as follows. (i) In the SCISC, the large conversion ratio can be achieved with four switches and five capacitors for a step-up gain of 37 or above. (ii) As for the higher step-up gain, it is easily realized through increasing the turn ratio or extending the number of pumping capacitors. (iii) The PWM technique is adopted here not only to enhance output regulation capability for the different desired output, but also to reinforce the output robustness against source/loading/reference variation. At present, the prototype circuit of the proposed converter is implemented in the laboratory as shown

ISBN: 978-988-14047-6-3
ISSN: 2078-0958 (Print); ISSN: 2078-0966 (Online)

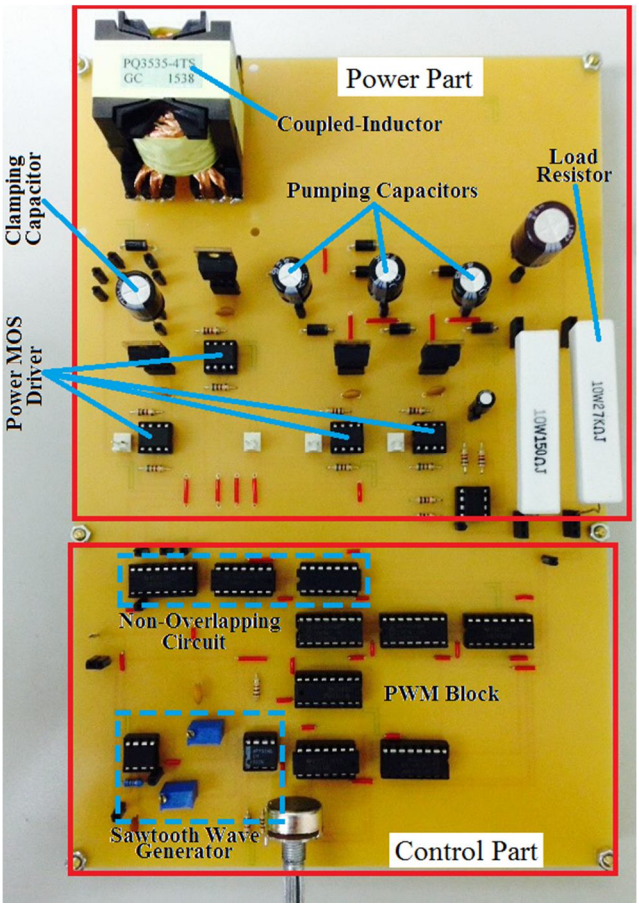

Fig. 7. Prototype circuit of SCISC.

the photo in Fig. 7. Some experimental results will be obtained and measured for the verification of the proposed converter.

REFERENCES

[1] G. Palumbo and D. Pappalardo, "Charge pump circuits: An overview on design strategies and topologies," *IEEE Circuits Syst. Mag.*, vol. 10, no. 1, pp. 31-45, 1st Quarter 2010.

[2] S. Singer, "Inductance-less up DC-DC convertor," *IEEE J. Solid State Circuits*, vol. SC-17, no. 4, pp. 778-781, Aug. 1982.

[3] J. K. Dickson, "On-chip high voltage generation in NMOS integrated circuits using an improved voltage multiplier technique," *IEEE J. Solid-State Circuits*, vol. SSC-11, no. 3, pp. 374-378, Jun. 1976.

[4] T. Tanzawa and T. Tanaka, "A dynamic analysis of the Dickson charge pump circuit," *IEEE J. Solid-State Circuits*, vol. 32, no. 8, pp. 1231-1240, Aug. 1997.

[5] O. C. Mak, Y. C.Wong, and A. Ioinovici, "Step-up DC power supply based on a switched-capacitor circuit," *IEEE Trans. Ind. Electron.*, vol. 42, no. 1, pp. 90-97, Feb. 1995.

[6] H. Chung and A. Ioinovici, "Switched-capacitor-based DC-to-DC converter with improved input current waveform," in *Proc. IEEE Int. Symp. Circuits Syst.*, Atlanta, GA, USA, 1996, pp. 541-544.

[7] G. Zhu and A. Ioinovici, "Steady-state characteristics of switched-capacitor electronic converters," *J. Circuits, Syst., Comput.*, vol. 7, no. 2, pp. 69-91, 1997.

[8] O. C. Mak and A. Ioinovici, "Switched-capacitor inverter with high power density and enhanced regulation capability," *IEEE Trans. Circuit Syst. I*, vol. 45, pp. 336-347, Apr. 1998.

[9] Y.-H. Chang, "Design and analysis of power-CMOS-gate-based switched-capacitor boost DC-AC inverter," *IEEE Trans. Circuits Syst. I: Fundamental Theory Appl.*, vol. 51, no. 10, pp. 1998-2016, Oct. 2004.

[10] S.-C. Tan, S. Bronstein, M. Nur, Y.M. Lai, A. Ioinovici, and C. K. Tse, "Variable structure modeling and design of switched-capacitor converters," *IEEE Trans. Circuits Syst. I: Reg. Papers*, vol. 56, no. 9, pp. 2132-2141, Sep. 2009.

[11] Y.-H. Chang, "Variable-conversion-ratio switched-capacitor-voltage-multiplier/divider DC-DC converter," *IEEE Trans. Circuits Syst. I: Reg. Paper*, vol. 58, no. 8, pp. 1944-1957, Aug. 2011.

[12] Y.-H. Chang, "A gain/efficiency-improved serial-parallel switched-capacitor step-up DC-DC converter," *IEEE Trans. Circuits Syst. I: Reg. Paper*, vol. 60, no. 10, pp. 2799-2809, Oct. 2013.

[13] Yuen-Haw Chang and Yu-Jhang Chen, "High-gain switched-inductor switched-capacitor step-up DC-DC converter," *International MultiConference of Engineers and Computer Scientists 2013 (IMECS'2013)*, vol. 2, pp. 670-675, Hong Kong, March 13-15, 2013.

[14] Gang Wu, "Non-isolated high step-up DC-DC converters adopting switched-capacitor cell," *IEEE Trans. Ind. Electron.,* vol. 62, no. 1, pp. 383-393, Jan. 2015.

[15] B. Axelrod and Y. Berkovich, "Switched-coupled inductor cell for DC–DC converters with very large conversion ratio," *IET Power Electron.*, vol. 4, no. 3, pp. 309-315, Mar. 2011.

[16] Shih-Ming Chen, "A novel switched-coupled-inductor DC-DC step-up converter and its derivatives," *IEEE Trans. Industry Applications.,* vol. 51, no. 1, pp. 309-314, Jan. 2015.

ISBN: 978-988-14047-6-3
ISSN: 2078-0958 (Print); ISSN: 2078-0966 (Online)