A High-Gain Multiphase Switched-Capacitor Coupled-Inductor Step-Up DC-DC Converter

Yuen-Haw Chang and En-Ping Jhao

Abstract—A closed-loop scheme of a high-gain multiphase switched-capacitor coupled-inductor (MSCCI) converter is proposed by combining a phase generator and pulse-width-modulation-based (PWM-based) gain compensator for step-up DC-DC conversion and regulation. The power part between source V_S and output V_O contains a three-stage serial-parallel switched-capacitor (SC) circuit plus a coupled-inductor device, and it raises the voltage gain up to $4[(n+1)+(1+nD)/(1-D)]$ at most, where D means the duty cycle of PWM and n is trun ratio of coupled inductor. Practically, this MSCCI can boost the voltage gain up to 44 when D=0.5, n=4. Further, the PWM technique is adopted not only to enhance the output regulation for the compensation of the dynamic error between the practical and desired outputs, but also to reinforce output robustness against source or loading variation. Finally, the closed-loop MSCCI is designed by SPICE and simulated for some cases: steady-state and dynamic responses. All results are illustrated to show the efficacy of the proposed scheme.

***Index Terms*—high-gain, pulse-width-modulation, step-up converter, multiphase switched-capacitor coupled-inductor.**

I. Introduction

Recently, with the rapid development of power electronics, the step-up DC-DC converters are emphasized more widely for the electricity-supply applications, such as lighting device, smart phone, medical equipment. General speaking, these power electronics converters are always required for a small volume, a light weight, a high efficacy, and a better regulation capability.

The switched-capacitor converter (SCC), possessed of the charge pump structure, is one of solutions to DC-DC power conversion because it has only semiconductor switches and capacitors. Unlike traditional converters, the inductor-less SCC has light weight and small volume. Up to now, many types have been suggested [1], [2], and some well-known topologies are presented, e.g. Dickson charge pump, Ioinovici SC. In 1976, Dickson charge pump was proposed with a two-phase diode-capacitor chain [3], [4], but it has the drawbacks of fixed gain and large device area. In the 1990s, Ioinovici proposed a SCC with two symmetrical capacitor cells, and presented a current-mode SCC [5], [6]. In 1997, Zhu and Ioinovici performed a comprehensive steady-state analysis of SCC [7]. In 1998, Mak and Ioinovici suggested a high-power-density SC inverter [8]. In 2004, Chang presented a current-mode SC inverter [9]. In 2009, Tan *et al*. proposed the modeling and design of SCC by variable structure control [10]. In 2011, Chang proposed an integrated step-up/down SCC (SCVM/ SCVD) [11]. In 2013, Chang proposed a gain/efficiency-improved serial-parallel switched-capacitor converter (SPSCC) by combining an adaptive-conversion-ratio (ACR) and pulse-width-modulation (PWM) control [12]. In 2016, Chang proposed a switch-utilization-improved switched-inductor switched-capacitor converter with adapting stage number (SISCC) is proposed by phase generator and PWM control [13].

For a higher voltage gain, it is one of the good ways to utilize the device of coupled-inductor. Nevertheless, the stress on transistors and the volume of magnetic device must be considered. In 2011, Berkovich *et al*. proposed a switched-coupled inductor cell for DC-DC converter with very large conversion ratio [14]. In 2015, Chen *et al*. proposed a novel switched-coupled-inductor DC-DC step-up converter via adopting a coupled inductor to charge a switched capacitor for making voltage gain effectively increased. Not only lower conduction losses but also higher power conversion efficiency is benefited from a lower part count and lower turn ratio [15]. Here, we try to combine a three-stage SC circuit with one coupled-inductor to propose a closed-loop MSCCI converter for realizing a high-gain conversion as well as enhancing the regulation capability.

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II. Configuration of MSCCI

Fig. 1 shows the overall circuit configuration of MSCCI step-up converter, and it contians two major parts: power part and control part for achieving the high-gain step-up DC-DC conversion and closed-loop regulation.

A. Power part

The power part of MSCCI is shown in the upper half of Fig. 1, and is composed of a multiphase serial-parallel switched-capacitor circuit plus combining a coupled-inductor device. The converter contains one coupled-inductor (L_1,L_2) with the turn ratio n ($n=N_2/N_1$), five switches (S_1-S_5), one clamping capacitor (C_1), two pumping capacitors (C_2-C_3), one output capacitor (C_O) and four diodes (D_1-D_4), where C_2 and C_3 has the same capacitance C ($C_2=C_3=C$). Fig. 2 shows the theoretical waveforms of MSCCI in one switching cycle T_{PWM} ($T_{PWM}=1/f_{PWM}$, f_{PWM}: switching frequency of PWM). A cycle T_S includes four steps (Step I_0, I_1, I_2, I_3), and each step has two phases (*Phase I* and *Phase II*) with the different time duration: DT_{PWM} and $(1-D)T_{PWM}$, where D is the duty cycle of PWM control. The operations for Step I_0-I_3 are described as follows.

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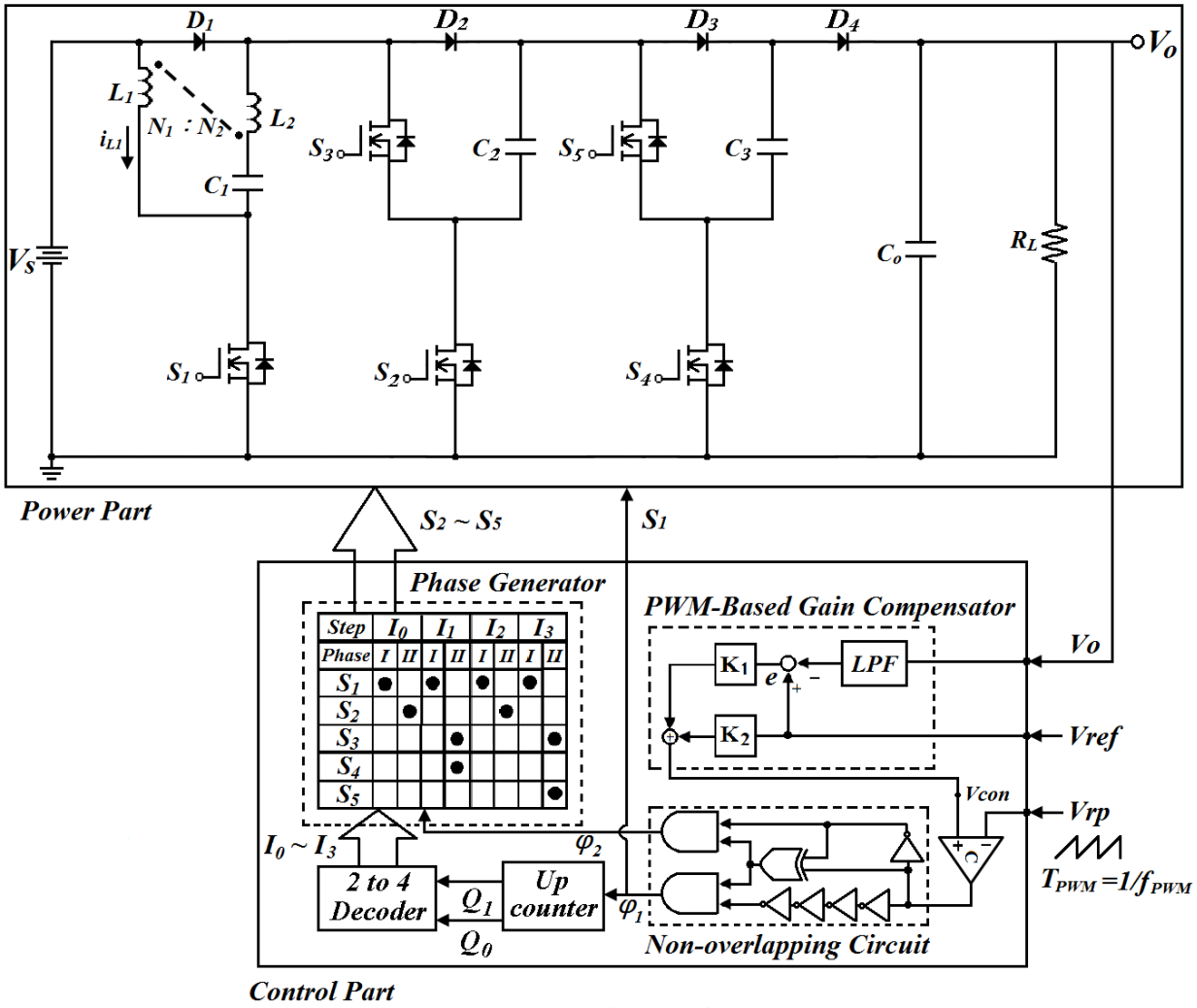

Fig. 1. Closed-loop configuration of MSCCI.

(i) *Step* I_0 :

(a) *Phase I* :

Let S_1 turn on, and the others be off. Then, the diodes D_1 is turned on, and the diodes D_2-D_4 are all off. The current-flow path is shown in Fig. 3(a). The inductor L_1 is charged by source V_S, and the energy is simultaneously transfered from the first side of the coupled-inductor to the secondary side for making the voltage across L_2 being nV_S. And then, the inductor L_2 is discharged in series together with V_S. to have the steady-state voltage of C_1 towards the value of $(n+1)V_S$. At the same time, output capacitor C_O just stands alone to supply load R_L.

(b) *Phase II* :

Let S_2 turn on, and the others be off. The diodes D_2 is on, and D_1, D_3, D_4 are all off. The current-flow path is shown in Fig. 3(b). The capacitors C_2 is charged by V_S in series together with V_{L1}, V_{L2} and V_{C1}, i.e. transferring the previous energy stored in L_1, L_2 and C_1 into C_2. Thus, the steady-state voltage of V_{C2} can reach towards the value of $[(n+1)+(1+nD)/(1-D)]V_S$. At the same time, output capacitor C_O just stands alone to supply load R_L.

(ii) *Step* I_1 :

(a) *Phase I* : Identical to *Phase I* of *Step* I_0.

(b) *Phase II* :

Let S_3, S_4 turn on, and the others be off. The diode D_3 is on, and D_1, D_2, D_4 are off. The current-flow path is shown in Fig. 3(c). The capacitors C_3 are charged by V_S in series together with V_{L1}, V_{L2}, V_{C1}, V_{C2} . i.e. transferring the previous energy stored in L_1, L_2 C_1 and C_2 into C_3. Thus, the steady-state voltage of V_{C3} can reach towards the value of $2V_{C2}$.

(iii) *Step* I_2 :

(a) *Phase I* : Identical to *Phase I* of *Step* I_0.

(b) *Phase II* : Identical to *Phase II* of *Step* I_0.

(iv) *Step* I_3 :

(a) *Phase I* : Identical to *Phase I* of *Step* I_0.

(b) *Phase II* :

Let S_3, S_5 turn on, and the others be off. The diode D_4 is on, and D_1, D_2, D_3 are off. The current-flow path is shown in Fig. 3(d), and is going from source V_S, through L_1, L_2, C_1, C_2, C_3, to output capacitor C_O and load R_L. This topology has the connection in series of V_S,V_{L1}, V_{L2}, V_{C1}, V_{C2} and V_{C3} in order to provide a higher voltage for transferring the energy into the output terminal (C_O and R_L).

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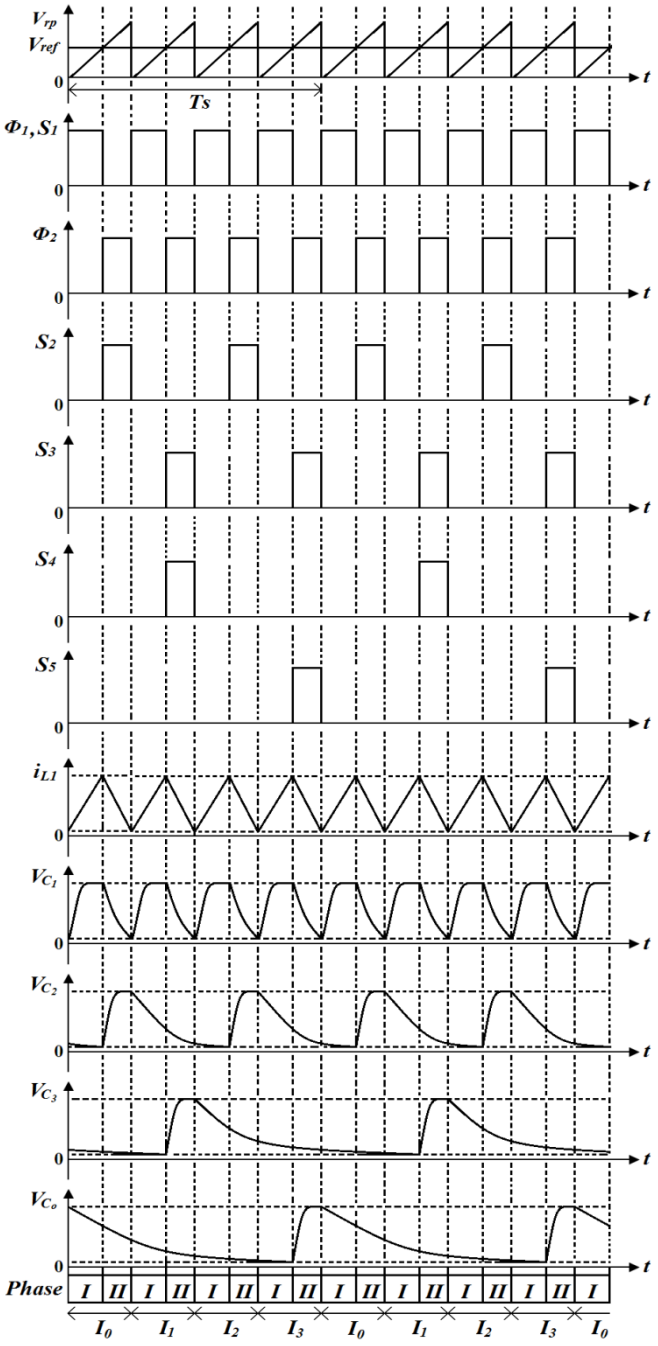

Fig. 2. Theoretical waveforms of MSCCI.

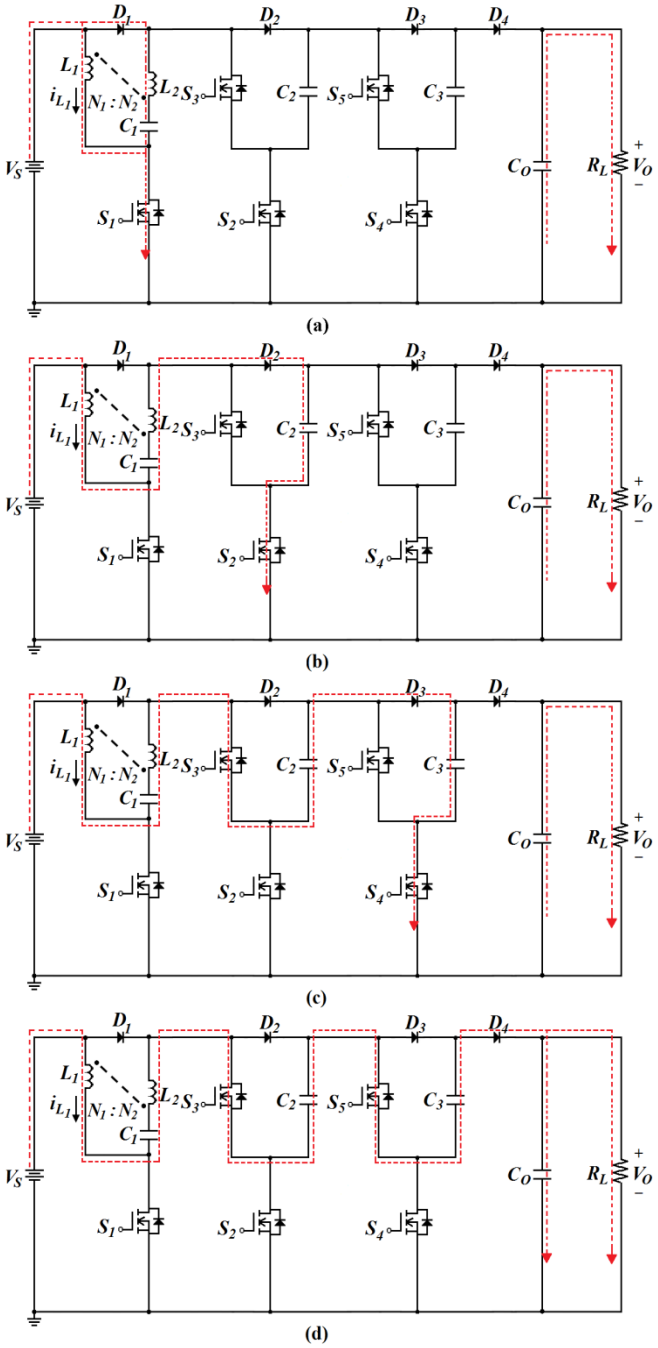

Fig. 3. Topologies for (a) Phase I of I_0-I_3；(b) Phase II of I_0,I_2；(c) Phase II of I_1；(d) Phase II of I_3.

Based on the cyclical operations of Step I_0-I_3, the overall step-up gain can reach to the value of $4[(n+1)+(1+nD)/(1-D)]V_S$ at most theoretically. Extending the capacitor count, the gain can be boosted into the value of $2^m[(n+1)+(1+nD)/(1-D)]V_S$, where m is the number of pumping capacitors.

B. Control part

The control part of MSCCI is shown in the lower half of Fig.1. It is composed of low-pass filter (LPF), a PWM-based gain compensator, an up counter, a 2 to 4 decoder and phase generator. From the controller signal flow, the feedback signal V_O is fed back into the OP-amp LPF for high-frequency noise rejection. Next, the control signal *Vcon* (related to the error signal $e=Vref-V_O$ via gains K_1 and K_2) is compared with the ramp *Vrp* to generate the duty-cycle signal DT_{PWM} of PWM. And then, the signal DT_{PWM} is sent to the non-overlapping circuit for producing a set of non-overlapping phase signals： φ_1 and φ_2. And then the signal φ_1 of non-overlapping phase signals is sent to the up counter for producing Q_0 and Q_1. After that the signals Q_0 and Q_1 are sent to the 2 to 4 decoder for obtaining a set of step signals：I_0, I_1, I_2, I_3 for the driver of multiphase operation as mentioned above. With the help of these signals： φ_2 and I_0-I_3 , the phase generator (realized by digital logic gates) can generate the driver signals of switches S_2-S_5 just like the waveforms of Fig. 2. To summarize, the digital rules of switch driver signals are listed as：

1) $S_1 = \varphi_1$,
2) $S_2 = (I_0 + I_2)\varphi_2$,
3) $S_3 = (I_1 + I_3)\varphi_2$,

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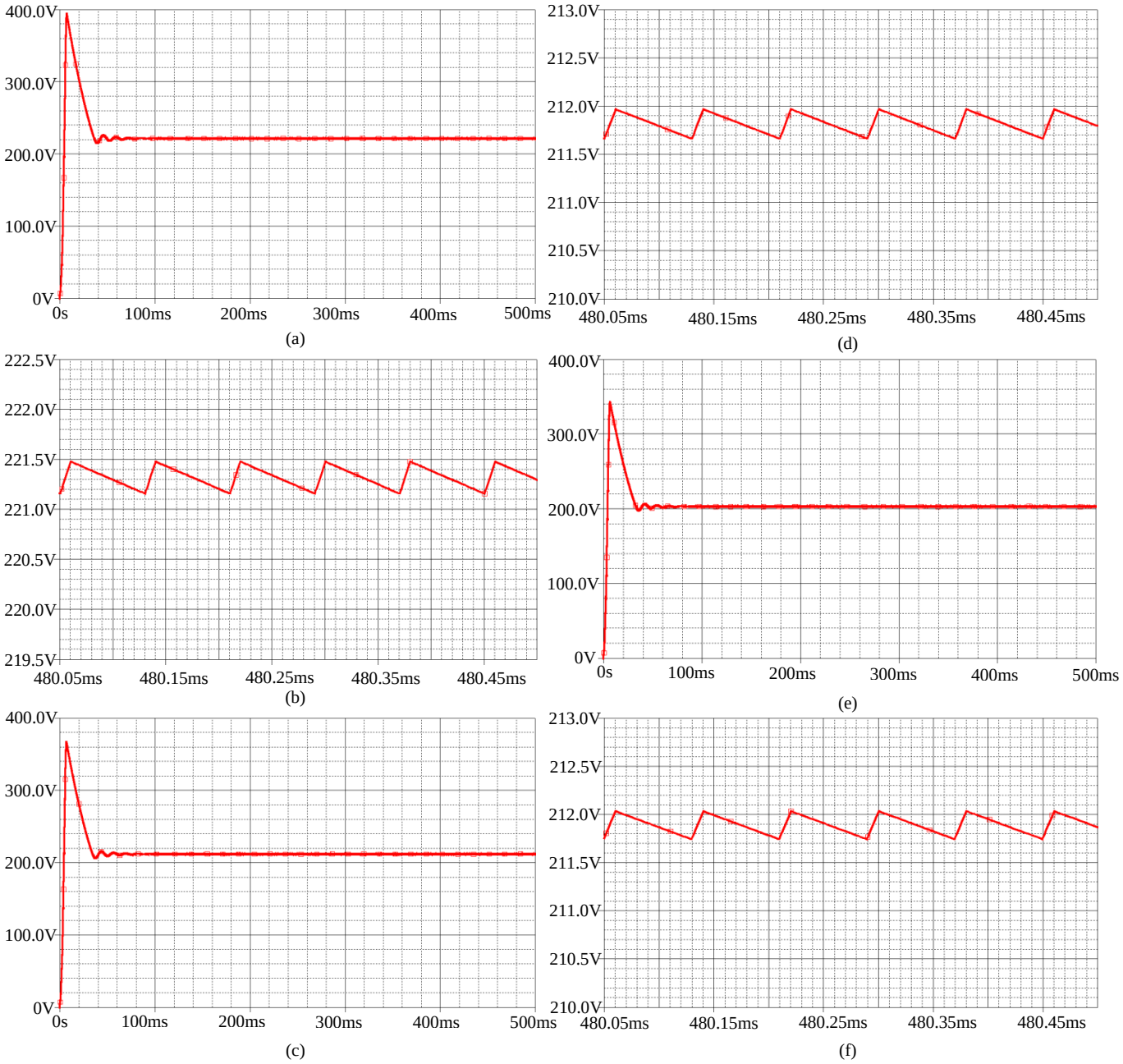

Fig. 4. Steady-state responses of MSCCI.
(a) V_O for V_{ref}=220V, (b) rp=0.144%, (c) V_O for V_{ref}=210V, (d) rp=0.143%, (e) V_O for V_{ref}=200V (f) rp=0.141%.

4) $S_4 = I_1 \varphi_2$,
5) $S_5 = I_3 \varphi_2$.

The main goal is to generate the driver signals of these MOSFETs for the different topologies as in Fig. 3(a)-(d), and further the closed-loop control can be achieved via the PWM-based compensator and phase generator in order to improve the regulation capability of this converte.

III. Examples of MSCCI

In this section, based on Fig. 1, this closed-loop converter is designed and simulated by SPICE tool. The results are illustrated to verify the efficacy of the proposed converter. The component parameters of the proposed converter are listed in Table I. This converter is preparing to supply the standard load R_L=500Ω. For checking closed-loop performances, some topics will be simulated and discussed, including: (i) Steady-state responses, (ii) Dynamic responses.

(i) Steady-state responses：

The closed-loop MSCCI is simulated for *Vref* = 220V/ 210V/ 200V respectively, and then these output results are obtained as shown in Fig.4(a)-(b) / Fig. 4(c)-(d) / Fig. 4(e)-(f). In Fig. 4(a), it can be found that the settling time is about 80ms, and the steady-state value of V_O is really reaching 221.48V, and this converter is stable to keep V_O following *Vref* (220V). In Fig. 4(b), the output ripple percentage is measured as rp = $\Delta v_o/V_O$ = 0.144%, and the power efficiency is obtained as η= 85.1%. In Fig. 4(c), the settling time is about 80ms, and the steady-state value of V_O is really reaching 211.96V. In Fig. 4(d), the output ripple percentage is measured as rp = $\Delta v_o/V_O$ = 0.143%, and the power efficiency is obtained as η=85.59%. In Fig. 4(e), the settling time is about 80ms, and the steady-state value of V_O is really reaching 203.03V.

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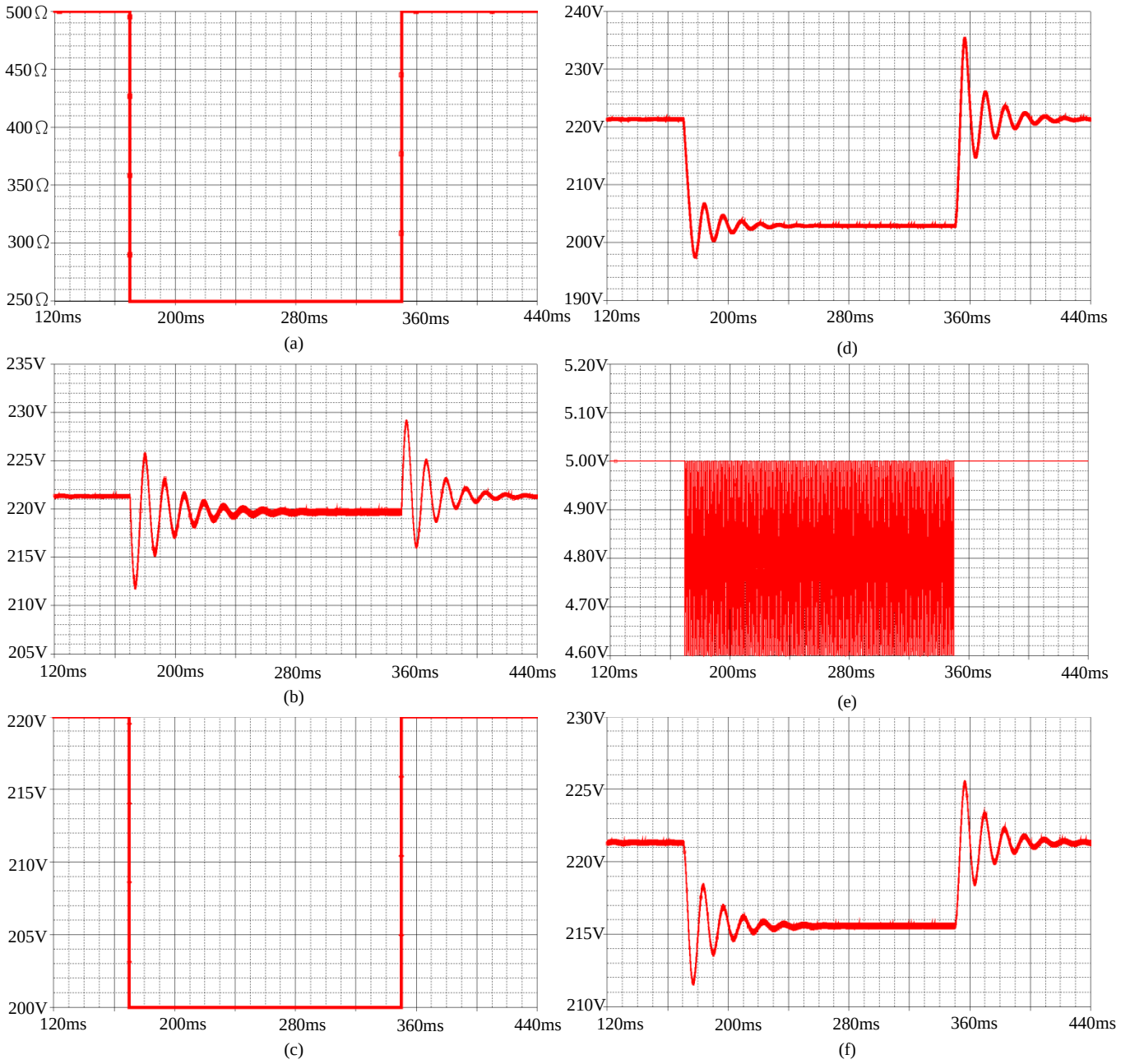

Fig. 5. Dynamic response of MSCCI.
(a) R_L=500Ω→250Ω→500Ω, (b) V_O (Case I); (c) V_{ref}=220V→200V→220V, (d) V_O (Case II); (e) V_S=4.8+0.2sin(2π×1000t) V, (f) V_O (Case III).

In Fig. 4(f), the output ripple percentage is measured as rp = $\Delta v_o/V_O$ = 0.141%, and the power efficiency is obtained as η= 85.98%. These results show that the closed-loop MSCCI converter has a high voltage gain and a good steady-state performance.

(ii) Dynamic responses：

Since the voltage of battery is getting low as the battery is working long time, or the bad quality of battery results in the impurity of source voltage, such a voltage variation should be considered as well as loading variation.

(a) Case I：(loading variation)

Assume that R_L is 500Ω normally, and it changes from 500Ω to 250Ω. After a short period of 180ms, the load recovers from 250Ω to 500Ω, i.e. R_L=500Ω→250Ω→500Ω as in Fig.5(a). Fig.5(b) shows the transient during waveform of V_O at the moment of loading variations. It is found that V_o has a small drop (1.5V) at R_L : 500Ω→250Ω (double loading). The curve shape becomes thicker during the period of the heavier load, i.e. the output ripple becomes bigger at this moment. Even though the double loading happens, it can be found that V_O still follows *Vref* (220V).

(b) Case II：(reference variation)

Assume that *Vref* is 220V normally, and it suddenly changes from 220V to 200V. After a short period of 180ms, the *Vref* recovers from 200V to 220V, i.e. *Vref*=220V→200V→220V as in Fig. 5(c). The waveform of V_O is obtained in the Fig. 5(d). It is found that V_O is still following *Vref* via the closed-loop compensation, even though *Vref* has a voltage drop of about 18.45V.

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Table I. Component parameters of MSCCI.

Supply source (V_S)	5V
Clamping capacitor (C_1)	100μF
Pumping capacitor (C_2,C_3)	10μf
Output capacitor (C_O)	100μF
Inductor (L_1, L_2)	L_1=40μH, L_2=640μH (n=4)
Switching frequency (f_{PWM})	50kHz
Diodes : D_1~D_4	D1N5834
On-state resistance of MOSFETs (Ron)	50μΩ
Load resistor (R_L)	500Ω

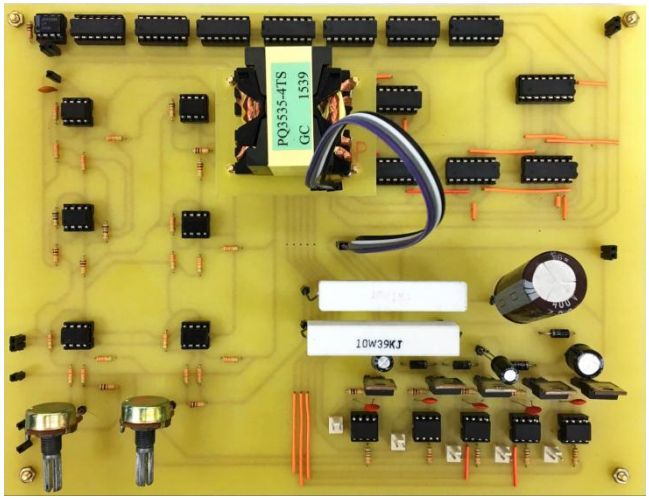

Fig. 6. Prototype circuit of MSCCI.

(c) Case III：(source variation)

Assume that V_S is the DC value of 4.8V and extra plus a sinusoidal signal disturbance of $0.4V_{P\text{-}P}$ as in the Fig. 5(e), and then the waveform of V_O is obtained in the Fig. 5(f) (*Vref*=220V). Clearly, by using the closed-loop control, V_O is still keeping on *Vref* in spite of source disturbance.

IV. Conclusions

A closed-loop high-gain MSCCI converter is proposed by combining a phase generator and PWM-based gain compensator for step-up DC-DC conversion and regulation. (MSCCI： $V_S \rightarrow V_O$： $2^m[(n+1)+(1+nD)/(1-D)]V_S$). Finally, the closed-loop MSCCI converter is designed and simulated by SPICE for some cases： steady-state and dynamic responses. The advantages of the proposed scheme are listed as follows. (i) In the MSCCI, the large conversion ratio can be achieved with five switches, three capacitors, and one coupled-inductor for a step-up gain of 44 or above. (ii) As for the higher step-up gain, it is easily realized through increasing the turn ratio or extending the number of pumping capacitors. (iii) The PWM technique is adopted here not only to enhance output regulation capability for the different desired output, but also to reinforce the output robustness against source/loading variation. At present, the prototype circuit of the proposed converter is implemented in the laboratory as shown the photo in Fig. 6. Some experimental results will be obtained and measured for the verification of the proposed converter.

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