Influence of Temperature to Electron Mobility on Top of Channel in 14 nm n-FinFET

Nuttapong Patcharasardtra, Weera Pengchan, *Member, IAENG*

***Abstract*—The temperature behavior that influential to the electron mobility on top surface in 14 nanometer FinFET channel. The Mobility could find on I-V characterizing simulation process and giving the result from the TCAD software by biasing on the FinFET structure with gate voltage at 1 volt and the drain-source voltage from 0 Volt to 1 Volt to obtain the saturation drain current from I-V characteristic. The Electron mobility was lowering by increasing the temperature from 303K (30°C) to 353K (80°C). This FinFET structure gave the $I_{DS\ (Sat)}$ about 29 µA and gave mobility at V_{DS} = 0 Volt about 575 cm^2/Vs, at V_{DS} = 1 Volt, the mobility dramatically down to 3.4 cm^2/Vs.**

Index Terms—FinFET, Electron Mobility, Device Simulation, Temperature Effect

I. Introduction

The device that brings solution to be a good smaller transistor in present, SOI Tri-gate FET. One kind of MOS structure consisted of silicon fin on silicon layers on top of BOX (buried oxide). It is a popular device in terms of research and commercial but, on them operate the temperature is a main parameter that forward to know mechanism of electron. There are two parameters as the electron concentration and the carrier mobility. Those two parameters have directly relationship because they have base of temperature. The solution to enhance the mobility of electron could be controlled by two parameters; the gate voltage and the temperature. While the gate voltage is enough and temperature has low, electron mobility will increased but when temperature has increased electron mobility will go down [1]. The parasitic resistance improving is the main condition that provided the good characteristics to devices including the mobility between the electron and hole [2]. This brings author interested to the mobility of the electron on top of channel in Tri-gate n-FinFET device by using the simulation method for studying the temperature effect of device structure to improve the research and reference the new experiment in the future.

Manuscript received December 21, 2016; revised February 8, 2017.

N. Patcharasardtra is with Department of Electronics Engineering, Faculty of engineering, King Mongkut's Institute of Technology Ladkrabang, Bangkok ,Thailand (corresponding e-mail: nuttapong_pat@hotmail.com)

W. Pengchan is with Department of Electronics Engineering, Faculty of engineering, King Mongkut's Institute of Technology Ladkrabang, Bangkok ,Thailand (e-mail: weera.pe@kmitl.ac.th)

II. Theory

A. Drain current saturation

The relationship between drain current and voltage (I-V), there is two states of this characteristic as linear and saturation. The drain current saturation was coming with linear part of threshold voltage that bring I_D from linear situations to saturation state and this current will not change by the gate voltage. The saturation drain current ($I_{D\ (Sat)}$) can solve by (1) [3]:

$$I_{D(sat)} = \varphi + \mu C_{OX} \cdot \frac{W_g}{L_g} \cdot \frac{(V_{gs} - V_{ds})^2}{2m} \quad (1)$$

$m = 1 + \frac{3 \cdot t_{ox}}{t_{si}}$, µ is electron mobility, C_{ox} is gate oxide capacitance (F/nm), V_{ds} is drain-source voltage (V), V_{gs} is gate voltage (V), W_g is FinFET gate width(nm), L_g is FinFET gate length (nm).

B. Electron mobility

The electron start moving by the applied of electrical field the mobility can calculate with (2) [4]:

$$\mu = \frac{V_d}{E} \quad (2)$$

E is magnitude of electric field (V/m^{-1}), V_d is drift velocity (V/cm).

III. Device structure simulation

The GTS framework by Global TCAD Solution [5] has used in this research. This software could be creating many kind of semiconductor devices but outstanding on MOS structure. The 14 nm n-FinFET was created by structure tool. It has 10 nanometer silicon layer thicknesses, 5 nanometer fin width with 90 nanometer on p-type silicon substrate and 14 nanometer gate length with 1 nanometer gate $1x10^{15}$ cm^{-3} n-dopant concentration and $3x10^{20}$ cm^{-3} on drain-source. The junction depth is about 1 nanometer. The gate electrode poly-silicon, drain and source electrodes were aluminum.

ISBN: 978-988-14047-7-0
ISSN: 2078-0958 (Print); ISSN: 2078-0966 (Online)

IV. Experiment

This paper has two parts of experiment. The first part is devices structure design by using the structure tool of software to create the structure and determine dopant concentration. The other one is device characteristics simulation. The current and voltage characteristics (I-V) giving by biasing to the structures by determining V_{DS} from 0 to 1 volt with 0.1 volt per step and V_{GS} at 1 volt to provide the relationship between electron mobility and structure temperature from 303K (30°C) to 353K (80°C) by increase 10K (10°C) per step. This relationship can give from I-V characteristic.

V. Results and Discussion

A. The tri-gate n-FinFET structure

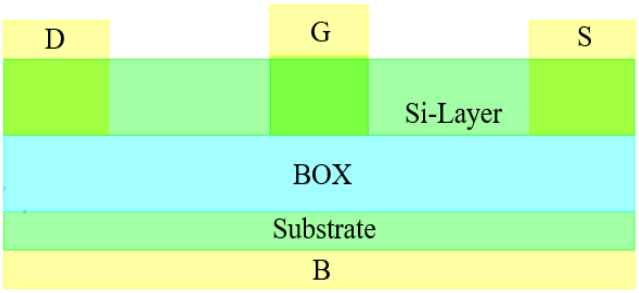

Fig. 1 (a)

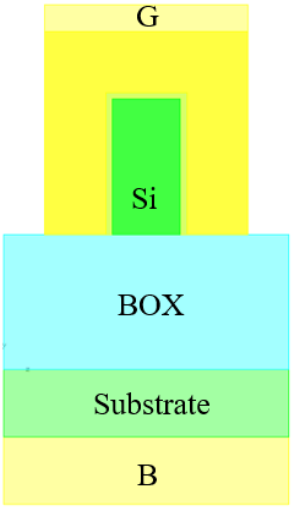

Fig. 1 (b)

Fig. 1 (a) tri-gate n-FinFET structure side view (b) cross section

Fig. 1 is the device structure and determined dopant concentration on device simulation structure topic. The FinFET structures consist of bulk contact, substrate, BOX, Si-layer, gate oxide (SiO_2), gate contact (Poly-Si) and drain source contact (Al).

B. I-V characteristic

This characteristic obtains the output current of tri-gate FinFET that control by gate voltage and drain-source voltage in case of difference temperature. This characteristic on six temperatures was shown in fig. 2.

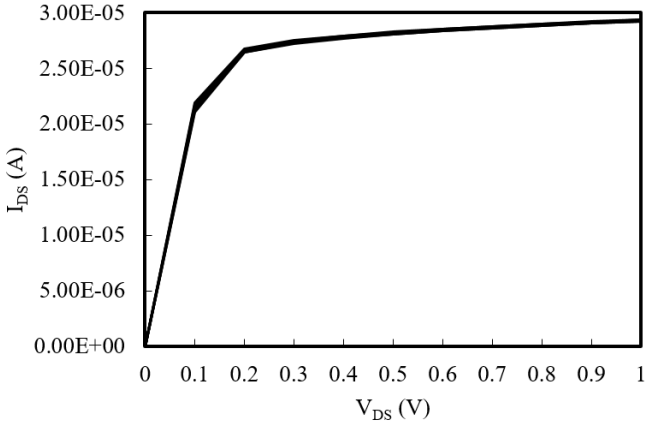

Fig. 2 I-V characteristics of FinFET with temperatures

In fig. 2, the saturation drain current value is the most significant attribute that giving the effect from increasing of temperature. This structure can give maximum current but average of this result has not slightly decrease.

C. Saturation drain current and temperatures

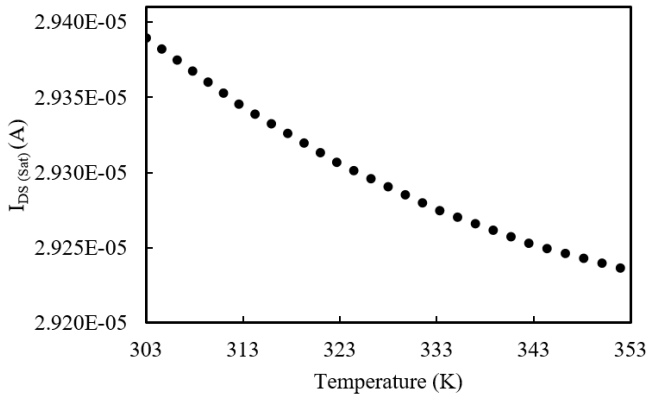

Fig. 3 Relationship between saturation drain current and temperatures

Influence of temperature taking effect on I-V characteristic is shown in fig. 2. The saturation drain current steadily decreased by the increasing of temperature from 303K to 353K. I-V characteristic result obtains the saturation drain current about 29 µA is shown in fig. 3.

D. Electron Mobility mechanism

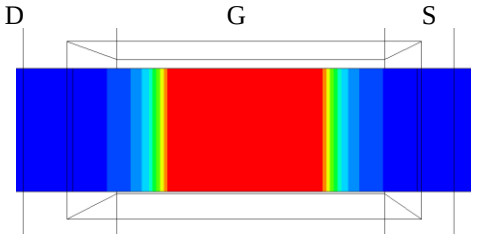

Fig. 4 (a)

ISBN: 978-988-14047-7-0
ISSN: 2078-0958 (Print); ISSN: 2078-0966 (Online)

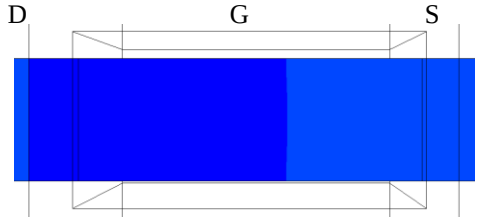

Fig. 4 (b)

Fig. 4 Electron mobility on top of channel (a) V_{DS} = 0 V (b) V_{DS} = 1 V at 303K structure temperature

Fig. 4(a) is the top view of FinFET structure. When giving gate voltage at 0 V, the electron mobility has higher on the middle top of the channel and lowering on the left and right. The result after biasing, the mobility was dramatically lowering because the electric field magnitude was increased and took a little left shift to drain area by effect of high temperature as shown in fig. 4(b).

Moreover the variation in mobility is not only change with the enlargement of temperature. The drift velocity and electric field magnitude is mainly parameter to determine the mobility.

E. Electron mobility and temperature

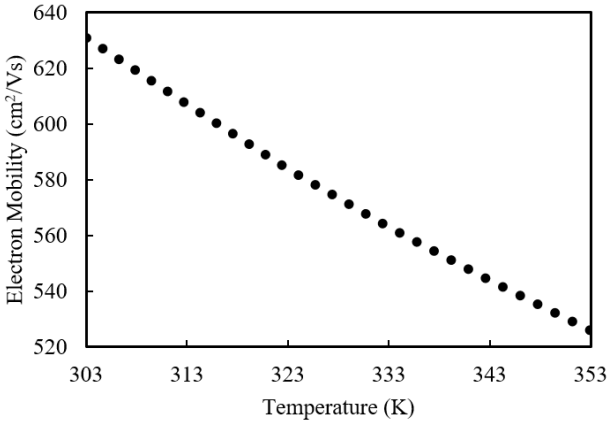

Fig. 5 (a)

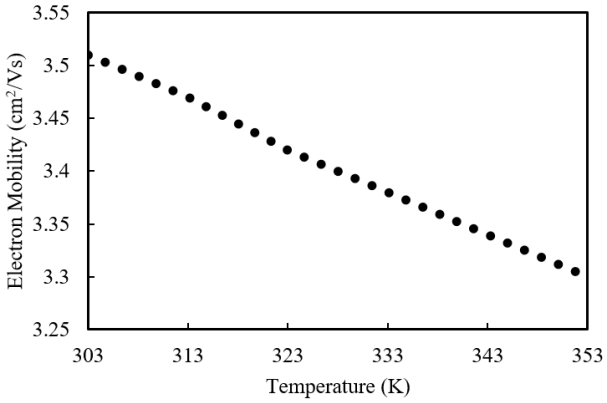

Fig. 5 (b)

Fig. 5 Relationship between electron mobility and temperature (a) V_{DS} = 0 V (b) V_{DS} = 1 V

The electron mobility has attained with the electric field magnitude on middle of channel in fig. 5. This result found the mobility on V_{DS} = 1 V was lower than mobility on V_{DS} = 0 V because the influence of positive charge from top of the gate biasing to control the channel and increased the electric field magnitude value.

F. Saturation drain current and Electron mobility

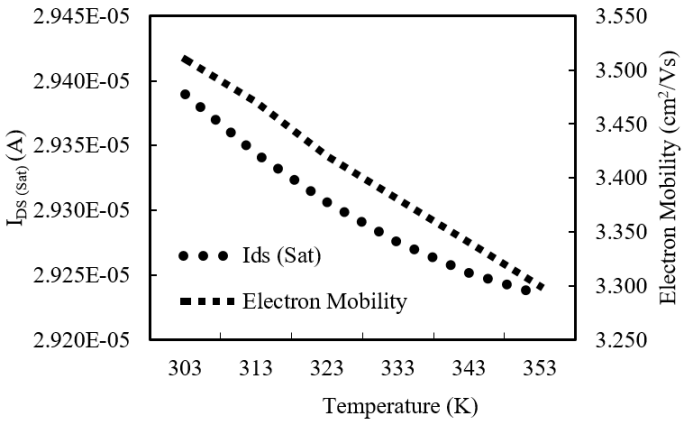

Fig. 6 Relationship between saturation drain current and Electron mobility on temperatures

From fig. 6 the temperature was controlling the electron mobility. On top of tri-gate FinFET channel at T = 303 K the mobility was higher (631 cm^2/Vs) at V_{DS} = 0.1 volt and lower (526 cm^2/Vs) at T = 353 K. After biased V_{DS} to 1 Volt giving the mobility higher (3.51 cm^2/Vs) at T = 303 K and lowest (3.30 cm^2/Vs) at T = 353 K.

This result shown the behavior of drain current and electron mobile that lowering with increasing of temperature because the decreasing of the drift velocity.

TABLE 1
RESULT SUMMARY

Temperature (K)	$I_{DS\ (Sat)}$ (μA)	Electron Mobility (cm^2/Vs)	
		V_{DS} = 0 V	V_{DS} = 1 V
303	29.40	631	3.51
313	29.30	607	3.47
323	29.30	584	3.42
333	29.30	563	3.38
343	29.30	544	3.34
353	29.20	526	3.30

From table 1, the trend of result has increasing of temperature inversely to saturation drain current and mobility. At V_{DS} = 0 V the mobility has decreased about 20 cm^2/Vs per 10K temperature variation and V_{DS} = 1 V mobility lowering about 0.4 cm^2/Vs. This effect takes the output of FinFET lowered and not appropriate to operate on high frequency.

ISBN: 978-988-14047-7-0
ISSN: 2078-0958 (Print); ISSN: 2078-0966 (Online)

V. Conclusion

The temperature is important attribute. It brings many effects to the device structure and operation as the lowering of I_{DS} and electron mobility. This paper shows the result of mobility on different temperature. While the temperature has increased the drain saturation current and mobility were decreased. The lowering of mobility on top of FinFET channel to bring the drain current down together because of the variation in electric field magnitude and drift velocity.

Acknowledgment

The Author gratefully thanks for software supported and experiment suggestion for Global TCAD Solution and faculty of engineering at King Mongkut's Institute of Technology Ladkrabang for research knowledge and research place.

References

[1] Jean-Pierre Colinge and team, *"Low-Temperature Electron Mobility in Trigate SOI MOSFETs", IEEE Electron Device Letters*, vol. 27, No. 2, pp. 120 – 122, Feb. 2006.

[2] Toshifumi Irisawa, *"Electron Mobility and Short-Channel Device Characteristics of SOI FinFETs with Uniaxially Strained (110) Channels,"* IEEE TRANSACTIONS ON ELECTRON DEVICES, vol. 56, No. 8, pp. 1651-1658, Aug. 2009.

[3] M. Zakir Hossain and Md. Alamgir Hossain, "*Electrical Characteristics of Trigate Finfet*", Global Journals of researches in Engineering Electrical and Electronics Engineering, vol. 11, pp. 8-10, Dec 2011.

[4] S.M. Sze and Kwog K. Ng., Physics of Semiconductor Devices, 3rd ed. New Jersey: John Wiley & Sons Inc., 2007, ch. 10.

[5] Nuttapong Patcharasardtra and Weera Pengchan, "*Electrical Characteristics of Different Gate Geometry of FinFET*", Key Engineering Materials, vol. 705, pp. 174-178. Aug. 2016.

Nuttapong Patcharasardtra received the B.S degree in computer engineering from Rajamangala University of Technology Lanna (RMUTL), Chiang Mai, Thailand, in 2015. Currently, he studying the M.S. degree in microelectronics engineering at King Mongkut's Institute of Technology Ladkrabang, Bangkok. His current interests include structure design, improve and technology of triple gate FinFET devices.

Weera Pengchan received the B.S. degree from Chiang Mai University, Chiang Mai, and the M/S/ and Ph.D. degree in electrical engineering from King Mongkut's Institute of Technology Ladkraband, Bangkok, Thailand.

He is instructor of microelectronics and electronics engineering at Department of electronics engineering at Department of electronics engineering, Faculty of engineering, King Mongkut's Institute of Techology Ladkrabang. His research area include microelectronics devices and fabrication technology, sensors and device simulation.

ISBN: 978-988-14047-7-0
ISSN: 2078-0958 (Print); ISSN: 2078-0966 (Online)