Real-Time Implementation of a Novel Asymmetrical Multilevel Inverter with Reduced Number of Switches

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***Abstract*—Numerous topologies of the multilevel inverter (MLI) are reported in the literature to reduce the number of switches for getting higher levels of output. This paper puts forward a novel asymmetrical MLI topology, in which the number of switches is reduced, compared to other topologies of MLI. Here, the performance of 9-level inverter is analysed using two types of the level shifted sinusoidal pulse width modulation techniques (SPWM) named alternate phase opposition disposition (APOD) SPWM and carrier overlapping (CO) SPWM. The performance analysis of the MLI is done using MATLAB/Simulink platform. Further, real-time implementation of the same has been carried out using Typhoon HIL 402 emulator. The comparative study of variations in total harmonic distortion (THD) of the output voltage and current of 9-level MLI under various conditions is presented in this paper to validate the proposed topology.**

***Index Terms*—Multilevel inverter (MLI), Sinusoidal pulse width modulation (SPWM), Alternate phase opposition disposition (APOD) SPWM, Carrier overlapping (CO) SPWM, Total harmonic distorion (THD).**

I. Introduction

Inverters play a vital role in power electronics for flexible power system and different drives purpose. Based on their structure and output inverters are classified into different types. Inverters having two levels in the output are called as two-level inverters and those having more than two levels in the output are called as MLI. The main drawback of the two-level inverters are harmonics present in the output. If AC drives are fed using two-level inverters, the fundamental value is responsible for producing useful power and harmonic components produce unnecessary heat and vibrations. These things degrade the performance of AC drives and require the regular maintenance. For reducing THD at the output side of inverter, filters can be used. The filters designed for removing lower order harmonics are bulky in size, thereby increasing the overall cost [1].

As a remedy to these issues, MLIs are introduced in the literature. MLIs are broadly classified into two categories based on construction and voltage sources rating. Diode clamped, flying capacitor and cascaded MLI is the example of construction based MLIs [2]. Symmetrical and asymmetrical MLIs are classified based on voltage sources rating [3]. Diode clamped, flying capacitor and cascaded H-bridge are the basic MLI, but they are complex in design and uses a number of switches. This will increase the size of the overall inverter, power loss, and switching complexity [4] [5]. Hence, reducing number of switches in MLIs became a novel research area for the researchers. A various number of researchers have been proposed different topologies of MLI with a reduced number of switches [6]-[8].

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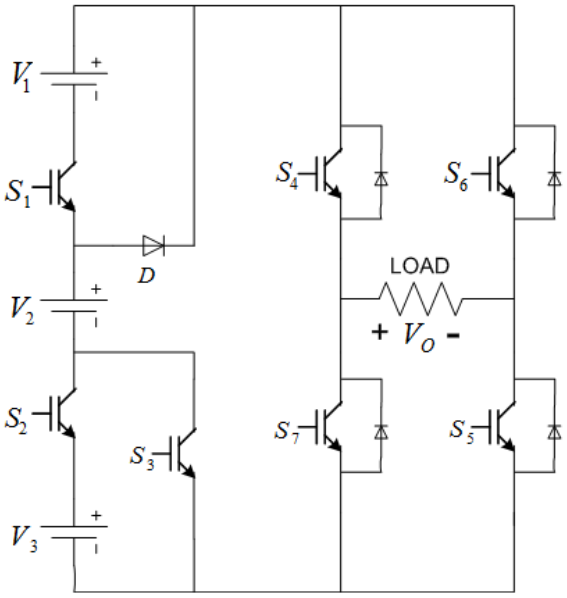

Fig. 1: Circuit diagram of proposed multilevel inverter

Gate pulses, which controls the switches of MLI to produce different levels of voltage can be generated by using different methods. Out of all the methods, SPWM is the most common technique, which removes the lower order harmonics for some extant [9]. In SPWM, the sinusoidal signal (modulating signal) is compared with high-frequency carrier signals and produces pulses, which can be used as gate pulses. This pulses can be used directly or after passing through the logic operators to achieve the desired levels in the output. SPWM, further categorized into different types based on the alignment and magnitude of carrier signals. Here two types of SPWM techniques are used to analyse the performance of a novel asymmetrical MLI, which is proposed using less number of switches. APOD SPWM is one of the techniques in which alternative carrier signals are used with phase opposition. The other technique used is CO SPWM in which carrier signals overlap with their neighbourhood carrier signals to some extent [10]. The above

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TABLE I: Switching states for various modes of operation

Mode	S_1	S_2	S_3	S_4	S_5	S_6	S_7	Output Voltage
Mode - 1	0	0	0	X	X	X	X	0
Mode - 2	0	0	1	1	1	0	0	$V_2 = V_{dc}$
Mode - 3	1	0	1	1	1	0	0	$V_1 + V_2 = 2V_{dc}$
Mode - 4	0	1	0	1	1	0	0	$V_2 + V_3 = 3V_{dc}$
Mode - 5	1	1	0	1	1	0	0	$V_1 + V_2 + V_3 = 4V_{dc}$
Mode - 6	0	0	1	0	0	1	1	$-V_2 = -V_{dc}$
Mode - 7	1	0	1	0	0	1	1	$-(V_1 + V_2) = -2V_{dc}$
Mode - 8	0	1	0	0	0	1	1	$-(V_2 + V_3) = -3V_{dc}$
Mode - 9	1	1	0	0	0	1	1	$-(V_1 + V_2 + V_3) = -4V_{dc}$

mentioned techniques are simulated in MATLAB/Simulink environment and further the real-time implementation is done using Typhoon HIL 402 emulator.

The content structure of the paper is as follows. Section II shows the circuit diagram, switching states, and gate pulses generation for proposed MLI using SPWM. Section III exhibits the simulation, emulation results and THD comparisons under various conditions (R, RL load, and changing modulation index). The conclusion follows in the last section of this paper.

II. Multilevel Inverter

A. Proposed Topology

The circuit diagram of the proposed asymmetrical MLI is shown in Fig.1. This topology is using three voltage sources (V_1 - V_3) and seven switches (S_1 - S_7) of different ratings for getting 9-level output voltage. For getting desired voltage levels, the author has taken the same values of sources V_1, V_2 and source V_3 having double the magnitude of V_1. Since this inverter is using voltage sources of various ratings, is called as asymmetrical MLI.

The switches S_1, S_2, and S_3 are responsible for producing positive levels of voltages, these switches operate at high frequency. Switches S_4, S_5, S_6, and S_7 combinedly form an H-bridge topology, which is responsible for the reversal of polarity and operates at the output frequency. The switching states for obtaining different levels of output voltage are shown in TABLE I.

TABLE II: Comparison between number of switches used in various inverter topologies

Output Voltage levels	Cascaded H-bridge	Ref.[7]	Ref.[8]	Proposed Topology
9-level	16	12	9	7
13-level	24	16	11	9
17-level	32	20	13	11
21-level	40	24	15	13

Considering $V_1 = V_2 = V_{dc}$ and $V_3 = 2V_{dc}$, the output voltages from mode-1 to mode-9 are as given in TABLE I. The 9-level output voltage is obtained by using 3 sources, 7 switches, and a diode(D). The same topology further extended for higher levels in output, such as the the 11-level output can be obtained by using 4 sources, 8 switches, and 2 diodes. The proposed MLI is giving higher levels of output voltage using less number of switches, compared to the topologies presented in ref.[7], ref.[8], and cascaded H-bridge, which is shown in TABLE II. The graphical analysis of the same is shown in Fig.2.

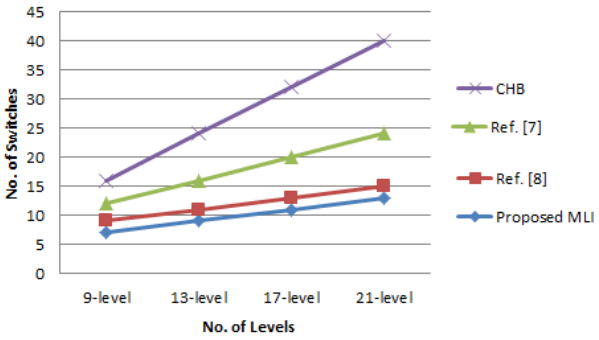

Fig. 2: Comparison between number of switches used in various inverter topologies

B. Generation of Gate Pulses

As mentioned in the section I, SPWM techniques are used for generating gate pulses.Fig. 3 is showing the diagram of control block generating gate pulses for switches of proposed MLI using SPWM techniques. Sinusoidal source shown in

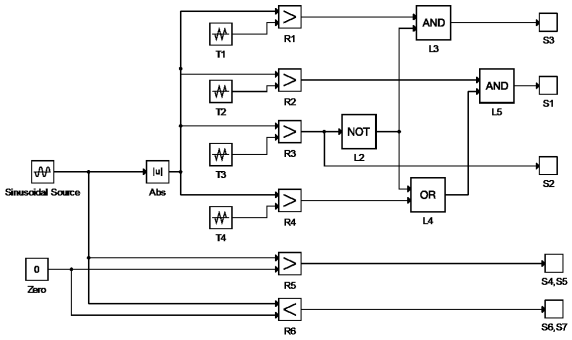

Fig. 3: Control block generating gate pulses using SPWM technique

the figure is the modulating signal, T1 - T4 represents carrier (high frequency) signals. R1 - R6 and L2 - L5 are the relational operators and logical operators respectively.

Here, author is analysing the performance of proposed MLI using two types of SPWM techniques, these are APOD

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SPWM and CO SPWM. These two techniques differ from each other based on the alignment and magnitude of carrier signals used, this is shown in Fig. 4 and Fig. 5.

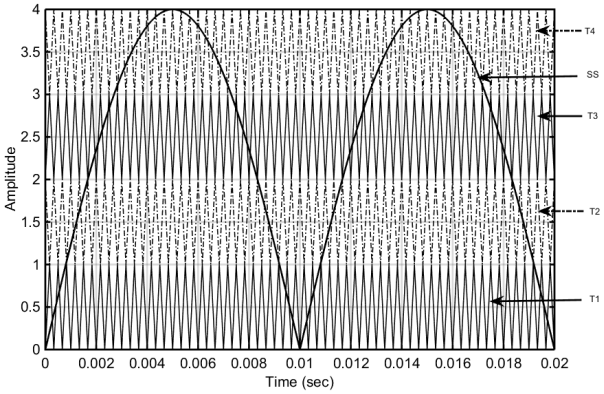


Fig. 4: Carrier signal alignment in APOD SPWM

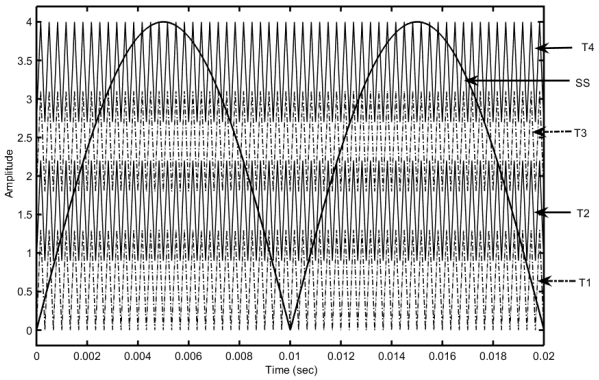


Fig. 5: Carrier signal alignment in CO SPWM

III. Simulation and Emulation Results

In this section, the analysis of the Proposed MLI is carried out using MATLAB/Simulink and Typhoon HIL emulator. Typhoon HIL works based on hardware in the loop (HIL) technique and used in the development and testing of complex real-time embedded systems. The results of the Typhoon HIL are taken from digital storage oscilloscope (DSO) using HIL 402 device.

The performance of proposed MLI is tested for R and RL loads. Further analysis is carried out using APOD and CO SPWM techniques and also by varying the modulation index(m_a). Here, 50Ω resistance, 10mH inductance, voltage sources of 75V each for V_1, V_2 and 150V for V_3 have been considered for analysis purpose.The frequency of the modulating signal is considered as 50Hz, carrier signals frequency is taken as 3kHZ.

HIL results of the output voltage and current for R load using APOD SPWM technique with m_a of 1 are shown in Fig. 6. These results are obtained from DSO in which channel one (CH1) is showing the output voltage and channel two (CH2) is showing load current. The horizontal axis of both channels is showing 10ms/div. The vertical axes of CH1 and CH2 are showing 200V/div and 5A/div respectively.

Fig. 7 is showing the fast Fourier transform (FFT) analysis of the above results. It observed from the results that the THD value is 6% in both voltage and current.

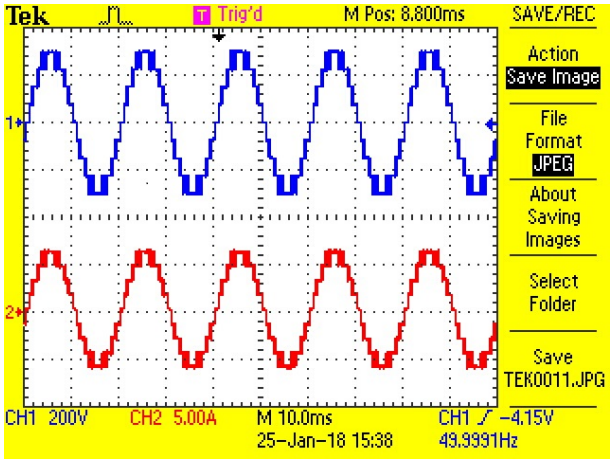
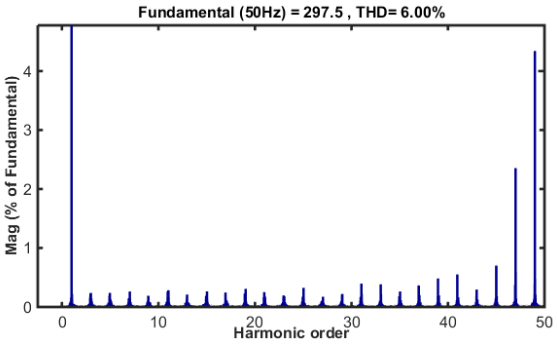
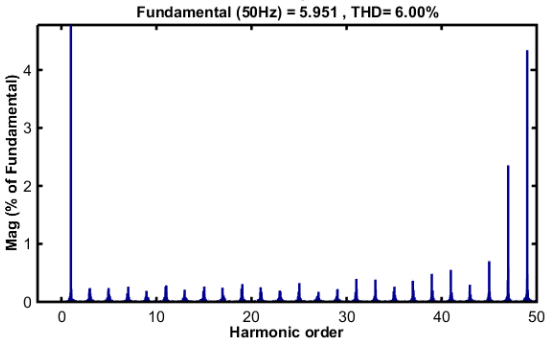


Fig. 6: HIL results of output voltage and current for R load and m_a = 1



(a) Voltage



(b) Current

Fig. 7: FFT analysis for R load and m_a = 1

Fig. 8 is showing the HIL results of the MLI for RL load, using APOD SPWM and with m_a of 1. FFT analysis of the output voltage and current, in this case, are shown in Fig. 9. From the FFT analysis, it is observed that the THD in output voltage and current are 6.14% and 2.29% respectively.

HIL results of the MLI for RL load, using APOD SPWM and with m_a of 0.8 are shown in the Fig. 10. Fig. 11 is showing the FFT analysis results of the output voltage and current in this case. From the FFT analysis, it is observed that the THD in output voltage and current are 4.46% and 2.38%.

Fig. 12 is showing the HIL results of the MLI for RL load, using APOD SPWM and with m_a of 1.2. FFT analysis results of the output voltage and current, in this case, are shown in Fig. 13. From the FFT analysis, it is observed that

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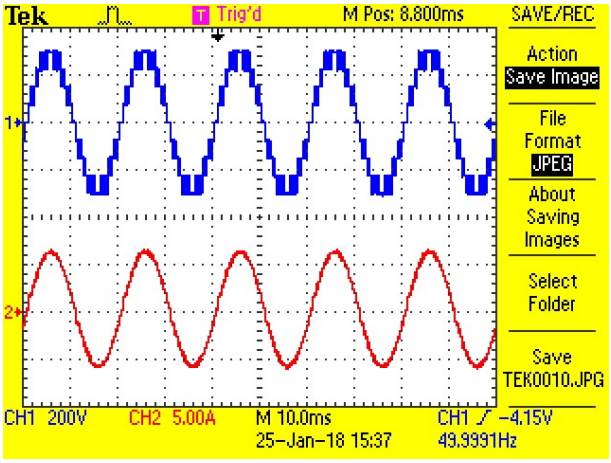


Fig. 8: HIL results of output voltage and current for RL load and m_a = 1

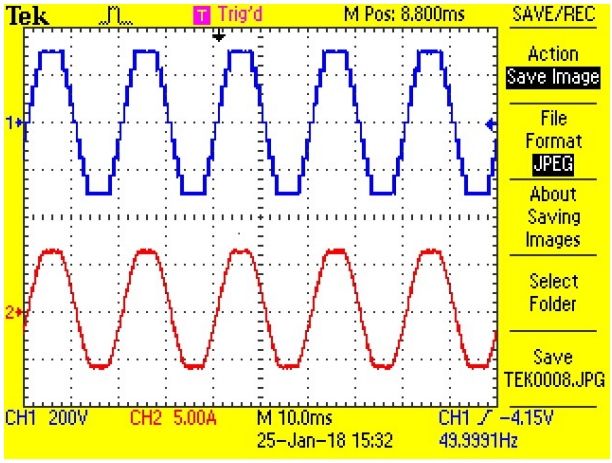
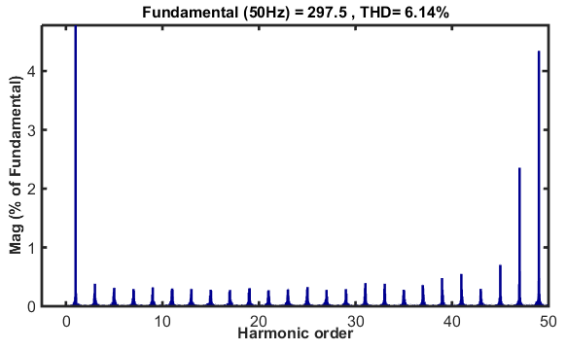
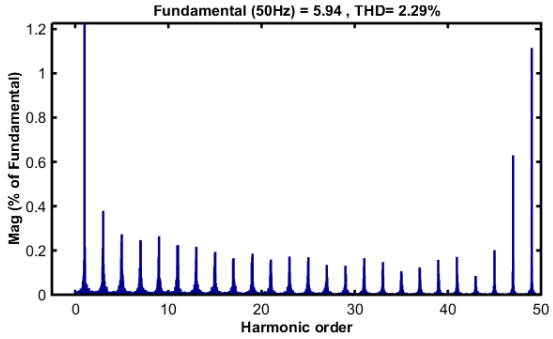


Fig. 10: HIL results of output voltage and current for RL load and m_a = 0.8

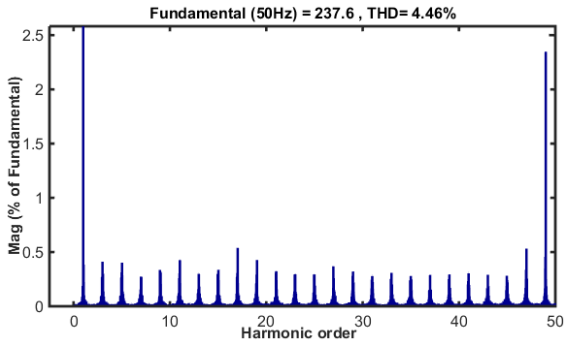


(a) Voltage

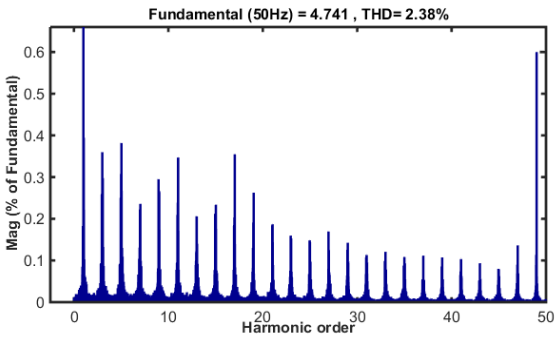


(b) Current

Fig. 9: FFT analysis for RL load and m_a = 1



(a) Voltage



(b) Current

Fig. 11: FFT analysis for RL load and m_a = 0.8

the THD in output voltage and current are 9.24% and 7.39%.

The THD and fundamental root mean square (RMS) values of the output voltage and current of the proposed MLI under various conditions are computed and shown in TABLE III and TABLE IV. TABLE III shows the results of APOD SPWM technique, under R and RL loads for different values of modulation index. The results of CO SPWM technique, under R and RL loads for different values of modulation index are shown in TABLE IV.

IV. Conclusion

A novel asymmetrical MLI topology with a reduced number of power switches has been proposed. The proposed MLI has been implemented in MATLAB/Simulink and Typhoon HIL emulator for 9-level output. Performance of this MLI has been analysed using APOD and CO SPWM techniques. Study of MLI has carried out under R and RL loads with different values of the modulation index(m_a). The value of THD in output voltage and current has been computed and compared under various conditions. It has been observed that APOD SPWM is producing output quantities with less THD as compared to CO SPWM. It was observed from the results that lesser harmonics were observed during under modulation. On the same time fundamental component of the output is decreasing. As per the requirment of the application proper values of m_a has to be chosen. The proposed topology can be used in solar plant, FACTS and UPS applications.

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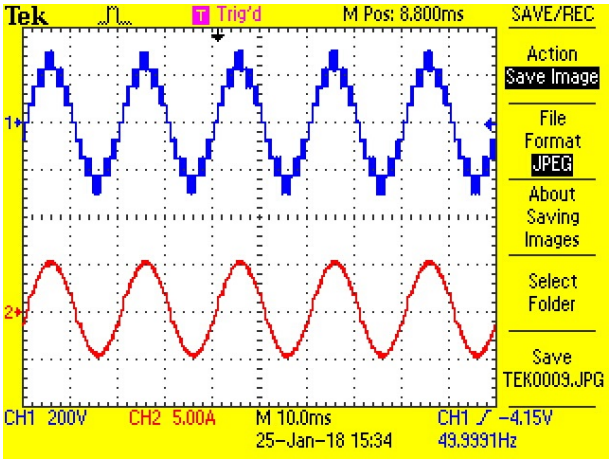
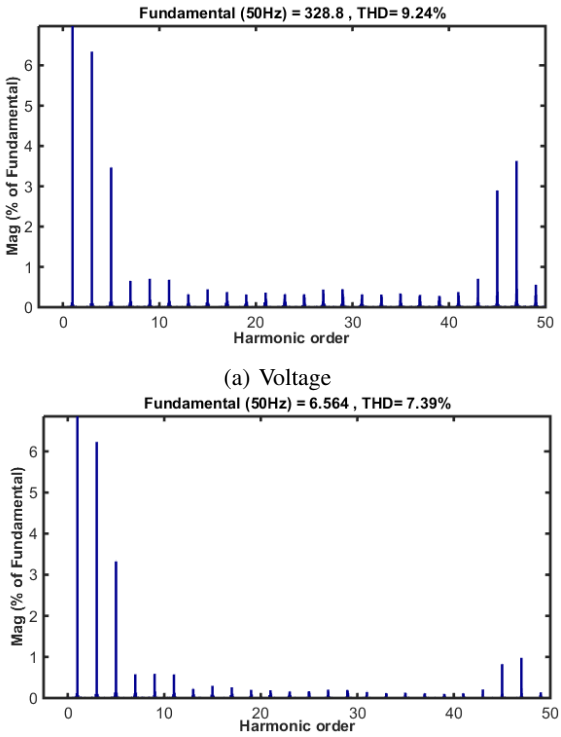


Fig. 12: HIL results of output voltage and current for RL load and m_a = 1.2



(a) Voltage

(b) Current

Fig. 13: FFT analysis for RL load and m_a = 1.2

TABLE III: THD(%) analysis of output voltage and current of MLI under different conditions using APOD SPWM

m_a	Load	V_{rms} (V)	THD V_0	I_{rms} (A)	THD I_0
0.80	R	168.0	4.24	3.36	4.24
0.80	RL	168	4.46	3.35	2.38
0.85	R	178.7	4.74	3.57	4.74
0.85	RL	178.7	4.93	3.56	2.32
0.90	R	189.2	5.30	3.78	5.30
0.90	RL	189.2	5.47	3.77	2.34
0.95	R	199.8	5.76	4.00	5.76
0.95	RL	199.8	5.91	3.99	2.36
1.00	R	210.4	6.00	4.21	6.00
1.00	RL	210.4	6.14	4.20	2.29
1.10	R	224.0	7.04	4.48	7.04
1.10	RL	224.0	7.16	4.47	4.15
1.20	R	232.5	9.13	4.65	9.13
1.20	RL	232.5	9.24	4.64	7.39

TABLE IV: THD(%) analysis of output voltage and current of MLI under different conditions using CO SPWM

m_a	Load	V_{rms} (V)	THD V_0	I_{rms} (A)	THD I_0
0.80	R	177.1	7.98	3.54	7.98
0.80	RL	177.1	8.04	3.53	7.15
0.85	R	188.4	7.23	3.77	7.23
0.85	RL	188.3	7.29	3.76	6.36
0.90	R	198.3	6.62	3.97	6.62
0.90	RL	198.3	6.68	3.96	5.75
0.95	R	207.4	6.14	4.15	6.14
0.95	RL	207.4	6.21	4.14	5.32
1.00	R	216.1	5.92	4.32	5.92
1.00	RL	216.1	5.99	4.31	5.12
1.10	R	227.8	7.26	4.55	7.26
1.10	RL	227.8	7.33	4.55	6.65
1.20	R	235.3	9.86	4.71	9.86
1.20	RL	235.3	9.91	4.70	9.32

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