A Dual-Clamped-Voltage Coupled-Inductor Switched-Capacitor Step-Up DC-DC Converter

Yuen-Haw Chang and Dian-Lin Ou

Abstract—A closed-loop high-gain dual-clamped-voltage coupled-inductor switched-capacitor (DCISC) converter is proposed by combining a pulse-width-modulation-based (PWM-based) compensator and a non-overlapping circuit for step-up DC-DC conversion and regulation. The power part contains two subcircuits: (i) a dual-clamped-voltage coupled-inductor (DCI) booster and (ii) a three-stage switched-capacitor (SC) doubler, in cascade connection between source $V_s$ and output $V_o$. With the help of two clamping capacitors and a coupled inductor with the turn ratio $n$, this DCI booster can provide the voltage of $(n+1)/V_s$ theoretically, where $D$ means the duty cycle of the MOSFET. And then by using the SC doubler, the overall step-up gain can reach to $3(n+1)/[(2-D)/(1-D)]$ at most. Practically, this DCISC can boost the voltage gain up to 41.94 when $D=0.61$, $n=3$. Further, the PWM technique is adopted not only to enhance the output regulation for the compensation of the dynamic error between the practical and desired outputs, but also to reinforce output robustness against source or loading variation. Finally, the closed-loop DCISC is designed by OrCAD SPICE and simulated for some cases: steady-state and dynamic responses. All results are illustrated to show the efficacy of the proposed scheme.

Index Terms—high-gain, dual-clamped-voltage coupled-inductor, switched-capacitor, pulse-width-modulation, step-up converter.

I. INTRODUCTION

Nowadays, step-up DC-DC converters have attracted great attention. Voltage boosting is widely used in many applications, such as renewable energy system, electronic equipment, electric vehicles, etc. In general, these power converters are always required for a high efficacy, a light weight, a small volume, and a better regulation capability.

The switched-capacitor converter (SCC), possessed of the charge pump structure, is one of solutions to DC-DC power conversion because it has only semiconductor switches and capacitors. Unlike conventional converters, the inductor-less SCC has small volume and light weight. Until now, many types have been suggested [1], [2], and some well-known topologies are presented, e.g. Dickson charge pump, Ioinovici SC. In 1976, Dickson charge pump was proposed with a two-phase diode-capacitor chain [3], [4], but it has obvious defects of fixed gain and large device area. In the 1990s, Ioinovici proposed a SCC with two symmetrical capacitor cells, and presented a current-mode control [12]. In 1998, Mak and Ioinovici proposed a high-power-density SC inverter [8]. In 2009, Tan et al. proposed the modeling and design of SCC by variable structure control [9]. In 2011, Chang proposed an integrated step-up/down SCC (SCVM/SCVD) [10]. In 2013, Chang proposed a gain/efficiency-improved serial-parallel switched-capacitor converter (SPSCC) by combining an adaptive-conversion-ratio (ACR) and pulse-width-modulation (PWM) control [11]. In 2016, Chang proposed a switch-utilization-improved switched-inductor switched-capacitor converter with adapting stage number (SISCC) is proposed by phase generator and PWM control [12].

In order to increase the voltage gain, it is one of the good ways to utilize the device of coupled-inductor. However, the stress on transistors and the volume of magnetic device must be considered. In 2011, Berkovich et al. proposed a switched-coupled inductor cell for DC-DC converter with very large conversion ratio [13]. In 2015, Chen et al. proposed a novel switched-coupled-inductor DC-DC step-up converter via adopting a coupled inductor to charge a switched capacitor for making voltage gain effectively increased [14]. In 2016, Chang et al. proposed a closed-loop high-gain switched-coupled-inductor switched-capacitor converter for step-up DC-DC conversion and regulation [15]. Here, we try to combine a dual-clamped-voltage coupled-inductor booster with three-stage SC doubler to propose a closed-loop DCISC converter for the realization of high-gain conversion as well as enhancement of regulation capability.

II. CONFIGURATION OF DCISC

Fig. 1 shows the overall circuit configuration of dual-clamped-voltage coupled-inductor switched-capacitor (DCISC) converter, and it contains two major parts: power part and control part for achieving the high-gain step-up DC-DC conversion and closed-loop regulation.

A. Power part

The power part of DCISC is shown in the upper half of Fig. 1, and it consists of two subcircuits: a dual-clamped-voltage coupled-inductor booster and three-stage SC doubler, connected in cascade between source $V_s$ and output $V_o$. This converter contains one coupled inductor ($L_1$, $L_2$) with the turn ratio $n$ ($n=N_2/N_1$), four power switches ($S_1$, $S_2$, $S_3$, $S_4$), two clamping capacitors ($C_1$, $C_2$), three pumping capacitors ($C_3$, $C_4$, $C_5$), one output capacitor ($C_o$) and nine diodes ($D_1$, $D_2$, $D_3$), where each capacitor of SC doubler has the same capacitance $C$ ($C_j=C_s=C_o$). Fig. 2 shows the theoretical waveforms of DCISC in one switching cycle $T_S$ ($T_p=1/f_p$, $f_p$: switching frequency). Basically, the operation of the DCISC converter contains two phases: Phase I and II, with the different phase periods of $DT_2$ and $(1-D)T_2$, respectively. The operations for Phase I and II are described as follows.

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Yuen-Haw Chang and Dian-Lin Ou are with the Department and Graduate Institute of Computer Science and Information Engineering, Chaoyang University of Technology, Taichung, Taiwan, R.O.C. Post code: 413. (e-mail: yhchang@cvut.edu.tw, s10527607@gm.cvut.edu.tw).
The voltage 

The corresponding topological path is shown in Fig. 3(a). It is obvious that the source \( V_3 \) energy is transferred to the primary and secondary windings of the coupled inductor, and then capacitor \( C_1 \) receives energy from the input source and secondary winding. The voltage \( V_{C1} \) across \( C_1 \) is getting up to \((n+1) \cdot V_c\). At the same time, \( C_2 \) receives energy from the secondary winding, and the voltage \( V_{C2} \) across \( C_2 \) is reaching towards \( n \cdot V_c \). Meanwhile, the capacitors \( C_3, C_4 \) and \( C_5 \) are discharged in series via \( S_3 \) and \( S_4 \) to transfer the energy into output capacitor \( C_o \) and load \( R_L \).

(ii) **Phase II**

During the period of phase II, \( S_2 \) is turned ON, and \( S_1, S_3 \) and \( S_4 \) are turned OFF. Thus, \( D_1, D_2 \) and \( D_3 \) are ON, and \( D_4-D_6 \) are OFF. The topological path is shown in Fig. 3(b). It is seen that the capacitors \( C_1, C_4 \) and \( C_5 \) are charged in parallel by the series voltages of inductors \( L_1, L_2 \), capacitors \( C_1, C_2 \) and \( V_p \). Simultaneously, output capacitor \( C_o \) stands alone to supply energy to load \( R_L \).

According to the theory of the booster, the steady-state voltage \( V_{L2} \) across \( L_1 \) is going towards the value of 

\[ DV_o/(1-D) \]

via the operation of duty cycle \( D \), and thus the voltage \( V_{L2} \) across \( L_2 \) in the secondary side is approaching the value of 

\[ nDV_o/(1-D) \]

Based on the current path as in Fig. 3(b), the capacitors \( C_3, C_4 \) and \( C_5 \) can be charged in parallel by using the series total voltage of \( V_{S}, V_{L1}, V_{C1}, V_{L2} \) and \( V_{C2} \) (i.e. \( V_3+V_{L1}+V_{C1}+V_{L2}+V_{C2} \)). Hence, the overall step-up voltage gain can reach the value of 

\[ 3(n+1)[(2-D)/(1-D)] \]

The control part of DCISC is shown in the lower half of Fig. 1. It is composed of a non-overlapping circuit and a pulse-width-modulation (PWM) block. From the controller signal flow, the feedback signal \( V_o \) is sent into the OP-amp low-pass filter (LPF) for high-frequency noise rejection. The filtered signal \( V_o \) is compared with a ramp function \( V_{ref} \) to produce the signal \( P_3 \) via the PWM block. Next, an adjustable voltage \( V_{rp} \) is compared with a ramp function \( V_{rp} \) to generate a non-symmetrical clock signal. And then, this clock is sent to the non-overlapping circuit for producing a set of non-overlapping phase signals \( \Phi_1, \Phi_2 \) for the driver signals of \( S_1, S_2 \). Also, the driver signals of \( S_3 \)
and $S_j$ can be obtained with the help of the synchronous operation with $\Phi_j$ and $P_j$ via AND logic gate, just like the waveform of Fig. 2.

The main goal of this control part is to generate the driver signals of these MOSFETs for the different topologies as in Fig. 3(a) and (b), and to keep $V_o$ on following the different desired $V_{ref}$ via the PWM-based compensator for the better closed-loop regulation capability.

### III. EXAMPLES OF DCISC

In this section, based on Fig. 1, this closed-loop converter is designed and simulated by SPICE tool. The results are illustrated to verify the efficacy of the proposed converter. The component parameters of the proposed converter are listed in Table I. This converter is preparing to supply the standard load $R_L=5k\Omega$. For checking closed-loop performances, some topics will be simulated and discussed, including: (i) Steady-state responses, (ii) Dynamic responses.

#### (i) Steady-state responses

The closed-loop DCISC is simulated for $V_{ref}=504V/490V/480V$ respectively, and then these output results are obtained as shown in Fig.4(a)-(b) / Fig. 4(c)-(d) / Fig. 4(e)-(f). In Fig. 4(a), it can be found that the settling time is about 5ms, and the steady-state value of $V_o$ is really reaching 503.33V, and this converter is stable to keep $V_o$ following $V_{ref}(504V)$. In Fig. 4(b), the output ripple percentage is measured as $rp = \Delta V_o/V_o = 0.05\%$, and the power efficiency is obtained as $\eta = 91.7\%$. In Fig. 4(c), the settling time is about 10ms, and the steady-state value of $V_o$ is really reaching 490.27V. In Fig. 4(d), the output ripple percentage is measured as $rp = \Delta V_o/V_o = 0.101\%$, and the power efficiency is obtained as $\eta = 89.5\%$. In Fig. 4(e), the settling time is about 15ms, and the steady-state value of $V_o$ is really reaching 481.02V. In Fig. 4(f), the output ripple percentage is measured as $rp = \Delta V_o/V_o = 0.15\%$, and the power efficiency is obtained as $\eta = 87.9\%$. In Fig. 4(g), the settling time is about 20ms, and the steady-state value of $V_o$ is really reaching 478.22V.

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#### Table I. Component parameters of DCISC.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply source ($V_S$)</td>
<td>12V</td>
</tr>
<tr>
<td>Clamping capacitor ($C_1,C_2$)</td>
<td>50µF</td>
</tr>
<tr>
<td>Pumping capacitor ($C_3,C_4,C_5$)</td>
<td>10µF</td>
</tr>
<tr>
<td>Output capacitor ($C_o$)</td>
<td>20µF</td>
</tr>
<tr>
<td>Inductor ($L_1,L_2$)</td>
<td>$L_1=100\mu\text{H}, L_2=900\mu\text{H} (n=3)$</td>
</tr>
<tr>
<td>Switching frequency ($f_s$)</td>
<td>20kHz</td>
</tr>
<tr>
<td>Diodes : $D_1$-$D_9$</td>
<td>D1N5820</td>
</tr>
<tr>
<td>On-state resistance of MOSFETs ($R_{on}$)</td>
<td>50µΩ</td>
</tr>
<tr>
<td>Load resistor ($R_L$)</td>
<td>5kΩ</td>
</tr>
</tbody>
</table>
as \( r_p = \Delta V_o / V_o = 0.253\% \), and the power efficiency is obtained as \( \eta = 88.1\% \). These results show that the closed-loop DCISC converter has a high voltage gain and a good steady-state performance.

(ii) Dynamic responses:

Since the voltage of battery is getting low as the battery is working long time, or the bad quality of battery results in the impurity of source voltage, such a dynamic variation should be considered as well as loading variation and reference variation.

(a) Case I: (loading variation)

Assume that \( R_L \) is 5k\( \Omega \) normally, and it changes from 5k\( \Omega \) to 2.5k\( \Omega \). After a short period of 400ms, the load recovers from 2.5k\( \Omega \) to 5k\( \Omega \), i.e. \( R_L = 5k\Omega \rightarrow 2.5k\Omega \rightarrow 5k\Omega \) as in Fig. 5(a).

Fig.5(b) shows the transient waveform of \( V_o \) during the duration of loading variations. It is found that \( V_o \) has a small drop (2.8V) at 300ms ~ 700ms (double loading). The curve shape becomes thicker during the period of the heavier load, i.e. the output ripple becomes bigger at this moment. Even though the double loading happens, it can be found that \( V_o \) still follows \( V_{ref} \) (504V).

(b) Case II: (reference variation)

Assume that \( V_{ref} \) is 504V normally, and it suddenly changes from 504V to 480V. After a short period of 400ms, the \( V_{ref} \) recovers from 480V to 504V, i.e. \( V_{ref} = 504V \rightarrow 480V \rightarrow 504V \) as in Fig. 5(c). The waveform of \( V_o \) is obtained in the Fig. 5(d). It is found that \( V_o \) is still following \( V_{ref} \) via the closed-loop compensation, even though \( V_{ref} \) has a voltage drop of about 24V.

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![Diagram](image-url)
Fig. 5. Dynamic responses of DCISC.
(a) $R_L = 5k\Omega \rightarrow 2.5k\Omega \rightarrow 5k\Omega$, (b) $V_o$ (Case I); (c) $V_{ref} = 504V \rightarrow 480V \rightarrow 504V$, (d) $V_o$ (Case II); (e) $V_S = 11 + \sin(2\pi \times 1000t)$ V, (f) $V_o$ (Case III).

(c) Case III : (source variation)
Assume that $V_S$ is normally at DC 12V, and suddenly turns into DC 11V plus a sinusoidal disturbance, i.e. $11 + \sin(2\pi \times 1000t)$ as in the Fig. 5(e). Fig. 5(f) shows the waveform of $V_o$ ($V_{ref} = 490V$). Clearly, via the closed-loop control, $V_o$ is still keeping on $V_{ref}$ in spite of source disturbance.

IV. CONCLUSIONS
A closed-loop high-gain DCISC converter is proposed by combining the PWM-based compensator and the non-overlapping circuit for step-up DC-DC conversion and regulation. (DCISC : $V_S \rightarrow V_o : 3(\alpha+1)\cdot\frac{2-D}{1-D}\cdot V_S$).
Finally, the closed-loop DCISC converter is designed and simulated by SPICE for some cases: steady-state and dynamic responses. The advantages of the proposed scheme are listed as follows. (i) In the DCISC, the large conversion ratio can be achieved with four switches, five capacitors, and one coupled inductor for a step-up gain of 41.94 or above. (ii) As for the higher step-up gain, it can easily be realized through increasing the turn ratio or extending the number of pumping capacitors. (iii) The PWM technique is adopted not only to enhance output regulation capability for the different desired output, but also to reinforce the output robustness against loading/reference/source variation. At present, the prototype circuit of the proposed converter is implemented in the laboratory as shown in the photo in Fig. 6. Some experimental results will be obtained and measured for the verification of the proposed converter.
Fig. 6. Prototype circuit of DCISC.

REFERENCES


