A Simple Greinacher-Doubler-Based Switched-Coupled-Inductor Boost DC-AC Inverter

Yuen-Haw Chang and Yu-Ming Lu

***Abstract*—This paper presents a simple configuration of Greinacher-doubler-based switched-coupled-inductor inverter (GSCII) by combining a non-overlapping phase generator and a sinusoidal pulse-width-modulation (SPWM) controller in order to realize boost DC-AC conversion and closed-loop regulation. The power part is composed of two sub-circuits between supply V_S and output V_O, including: (i) a Greinacher-doubler-based switched-copuled-inductor booster (one coupled inductor, four capacitors, and one switch regulated by the phase generator), and (ii) a half-bridge DC-link inverter (one output capacitor, a load resistor, and two switches controlled by the SPWM controller) , so as to obtain the maximum range of AC output: $+[(n+1)/(1-D)]V_S \sim -[(n+1)/(1-D)]V_S$, where n is the turn ratio of the coupled inductor and D is duty cycle of charging this inductor. When n=2 and D=0.5, the DC-AC conversion from DC 24V to AC 100VRMS, 60Hz can practically be achieved. Furthermore, the SPWM is employed to enhance regulation capability for the different output amplitude and frequency, as well as robustness to source or loading variation. Finally, the closed-loop GSCII is designed and simulated by SPICE for some cases of steady-state and dynamic responses. All results are illustrated to show the efficacy of the proposed scheme.**

***Index Terms*—Greinacher-doubler-based switched-coupled-inductor inverter (GSCII), boost DC-AC conversion, closed-loop regulation, sinusoidal pulse-width-modulation (SPWM).**

I. Introduction

In recent years, the boost power converters for DC-DC or DC-AC are widely applied when a circuit or module has just a low-voltage supply source available, such as lighting system, smart phone, and medical equipment, etc. They are always asked for some good features, including small volume, light weight, high efficiency, and robust regulation capability. Generally, the conventional converters have a large volume and a heavy weight due to magnetic devices used. Therefore, more manufactures and researchers pay attention to this topic, and ultimately aiming for step-up converters realized on a compact chip by mixed-mode VLSI technology.

This sort of switched-capacitor (SC) power converters, consisting of capacitors and MOSFET switches, is one of the good solutions to produce a high voltage gain for the boost DC-DC/DC-AC conversion without magnetic device. Up to now, the various SC types have been suggested. In 1976, Dickson charge pumping was proposed based on a chain structure of diodes and capacitors [1]. In 1990s, Ioinovici *et al*. proposed many SC schemes with two capacitor cells working in anti-phase by voltage/current mode [2-3]. In 2007, Chang proposed a CPLD-based implementation of SC step-down DC-DC converter for multiple output choices [4]. In 2011-2014 Chang *et al*. proposed a series of multistage/ multiphase SC step-up/down DC-DC converter or DC-AC inverter with sinusoidal PFM [5-9]. In 2015, Chang *et al*. proposed a closed-loop switched-capacitor-inductor-based boost DC-AC inverter [10].

For a higher voltage gain, it is one of the good ways to take advantage of turn ratio and/or extra winding stage of coupled inductor. However, the stress on transistors and the volume of magnetic device must be considered. In 2015, Chen *et al*. proposed a high-gain and input-current-ripple-free boost integrated flyback converter including coupled inductor [11]. Bahrami *et al*. suggested a modified step-up boost converter with coupled-inductor and super-lift techniques [12]. Chen *et al*. proposed a novel switched-coupled-inductor (SCI) DC-DC step-up converter and its derivatives [13]. Wu *et al*. proposed a non-isolated high step-up DC-DC converter via adopting SC cell [14]. Nouri *et al*. proposed an interleaved high-gain step-up DC-DC converter based on three-winding coupled-inductor and voltage-multiplier cell [15]. In 2016-2017, Chang *et al*. proposed a novel coupled-inductor switched-capacitor boost DC-AC inverter, and then plus a four-stage SC, presented a high-gain serial-parallel-switched-capacitor coupled-inductor inverter [16-17]. Going a further step, Chang *et al*. proposed a simple SCI boost DC-AC inverter for fewer device count [18]. In this paper, based on the consideration of circuit complexity, voltage gain, device count, the authors try to suggest a simple scheme of GSCII for boost DC-AC conversion and closed-loop regulation.

II. Configuration of GSCII

Fig. 1 shows the closed-loop scheme of Greinacher-doubler-based switched-coupled-inductor inverter (GSCII) proposed, and it contains two major parts: power and control parts for achieving the boost DC-AC conversion/regulation (DC 24V to AC 100VRMS, 60Hz). The details of the two parts are discussed as follows.

A. Power Part

The power part of this inverter as in the upper half of Fig. 1 contains two sub-circuits: (i) a Greinacher-doubler-based SCI booster and (ii) a half-bridge DC-link inverter, which are

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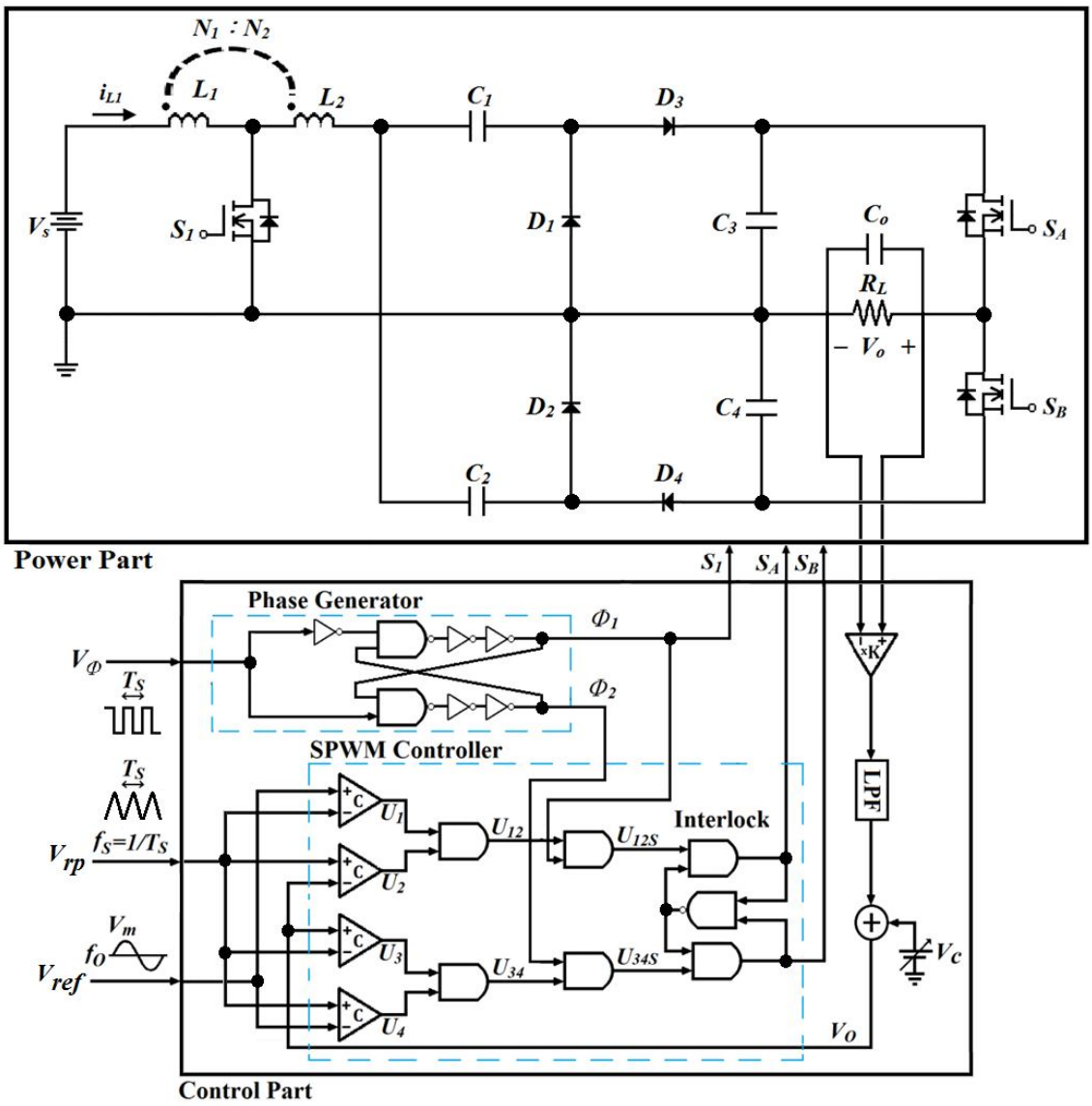

Fig. 1. Configuration of closed-loop GSCII.

in cascaded connection between supply V_S and output V_O. Firstly, the front-stage booster circuit is mainly in charge of step-up DC-DC conversion, including a MOSFET switch S_1, a coupled inductor L_1, L_2, four diodes D_1–D_4, four capacitors C_1–C_4, where the same capacitance C (C_1=C_2=C_3=C_4=C) is assumed. This coupled inductor (L_1 and L_2) is modeled as an ideal transformer with a turn ratio of n (n=N_2/N_1). The main function of this booster is to lift both of the capacitor voltages across C_3 and C_4 up to $[(n+1)/(1-D)]V_S$, where D ($0<D<1$) is the duty cycle of the driver signal of switch S_1, and DT_S is the period of charging this coupled inductor in one switching cycle T_S (T_S=1/f_S, f_S: switching frequency). Secondly, the rear stage: half-bridge DC-link circuit is mainly to handle DC-AC invertsion, and it includes two multual devices C_3,C_4 (as half-bridge capacitors), two switches S_A and S_B (for SPWM control), a filter capacitor C_O, and a load resistor R_L. Here, with the help of S_A, S_B, plus half-bridge voltages on C_3, C_4, the range of the AC output V_O can reach: $+[(n+1)/(1-D)]V_S$ ~ $-[(n+1)/(1-D)]V_S$. Fig. 2 shows the theoretical waveforms within an output cycle T_O (T_O=1/f_O, f_O: output frequency). Here, for the convenience of explanation, one T_O contains 11 (or above actually) switching cycle T_S. Each T_S has two phases: Phases I and II with the different periods DT_S and $(1-D)T_S$. The detailed operations are explained as follows.

1) Phase I:

During this time interval, turn ON S_1, turn SPWM-ON S_A, and turn OFF S_B. The relevant topology is shown in Fig. 3(a). The inductor L_1 is charged by supply V_S, and the energy is transferred from the primary winding of this coupled inductor to the secondary one for making the voltage as: V_{L1}=V_S, V_{L2}=nV_S. Then, the inductor L_2 in the secondary side is discharged via S_1, D_1 to transfer the energy into C_1 for clamping V_{C1} up to nV_S. Also, L_2 is connected with C_2 in series via S_1, D_4 to transfer the energy into C_4 (V_{L2}+V_{C2} →V_{C4}). At the same time, the control signals from SPWM controller are manipulating S_A be SPWM-ON and S_B be OFF, so as to make C_3 supplying the energy to C_O and R_L, and then V_O is heading towards the direction of the positive output.

2) Phase II:

During this time interval, turn OFF S_1 and S_A, and turn SPWM-ON S_B. The relevant topology is shown in Fig. 3(b). According to the booster theory, the steady-state voltage V_{L1} across L_1 is going towards $-DV_S/(1-D)$ via the cyclical operation of duty cycle D, and thus V_{L2} across L_2 in the secondary side is approaching the value of $-nDV_S/(1-D)$. Then, C_2 is charged by V_S, V_{L1}, V_{L2} in

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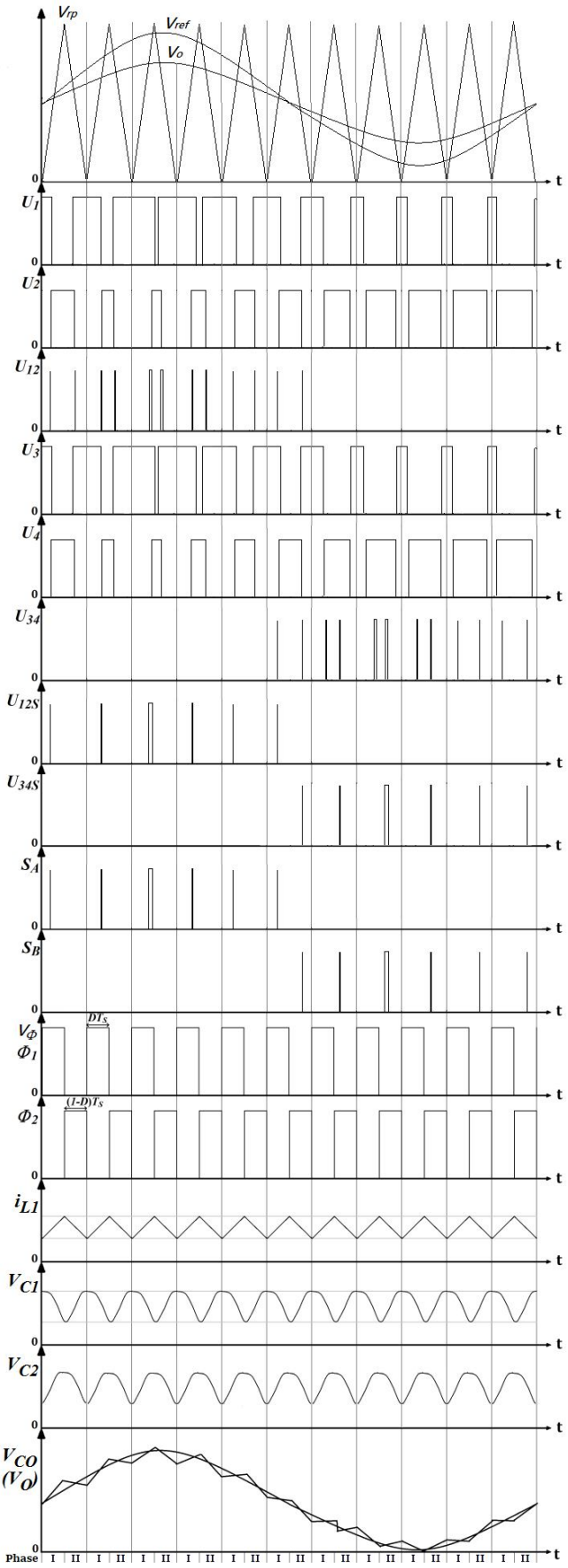

Fig. 2. Theoretical waveforms of GSCII.

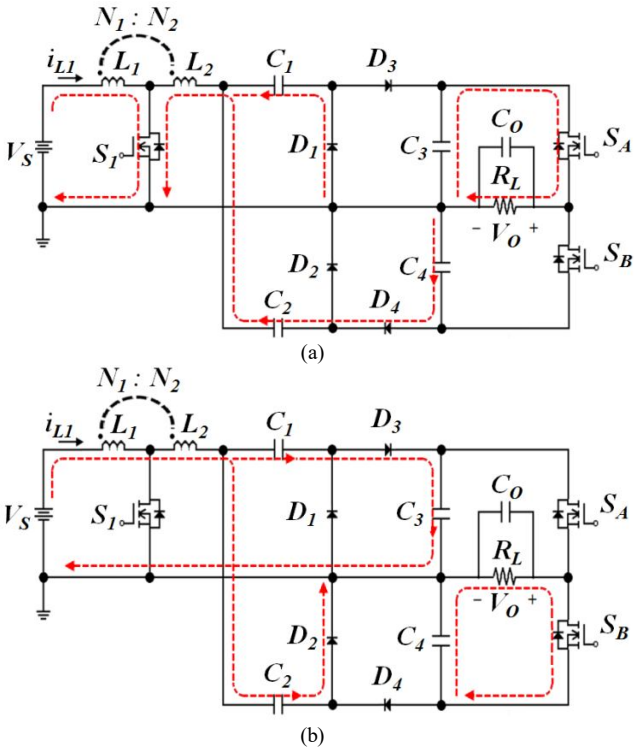

Fig. 3. Topologies for Phase (a) I (S_1:ON, S_A:SPWM-ON, S_B:OFF), (b) II (S_1:OFF, S_A:OFF, S_B:SPWM-ON).

series via D_2 (V_S+|V_{L1}|+|V_{L2}|→V_{C2}), and V_{C2} is going towards the value of V_S +DV_S/(1−D)+nDV_S/(1−D)= [(1+nD)/(1−D)]V_S. Simultaneously, the half-bridge capacitor C_3 is charged by V_S, V_{L1}, V_{L2}, and V_{C1} in series via D_3 (V_S+|V_{L1}|+|V_{L2}|+V_{C1}→V_{C3}), and so V_{C3} is going towards the value of V_S+DV_S/(1−D)+nDV_S/(1−D)+nV_S= [(n+1)/(1−D)]V_S. Now, the SPWM control signals are manipulating S_A be OFF and S_B be SPWM-ON, so as to make C_4 supplying the energy to C_O and R_L, and then V_O is heading towards the direction of the negative output. Here, a remark about V_{C4} across half-bridge capacitor C_4 is discussed. As mentioned above, L_2 is connected with C_2 in series via S_1, D_4 to transfer the energy into C_4 (V_{L2}+V_{C2}→V_{C4}) when the operation gets back to Phase I. Thus, V_{C4} is going towards the steady-state value of nV_S+(1+nD)V_S/(1−D)=[(n+1)/(1−D)]V_S. The half-bridge capacitor voltages V_{C3} and V_{C4} will be both boosted into [(n+1)/(1−D)]V_S.

Based on the cyclical operations of Phase I and II, the overall step-up output V_O can reach the AC voltage range as: +[(n+1)/(1−D)]V_S ~ −[(n+1)/(1−D)]V_S . For example, when V_S=24V, n=2, and D=0.5, both the steady-state values of V_{C3} and V_{C4} will be boosted into DC 144V. It is reasonable that the proposed inverter can attain the DC-AC conversion from DC 24V to AC 100V_{RMS}, 60Hz.

B. Control Part

The control part of this GSCII is composed of the phase generator and SPWM controller as in the lower half of Fig.1. The operations of the two blocks are discussed here. Firstly, a common timing integrated circuit (e.g. NE555) is employed and operated at the astable mode, and is treated as a multi-vibrator (i.e. function generator) to generate two synchronous non-symmetrical signals: square-wave function V_Φ and ramp-wave function V_{rp}, just like the waveforms as in Fig. 2. And then, V_{rp} is sent to the phase genertaor so as to obtain a set of non-overlapping anti-phase signals Φ_1 and Φ_2 referring to

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Phase I and II. In one T_S, Φ_1 and Φ_2 are with the high-level periods of DT_S and $(1-D)T_S$ for the driver signal of S_1 and the phase-in signal of S_A, S_B. The main goal is to generate the driver signals of switches for the different topologies.

Secondly, from the point of view of signal flow, the output voltage V_O is attenuated and fed back into the OP-amp low-pass filter (LPF) for high-frequency noise rejection. Next, the filtered V_O is obtained by combining a DC shift of V_C, and compared with the desired output V_{ref} via four comparators for U_1, U_2, U_3 and U_4. Following by using logic-AND, a set of SPWM control signals U_{12}, U_{34} can be obtained. When e>0 and |e| is rising (e= $V_{ref}-V_O$), the pulse width of U_{12} is getting bigger. When e<0 and |e| is rising, the pulse width of U_{34} is getting bigger. And then, by using the interlock circuit (avoid S_A and S_B being 1 simultaneously) plus coming into the phase of Φ_1 and Φ_2, the driver siagals of S_A and S_B can be obtained for realizing SPWM control. The main goal is to keep V_O on following the desired output V_{ref} (i.e. sinusoidal reference with output frequency f_O and amplitude V_m) to enhance the regulation capability of this proposed inverter. To summarize, based on V_O and V_{ref}, the rules of the control/driver signals are listed as follows.

1) Φ_1, Φ_2: non-overlapping anti-phase signals;
   $S_1=\Phi_1$;
2) If $V_{ref}>V_{rp}$, then $U_1=1$; If $V_{ref}<V_{rp}$, then $U_1=0$;
   If $V_{rp}>V_O$, then $U_2=1$; If $V_{rp}<V_O$, then $U_2=0$;
   If $V_O>V_{rp}$, then $U_3=1$; If $V_O<V_{rp}$, then $U_3=0$;
   If $V_{rp}>V_{ref}$, then $U_4=1$; If $V_{rp}<V_{ref}$, then $U_4=0$;
3) If $U_1=1$ and $U_2=1$, then $U_{12}=1$ (otherwise $U_{12}=0$);
   If $U_3=1$ and $U_4=1$, then $U_{34}=1$ (otherwise $U_{34}=0$);
4) If $U_{12}=1$ and $\Phi_1=1$, then $U_{12S}=1$ (otherwise $U_{12S}=0$);
   If $U_{34}=1$ and $\Phi_2=1$, then $U_{34S}=1$ (otherwise $U_{34S}=0$);
5) SPWM control signals:
   $S_A=U_{12S}$, for $V_{ref}>V_O$;
   $S_B=U_{34S}$, for $V_{ref}<V_O$.
   (Interlock: $U_{12S}\cdot U_{34S}\neq 1$)

III. Examples of GSCII

In this paper, the proposed GSCII is simulatedby SPICE, and all circuit parameters are listed in TABLE I. Based on the parameters, we have three cases for steady-state responses and four cases for dynamic responses in total. Then, these results are illustrated to verify the efficacy of the proposed inverter.

TABLE I
Circuit parameters of GSCII.

Supply source (V_S)	24V
Pumping capacitor (C_1, C_2)	47μF
Coupled inductor (L_1, L_2)	80μH, 320μH (n=2)
Half-bridge capacitor (C_3, C_4)	47μF
Output capacitor (C_O)	1.5μF
Power MOSFETs (S_1/S_A,S_B)	ASW (ON-state: 50μΩ/0.5Ω)
Dodes (D_1–D_4)	D1N5822
Load resistor (R_L)	500Ω
Switching frequency (f_S)	50kHz

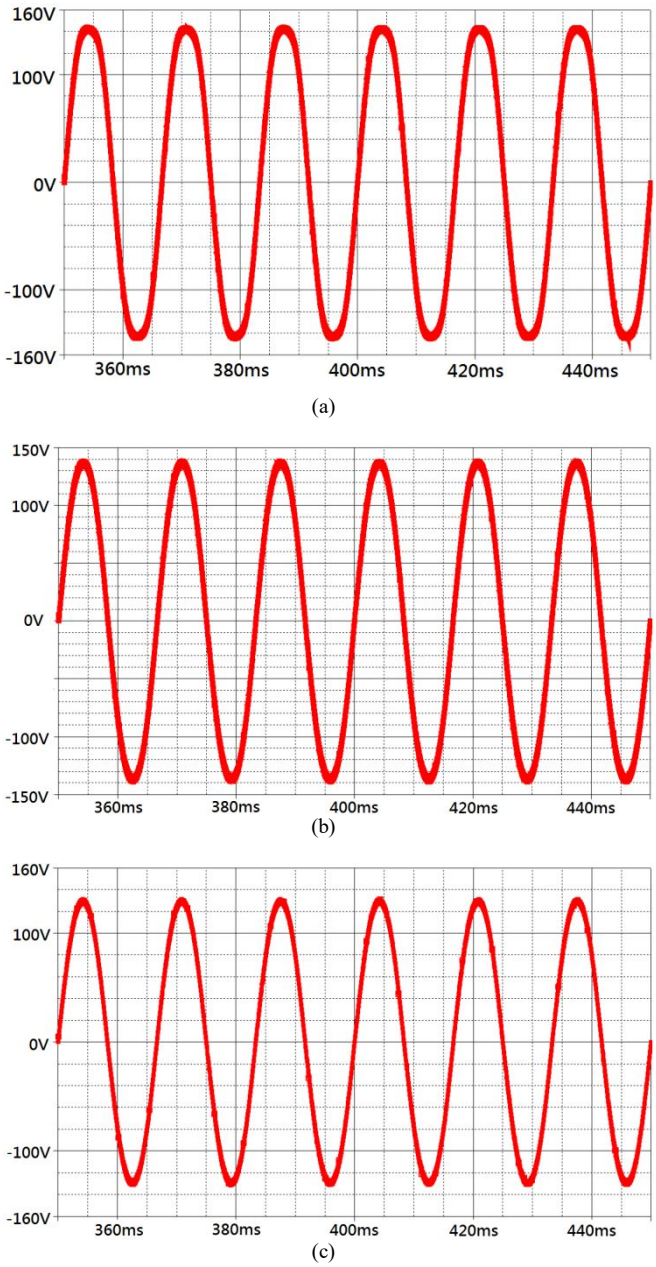

Fig. 4. Output V_O for V_{ref}: (a) f_O=60Hz, V_m=145V; (b) f_O=60Hz, V_m=135V; (c) f_O =60Hz, V_m=125V.

1) Steady-State Responses:

Case 1: f_O=60Hz, V_m=145V

Let the supply source V_S be DC 24V, load R_L be 500Ω, and the peak value and output frequency of V_{ref} are V_m=145V, f_O=60Hz. The waveform of V_O is obtained as in Fig. 4(a). V_O has the practical peak value of 142.5V (i.e. $100V_{RMS}$), and the practical output frequency is about 60Hz. The efficiency is 72.47% and the value of total harmonic distortion (THD) is 6.654%.

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Case 2: f_O=60Hz, V_m=135V

Let the supply source V_S be DC 24V, load R_L be 500Ω, and the peak value and output frequency of V_{ref} are V_m=135V, f_O=60Hz. The waveform of V_O is obtained as in Fig. 4(b). V_O has the practical peak value of 137.2V (i.e. 97V_{RMS}), and the practical output frequency is about 60Hz. The efficiency is 61.1% and THD is 2.078%.

Case 3: f_O=60Hz, V_m=125V

Let the supply source V_S be DC 24V, load R_L be 500Ω, and the peak value and output frequency of V_{ref} are V_m=125V, f_O=60Hz. The waveform of V_O is obtained as in Fig. 4(c). V_O has the practical peak value of 129.6V (i.e. 92V_{RMS}), and the practical output frequency is about 60Hz. The efficiency is 55.3% and THD is 1.475%.

2) Dynamic Responses:

Since the battery voltage is getting low as the battery is working long time, or the bad quality of battery results in the impurity of supply voltage, such a variation of source V_S must be considered, as well as variation of load R_L and/or reference V_{ref} (f_O or V_m).

Case 1: variation of V_S

Assume that V_S is normally at DC 24V, and then it has an instant voltage drop of 24V→22V on 466ms and a voltage jump of 22V→24V on 516ms (V_{ref}: f_O=60Hz, V_m=145V). The waveform of V_O is shown as in Fig. 5(a). Obviously, V_O has a slight decrease to about 139V during the variation of V_S. After that, V_O still can get back into following V_{ref} as usual.

Case 2: variation of R_L

Assume that R_L is 500Ω normally, and then it suddenly changes from 500Ω to 300Ω on 466ms and changes from 300Ω to 500Ω on 516ms (V_{ref}: f_O=60Hz, V_m=145V). Fig. 5(b) shows the transient waveform of V_O during the variation of R_L. Obviously, V_O has a small voltage drop but can still be following V_{ref}.

Case 3: variation of f_O

Assume that the frequency f_O of V_{ref} is 60Hz normally, and then it suddenly changes from 60Hz to 120Hz during the period from 466ms to 516ms. Fig. 5(c) shows the transient waveform of V_O at the moment of variation: f_O=60Hz→120Hz→60Hz (V_m=145V). Obviously, V_O is still able to follow V_{ref} even the output frequency f_O changes.

Case 4: variation of V_m

Assume that V_m is 145V normally, and then it suddenly changes from 145V to 125V on 466ms and changes from 125V to 145V on 516ms. Fig. 5(d) shows the transient waveform of V_O at the moment of variation: V_m=145V→125V→145V (f_O=60Hz). Obviously, V_O is still able to follow V_{ref} even the output amplitude V_m changes.

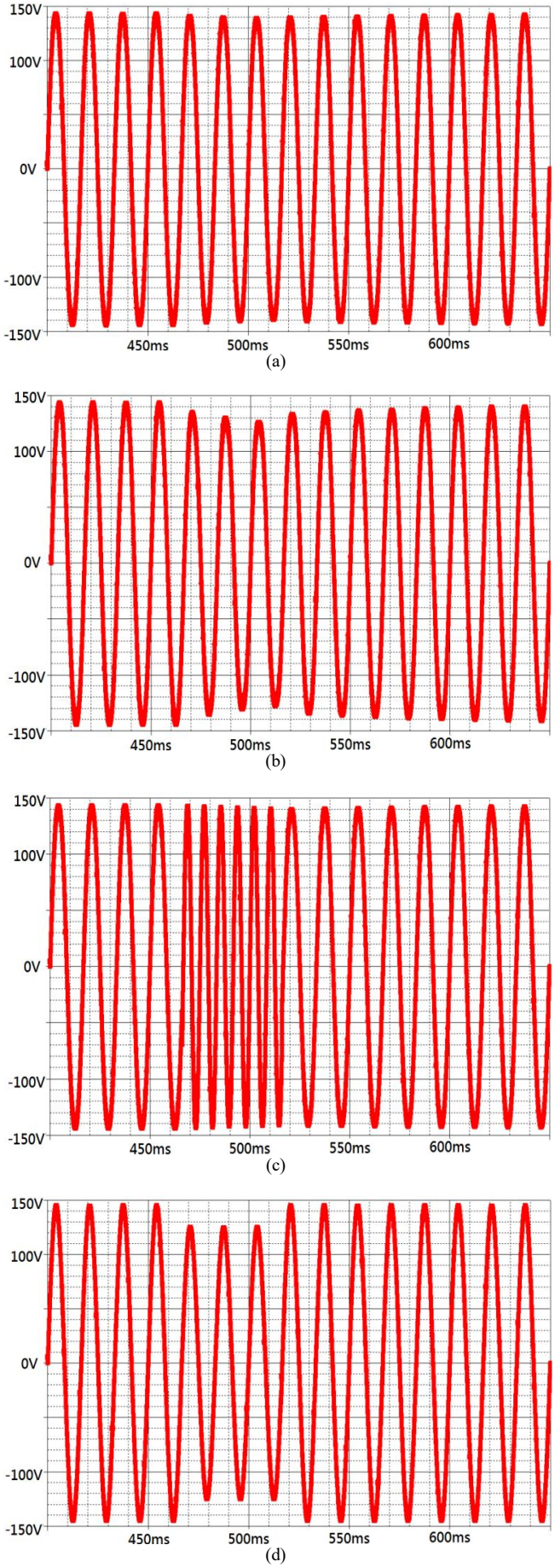

Fig. 5. Output V_O for the variation of (a) V_S; (b) R_L; (c) f_O; (d) V_m.

According to the above results, it is obvious that V_O is following V_{ref} for the cases, including V_S source variation, R_L

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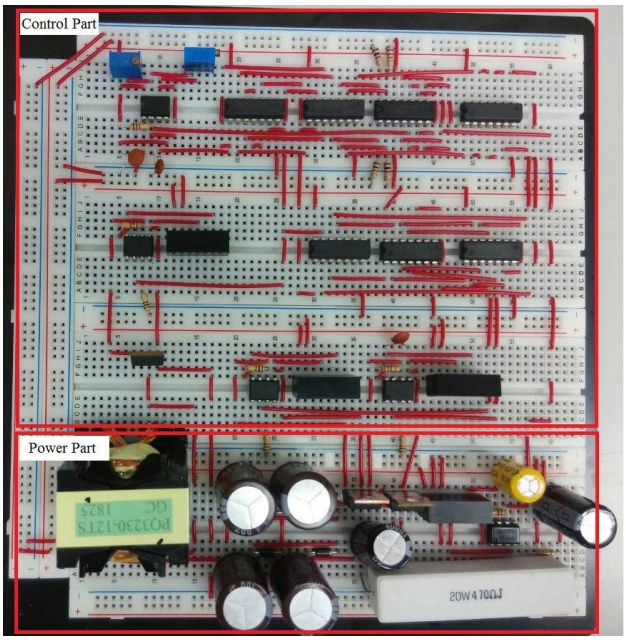

Fig. 6. Prototype circuit of GSCII.

loading variation, f_O frequency variation, V_m amplitude variation. These results show that this proposed inverter has good closed-loop dynamic performances.

IV. Conclusions

This paper presents a simple configuration of GSCII by combining a non-overlapping phase generator and a SPWM controller in order to realize boost DC-AC conversion and closed-loop regulation. The power part is composed of a Greinacher-doubler-based SCI booster and a half-bridge DC-link inverter between supply V_S and output V_O, so as to obtain the AC output range: $+[(n+1)/(1-D)]V_S \sim -[(n+1)/(1-D)]V_S$, where n is the turn ratio of the coupled inductor and D is duty cycle of charging this inductor. When n=2 and D=0.5, the DC-AC conversion from DC 24V to AC 100V_{RMS}, 60Hz can practically be achieved. Finally, the closed-loop GSCII is designed and simulated by SPICE for some cases of steady-state and dynamic responses. The advantages of the proposed scheme are listed as follows. (i) This GSCII needs just one coupled inductor. Except this, other components (switches, diodes, and capacitors) can be made in IC fabrication promisingly. (ii) This proposed inverter sure is to present a simple boost DC-AC scheme via using fewer device count. It is beneficial to circuit complexity decrease as well as cost reduction. (iii) For a higher gain, it can be realized with increasing the turn ratio of coupled inductor and/or extending the number of capacitors. (iv) The SPWM technique is adopted not only to enhance output regulation capability for the different desired output, but also to reinforce the output robustness against source/loading variation. At present, the prototype circuit of this inverter is implemented in the lab as in the photo of Fig. 6. Some experimental results will be obtained and measured for the verification of the proposed inverter.

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