Backside Layout Design of Snapback-free RCIGBT with Multiple-Cell

Zhongke. Chang, Xiaofei. Zhu, and Masahide. Inuishi

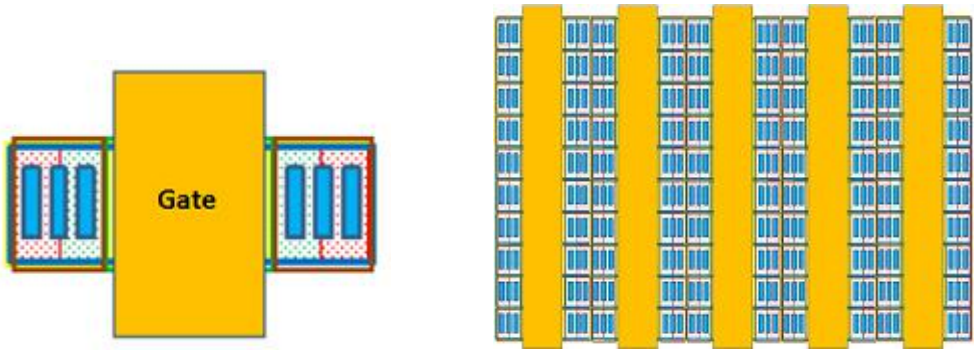
ABSTRACT—A backside layout design for multiple cell RCIGBT is proposed to suppress the snapback effect which happens in the turn-on process of RCIGBT in this paper. The internal operation mechanism of RCIGBT has been analyzed by device simulation, proving that our backside layout design works well. Reduction in the ratio of backside N+/P+ area as well as the N buffer doping density and increase in the number of cells in chip are all proved as useful methods in reducing snapback voltage. Although some novel RCIGBT structures have been proposed to eliminate the snapback effect, most of them have been based on a single cell structure, which is not sufficient for the analysis of RCIGBT. It's more practical and feasible in production to simply optimize the backside layout design of N+, P+ short area with the multiple cell RCIGBT structure. Here we will report on the analysis of the snapback effect and the backside optimum layout design for the multiple cell RCIGBT.

Index Terms—backside layout, multiple cell, RCIGBT, snapback

I. Introduction

The RCIGBT(reverse-conducting insulated gate bipolar transistor) is a promising kind of power devices, which can replace the pair of an IGBT chip and a free wheeling diode chip in some conversion circuits by one. Also it can flow larger current than the VDMOS. However, the snapback effect is a common problem in the turn on process of RCIGBT, which has a bad influence on the performance of circuits.

In this paper, we propose a novel and practical backside layout design, taking the multiple cell structure of RCIGBT into consideration, as shown in Fig. 1(b). The results of simulation clarify that our design can achieve snapback-free with simpler fabrication process comparing with other structure designs based on a single cell, which will be helpful in production.



(a) (b)

Fig. 1. Top view of RCIGBT chip (a)Single cell structure (b)Multiple cell structure

II. Structure and Mechanism

The operating mechanism of RCIGBT in the forward mode can be divided into two modes generally. In Fig. 2, the P body, the N-drift region and the P+ collector form a PNP bipolar transistor. R_{ch} is the channel resistance. R_j is the the junction FET resistance. $R_{n\text{-}drift}$ is the the drift region resistance. And R_{CS} is the equivalent collector short resistance which impedes electrons to flow from the drift region to the N+ collector short. I_e and I_h are the electron current and the hole current. In Fig. 2(a), the voltage between the base and the emitter is low. PNP bipolar transistor is in the OFF state. There is only electron current flowing through the device. RCIGBT works in the MOS mode. With the increase of collector voltage, RCIGBT turns into the IGBT mode like Fig. 2(b). Holes in the P+ collector are injected into the N-drift region and the PNP bipolar transistor turns on. The conductivity modulation of the drift region causes the significant reduction of the $R_{n\text{-}drift}$, which leads to a snapback in voltage[1]. V_{SB} is the collector voltage when snapback

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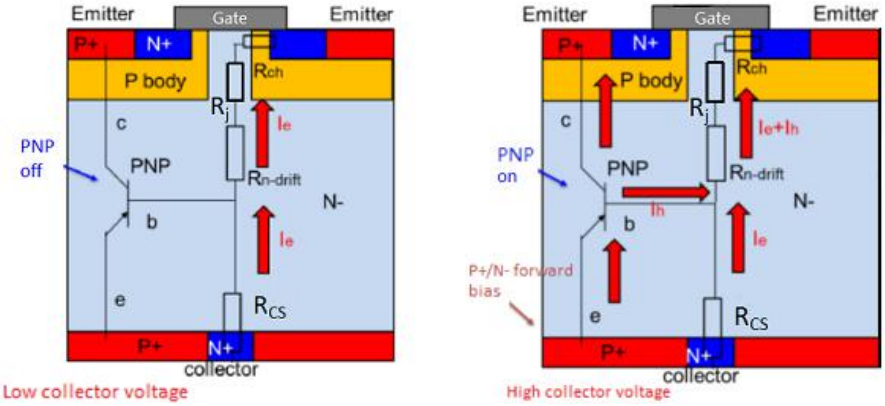
effect happens. V_{pn} is the build-in potential between backside P+ short and N-drift or backside P+ short and N-buffer[2].



(a) (b)

Fig. 2. Forward mode of RCIGBT (a)MOS Mode (b)IGBT Mode

Fig. 3 shows the snapback effect in the I-V characteristics of RCIGBT.

$$V_{SB} = \frac{R_{ch} + R_j + R_{n\text{-}drift} + R_{CS}}{R_{CS}} V_{pn} \qquad (1)$$

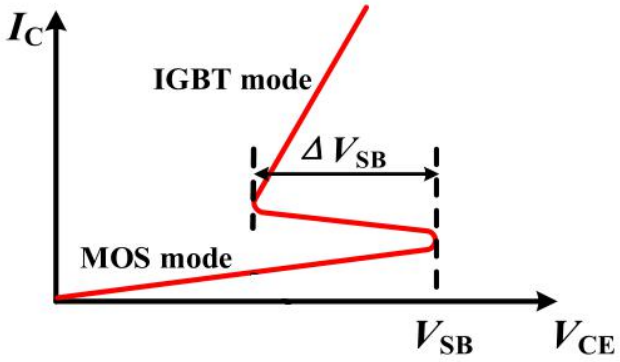


Fig. 3. Snapback effect of RCIGBT

III. Simulation and Analysis

Refer to (1), there are four factors R_{ch}, R_j, $R_{n\text{-}drift}$ and R_{CS}, which can be adjusted to suppress the snapback effect. R_{ch}, R_j and $R_{n\text{-}drift}$ are mainly determined by the MOSFET structure and the doping concentration of the wafer while R_{CS} mainly depends on the backside layout.

A. Reducing R_{ch} and R_j

By extending the distance between two P bodies in each cell or reducing the lateral channel length under the gate, we can obtain smaller R_j and R_{ch}, leading to smaller V_{SB}.

Since the carrier density is also influenced by the P-body distance and the channel length after the device turns into the IGBT mode, even though we can reduce V_{SB}, ΔV_{SB} keeps almost the same.

B. Reducing $R_{n\text{-}drift}$

By reducing the wafer thickness or using the carrier stored layer(CS layer)[3] under the P body, the conductivity modulation[4] by the injection of carriers into the N-drift region can be enhanced. As a result, we can obtain smaller $R_{n\text{-}drift}$ and smaller V_{SB}.

In the same principle as reducing R_{ch} and R_j, the carrier densities of hole and electron increase and we can reduce V_{SB}. However, ΔV_{SB} keeps almost the same. As shown in Fig. 4, the V_{SB}(10V) of RCIGBT on 150um wafer is much smaller than that(18V) of RCIGBT on 300um wafer, while the ΔV_{SB}(5.6V) of RCIGBT on 150um wafer is almost the same as that(5.8V) of RCIGBT on 300um wafer.

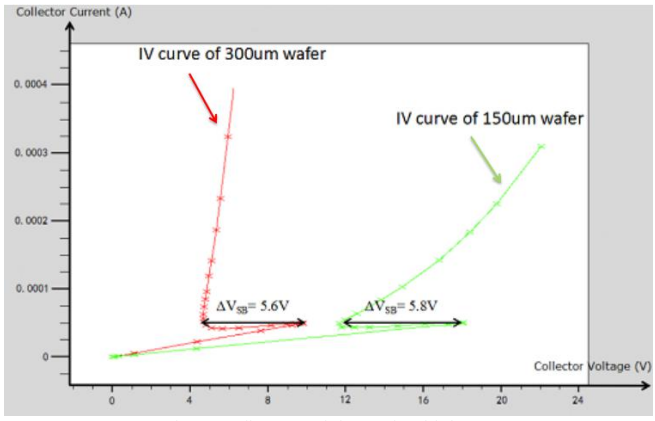


Fig. 4. Influence of the wafer thickness

C. Increasing R_{CS}

R_{ch}, R_j and $R_{n\text{-}drift}$ are constant once structure parameters of the MOS device and the wafer are determined. Since it is preferable to reduce not only V_{SB} but also ΔV_{SB}, we need to increase R_{CS} by optimizing the backside layout.

Amounts of analysis and simulation of a single cell RCIGBT have been reported by former researchers. However, actual power device products usually consist of hundreds of single cell which are connected in parallel in order to flow large current. Analysis only based on single cell is not sufficient and reliable for the improvement of RCIGBT. Fig. 5 shows the basic multiple cell structure of our device

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simulation.

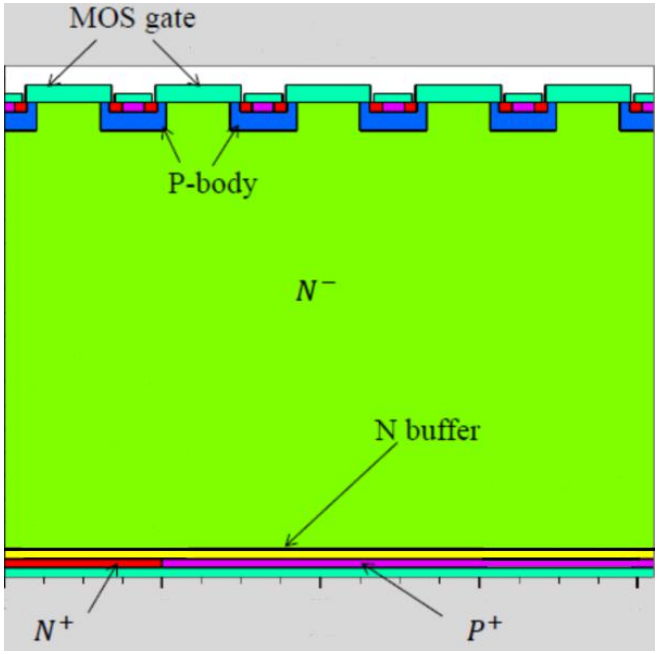

Fig. 5. Multiple Cell RCIGBT structure

Table. I gives the parameters used for the multiple cell RCIGBT in device simulation.

As shown in Fig. 6, when the number of the top cells increases while the ratio of backside N+/P+ area is kept constant as 1:1, V_{SB} is reduced from 100V(2 cells), 50V(3 cells) to 18V(5 cells). Also ΔV_{SB} is reduced from 77V(2 cells), 32V(3 cells) to 7V(5 cells).

TABLE I
DEVICE SPECIFICATIONS

Parameter	Value
Wafer thickness	300 um
N-drift doping density	1×10^{14} cm^{-3} (Phosphor)
N-drift width for each cell	82 um
N-buffer thickness	1 um
P-body width for each cell	21 um
P-body depth	10 um
P-body doping density	5×10^{16} cm^{-3} (Boron)
Backside N+ short thickness	1 um
Backside N+ short doping density	1×10^{20} cm^{-3} (Phosphor)
Backside P+ short thickness	1 um
Backside P+ short doping density	1×10^{20} cm^{-3} (Boron)
N-emitter thickness	1 um
N-emitter doping density	1×10^{20} cm^{-3} (Phosphor)
P-emitter thickness	1 um
P-emitter doping density	1×10^{20} cm^{-3} (Boron)
Gate oxide thickness	50 nm
Gate voltage	15V

Once the gate is turned on and high voltage is applied to the collector, the initial electron current flows from the N-emitter to the backside N+ short, passing through the N-drift region above the collector. We can regard the travelling path of electrons inside the N-drift region as two dimensions: vertical and lateral. Actually, the lateral distance along which the initial electron current flows increases with increase in the number of the top cells, as shown in Fig. 7. In this way, R_{CS} increases, resulting in the reduction of the snapback effect.

In the same principle, reducing the ratio of backside N+/P+ short area can also suppress the snapback effect[5].

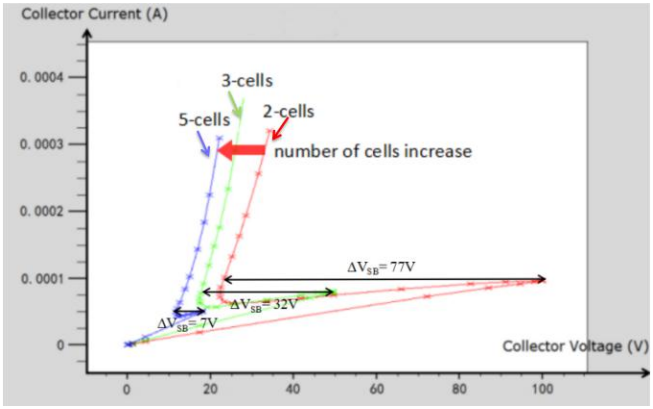

Fig. 6. Influence of the number of cells on snapback voltage(N buffer doping=5×10^{16}cm^{-3})

Fig. 7 shows the backside N+ short placed at the one side of the chip instead of in the middle position. With this layout design, the total lateral travelling distance of electron currents from each channel will be the maximum. Consequently the snapback effect can be completely eliminated as shown in Fig. 8.

Surrounding the IGBT area with reverse diode area on the backside of the chip will be an economical and practical snapback-free method.

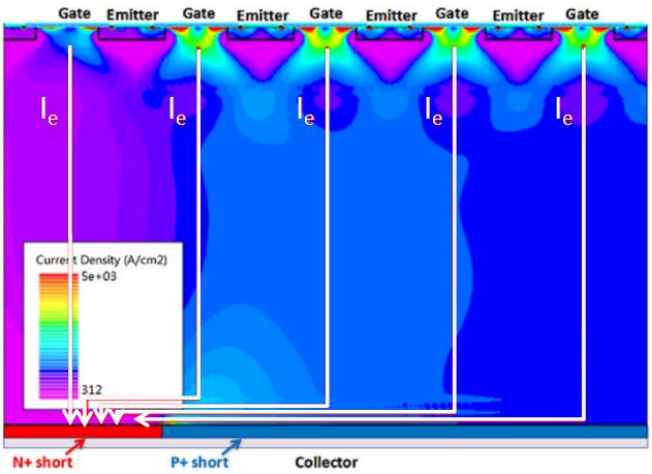

Fig. 7. Electron Current distribution

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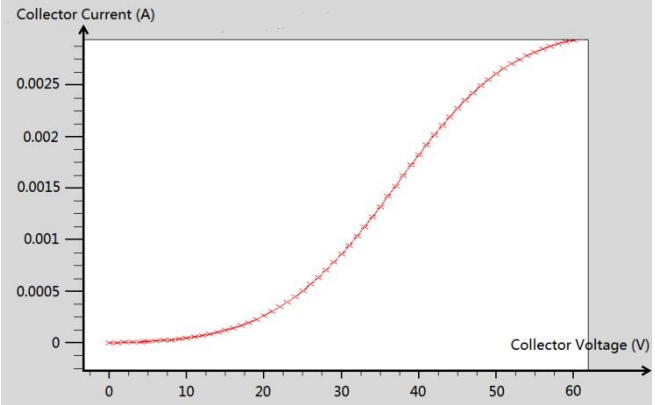


Fig. 8. I-V characteristics when N+ short is at side(N buffer doping=$1\times10^{17}cm^{-3}$, ratio of backside N+/P+ width=1:3)

In Fig. 9, V_{SB} is reduced from 32V($1\times10^{17}cm^{-3}$), 17.5V($5\times10^{16}cm^{-3}$) to 0V($1\times10^{16}cm^{-3}$) with the decrease of the N-buffer doping density. Also ΔV_{SB} is reduced from 16V($1\times10^{17}cm^{-3}$), 5V($5\times10^{16}cm^{-3}$) to 0V($1\times10^{16}cm^{-3}$).

The N-buffer, commonly used to increase the breakdown voltage, also affects the snapback voltage. With increase in the N-buffer doping density, the breakdown voltage of the vertical device will increase. Taking the trade-off relationship of breakdown voltage and snapback voltage into consideration, it is required to optimize the N-buffer doping density.

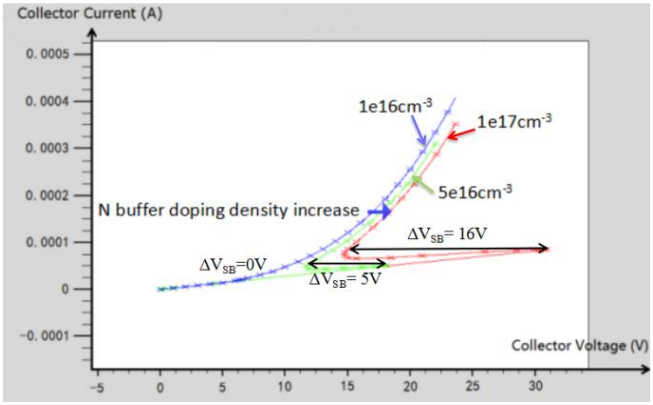
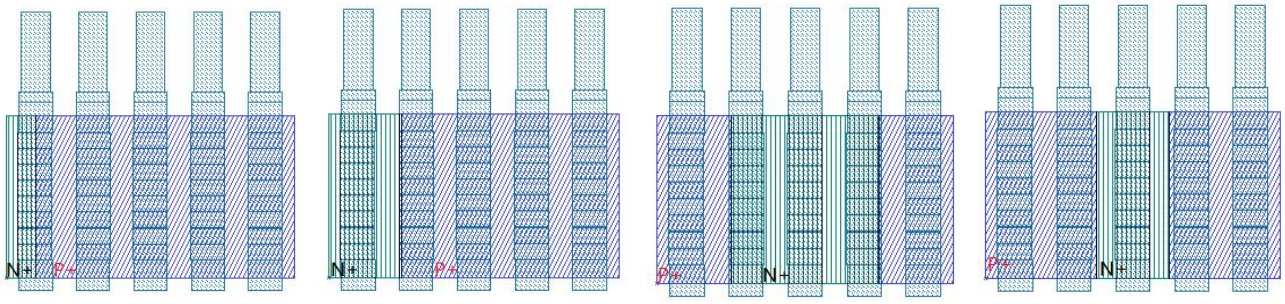


Fig. 9. Influence of the N-buffer doping density (ratio of N+/P+=1:1, N+ in the middle of backside, N-buffer doping=1×10^{16}, 5×10^{16}, $1\times10^{17}cm^{-3}$)

IV. Experiment and Results

We have designed several kinds of backside layout for RCIGBT chip. Fig. 10 shows some of our backside masks which will be used in the fabrication process. In Fig. 10, the whole backside active area of the chip is covered by the N+ short and the P+ short. The ratio of N+/P+ area are 1:9, 1:3 and 1:1 respectively with N+ area at one side of the chip and in the middle of the chip.



(a) (b) (c) (d)

Fig.10. Backside masks for N+/P+ short area with Gate
(a)N+ area at side & N+/P+=1：9 (b)N+ area at side & N+/P+=1：3 (c)N+ area in the middle & N+/P+=1：3 (d)N+ area in the middle & N+/P+=1：1

Fig. 11 shows the fabricated wafer.

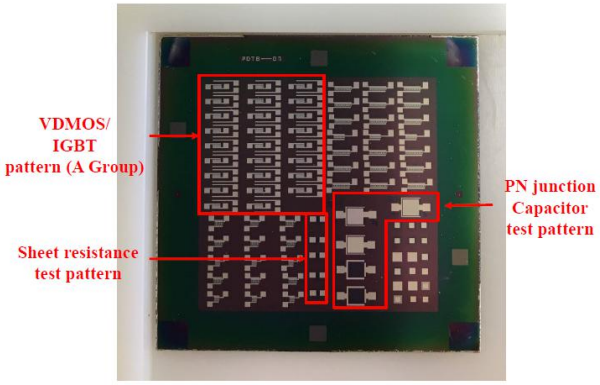


Fig. 11. Power devices on wafer including RCIGBT

V. Conclusion

Basically, there are several design methods of backside layout to suppress the snapback effect in the turn on process of RCIGBT, such as increasing the number of cells in power device chip, reduction in the ratio of the backside N+/P+ short area and decrease in the N-buffer doping density within limit. However, optimizing the relative positions of backside N+/P+ shorts is a more practical way for the production.

Novel RCIGBT structures like AB RCIGBT, TFP RCIGBT, and DFS RCIGBT[6-12] have been proposed to realize snapback-free RCIGBT. But the multiple cell structure should be taken into consideration when we analysis and evaluate the characteristic of the RCIGBT.

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