UVM Verification of Multicarrier Modulation System (FDM)

Laksh Lavish Thakkar, Zenithbhai Chokshi, and Lili He, *Member, IAENG*

ABSTRACT-OFDM or orthogonal frequency-division is one of those concepts that have been percolating for a long time and finally materialized when mass market applications appeared at the same time as efficient software and electrical technologies were widely available. This article provides an overview of the history and early development of OFDM, as well as an explanation of the reasons for using it. Offset frequency-division multiplexing (OFDM) is a kind of frequency-division multiplexing (FDM) in which adjacent sub-channels do not interfere with one another. However, the computing approach known as the fast Fourier transform (FFT) of the discrete Fourier transform (DFT) is not required. For OFDM, this research uses the Universal Verification Methodology to validate the Backward Fourier Transform (IFFT), the feasible technique, and the QPSK algorithms. The IEEE 1800 standard for UVM guides developing a setting conducive to verifying elaborate designs. The UVM verification developed for this project is portable, meaning it may be used to check algorithms utilized by other FDM techniques.

Index Terms- QPSK, FDM, System Verilog, Verification

I. Introduction

Among all the possible modulation options QPSK has two pair to signals whose phase difference is 90 degrees. Multiplexing using orthogonal frequency division, sometimes known as OFDM multiplexing, is a kind of multicarrier modulation. An OFDM signal is a set of closely spaced modulated carriers that are produced when OFDM is applied [10]. The stream of high data rate is spread over many narrowband subcarriers, each of which is modulated slowly and is closely spaced. This is how OFDM modulation systems work. The data signals that make up an OFDM signal must be geographically separated from one another by a certain quantity of carrier space for the receiver to correctly demodulate the signal. The reciprocity of the symbol period, which is the whole time that an OFDM signal is transmitted, is what determines the carrier spacing [9].

The fact that an OFDM transmitter and receiver system must operate linearly is the most crucial requirement for the system. As was previously said, the OFDM signal is comprised of a great deal of modulated digital signals. If there is any nonlinearity in the system, this will produce inter-modulation distortion, which will lead to a loss of information on the receiver side. The following are some of how the OFDM approach is distinct from more conventional frequency division multiplexing techniques:

1. The information stream is carried by more than one carrier in the OFDM system.

2. In the OFDM system, all subcarriers are orthogonal (parallel in-phase).

3. A guard interval (carrier spacing) is placed between the subcarriers in the OFDM system to prevent inter-modulation interference the OFDM system to prevent inter-modulation interference.

Fig.1 displays an easy-to-understand representation of the OFDM signal in the form of frequency against time. The diagram illustrates how the OFDM signal's time domain and frequency domain are interrelated with one another. The graphic makes it very evident that, in the frequency domain, numerous subcarriers are individually modulated with complicated digital data [10]. This can be seen quite clearly in the Diagram. On the modulator side, the picture depicts a basic IFFT implementation, whereas, on the demodulator side, an FFT is shown.

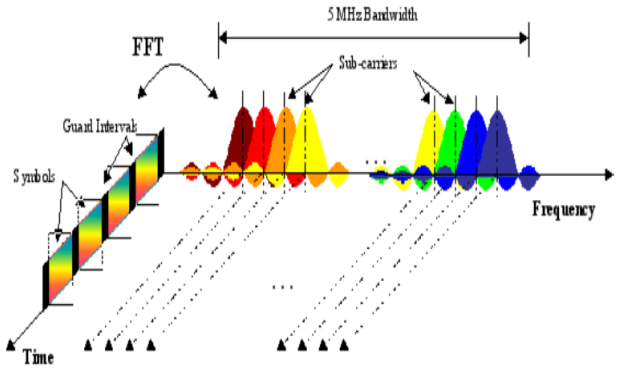

Fig. 1. Frequency vs. Time representation of Orthogonal Signals

On the transmitter side, IFFT is used to modulate the multiple digital signals, while on the reception side, FFT is used to demodulate the incoming OFDM signals. Both functions are performed by the receiver. In this context, the term "modulate signal" refers to the process of converting signals from the time domain to the frequency domain,

Manuscript received March 6, revised May 30, 2023.
Mr. Thakkar(email: laksh.thakkar@sjsu.edu and Mr. Chokshi (email: Zenithbhai. Chokshi@ sjsu. edu were graduate students and Dr. Lili He (email: lili.he@sjsu.edu) is a professor at the Department of Electrical Engineering, San Jose State University, San Jose, California, USA. Mr. Thakkar and Mr. Chokshi are equal contribution authors.

while the term "demodulation" refers to the process of transferring a signal from the frequency domain to the time domain. Guard intervals are included in the OFDM signal to avoid interference between symbols, and the original data bits are reconstructed at the receiver using FFT.

Verification work is being done on the OFDM scheme's Inverse Fast Fourier Transforms (IFFT), Pilot-based method, and Quadrature Phase Shift Keying (QPSK) algorithms as part of this project. The Universal Verification Method is used in the setting where verification is performed. Verification consists of the following: the generation of sequences to stimulate the Design Under Test (DUT); the use of an input and output monitor to observe the pin-level activities on the DUT; the use of a driver to send the generated sequences on the DUT; the use of scoreboards to capture and process the pin level information from the input and output monitors; the use of an active agent to encapsulate the driver, monitor, and sequence for the OFDM transmitter interface; the use of an environment to create For this project, the black-box method of verification is used to confirm the design of the OFDM transmitter. To test whether or whether the DUT functions correctly, we have further made use of GTK wave analysis and UVM standardized messaging.

II. OFDM BLOCK DIAGRAM

A. OFDM Tx and Rx

The diagram on the right illustrates the fundamental idea that underpins the production of OFDM signals. In this fundamental system, there are N concurrent sine and cosine signals, and every child carrier transmits single-bit data, with the amount of data transmitted being determined by whether it is present in the output, which is indicated by switches that come before the symbol combiner [10]. The output signal is refreshed at the end of each periodic interval that corresponds to the symbol period (T). To keep the statistical independence of the OFDM system unbroken, the symbol period must be the inverse of the subcarrier spacing [1].

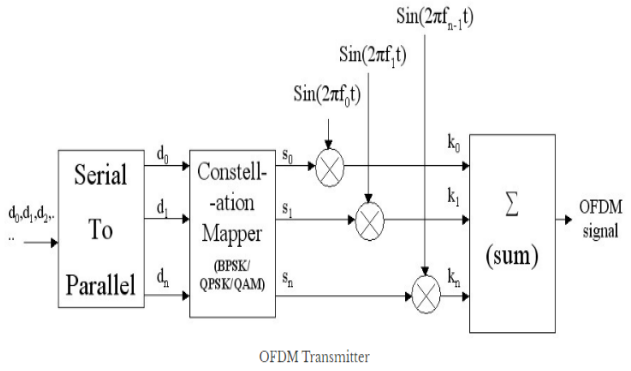

Fig. 2. OFDM Tx Block Diagram

In traditional modulation techniques, a single bit is sent one at a time via the carrier. On the other hand, OFDM transmits many bits over a single carrier in a parallel fashion [3]. Since this is the case, we can transmit numerous message signals simultaneously by using the same carrier for its modulation. OFDM system offers numerous advantages [3]:

1. Frequency Selective Fading: Single channel is converted into multiple side bands in OFDM Technique, so it is resistant to frequency selective fading.
2. Immune to Intersymbol Interference: Due to the fewer frequency variations in OFDM signal, it is very immune to the effects of intersymbol interference. Resistance to Interference: Because OFDM restricts interference to a specific channel's bandwidth, the interference will not affect the sub-channel, making the OFDM signal resistant to interference.
3. The Orthogonal Frequency Division Multiplexing technology has achieved a large amount of favor in the market for wireless networking because of its high information capacity, high bandwidth, and immunity to interference [8]. OFDM has developed into an essential component of the modern wireless communication industry [2] since all these characteristics are of great significance in the modern wireless communication scene. The following is a list of some of the OFDM system's further applications:
   i. Wireless Fidelity
   ii. Wireless and Cellular Communication
   iii. Radio and Television Broadcasting
   iv. 4G/5G communication

B. IFFT Implementation for OFDM Receiver

The step-by-step implementation of IFFT is shown in the Diagram that may be seen below. The components of the system are as follows: a modulator, a backward Fourier Transform block, a concurrent to bit-by-bit converter, and a frequency up-conversion unit. The outcomes of the simulations performed on the Transmitter have been appended in a different section. Our given approach employs 16 space diagram points. To generate a variety of distinct constellations, the constellation data is split up into registers of four bits each, and then each bit is encoded with gray code for improved precision [7]. The two bits known as the MSB are used to represent imaginary numbers, whereas the two bits known as the LSB are used to represent real numbers. System Verilog makes use of the case statement to do it [8].

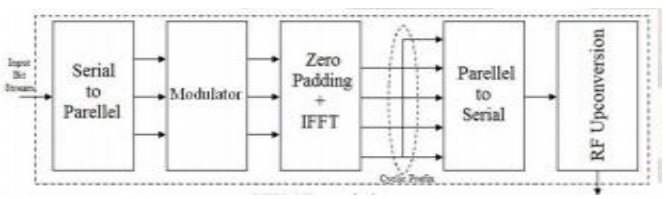

Fig. 3. IFFT Receiver Flow diagram

IFFT: After the bit-by-bit to concurrent conversion has been completed, the base 2 reduction in sampling rate in time for the IFFT algorithm is used for the data. Diagram

ISBN: 978-988-14049-4-7
ISSN: 2078-0958 (Print); ISSN: 2078-0966 (Online)

4 displays a straightforward butterfly diagram of the radix2 decimation in time IFFT algorithm. The same base 2 decimations in frequency are applied on the receiver's end.

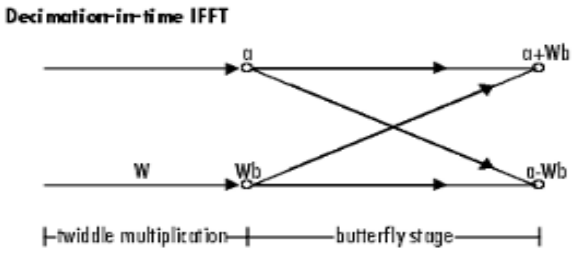

Fig. 4. Radix 2 Decimation in time IFFT

So that the OFDM signal may be demodulated. The QAM modulation method is utilized here in this backward Fourier transform format of the FDM system to generate a new constellation [6]. The desired system receives the data bit by bit, converts it into the concurrent data bit streamline, modulates every single data bit using the Quad Plan Amplitude modulation, and then implements the backward Fourier Transform to the data bits. This process begins when the system receives the serial data. Following the execution of the backward Fourier Transform on the data bits, the system transforms the concurrent bits of data into streamlined serialized data, and then it sends the signal via a frequency up-conversion block [7]. The following is a straightforward equation:

IFFT

$$X(n)=\frac{1}{N}*\sum_{k=0}^{N-1} X(k) * e^{i*2*pi*n*k/N} \quad \text{...IFFT Equation}$$

Where, X(n) = Signal Representation in Time Domain

X(k) = Signal Representation in Frequency Domain

K ∈ [0:N-1]

N = Size of FFT Sample Data

C. Testbench Verification Flow

Universal Verification Methodology is the full meaning of the abbreviation UVM. Hardware validation using this technique is the standard in the business world. Engineers may use UVM's collection of application programming interfaces (APIs), classes, and documented verification rules to create a verification environment that is both reusable and effective. Code written in UVM is made more efficient by using features from System Verilog. The Unified Verilog Model (UVM) is a class structure for the System Verilog language [12].

Key UVM code structure elements are UVM Sequence, UVM Sequence Item, UVM Driver, UVM Monitor, and UVM Scoreboard. Here's a visual representation of this fact:

Testbench Class Hierarchy provides a collection of fundamental classes. The parent class is often used to refer to the foundational classes. Classes that are derived from another or the parent class are called "extended classes" or "kid classes." Therefore, the engineer constructs several child classes to do all the necessary tasks in the code [6]. These descendant classes rely on properties defined by their ancestors. Such enlargements are called Inheritance in System Verilog.

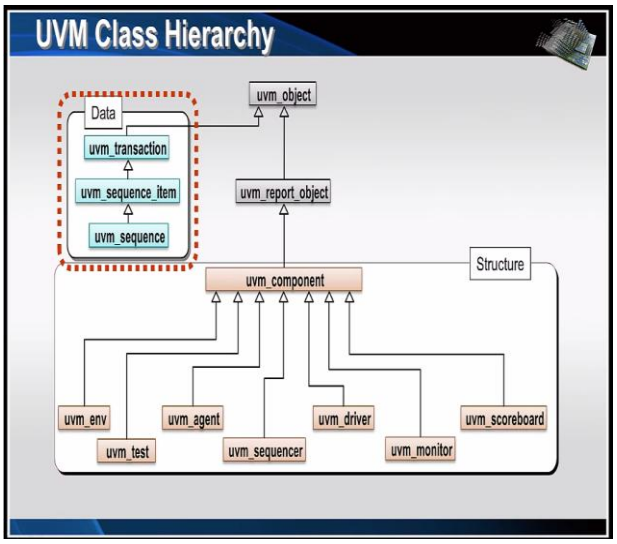

Fig. 5. Hierarchy – UVM

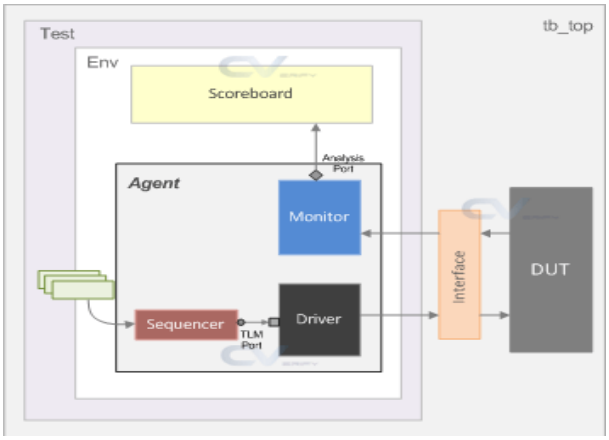

Fig. 6. Component Hierarchy UVM

III. Result and Analysis

Test Module FDM: The test module is constructed after the root module in the UVM module hierarchy. The uvm test parent class extends the test module. The UVM test class is used to generate and instantiate the environment and sequence.

Wrapper Module FDM: All connections between the UVM environment and the System Verilog DUT are contained inside the FDM/DUT wrapper. This instantiation might potentially be done in the root module, but it's often done in a wrapper for better scalability and more obvious placement.

ISBN: 978-988-14049-4-7
ISSN: 2078-0958 (Print); ISSN: 2078-0966 (Online)

```
module top();

FDM_interface FDM_inf();
QPSK_wrap dut_qpsk(FDM_inf.qpsk_mp);

initial begin
    FDM_inf.clk=0;
    FDM_inf.rst=1;
    #10 FDM_inf.rst=0;
    forever #10 FDM_inf.clk=~FDM_inf.clk;
    #1000;
    $finish;
end

initial begin
    uvm_config_db #(virtual FDM_interface)::set(null, "*", "v_if", FDM_inf);
    run_test("FDM_test");
end

initial begin
    $dumpvars;
    $dumpfile("QPSK.vcd");
end

endmodule : top
```

Fig. 7. FDM DUT

```
////////////////////////////////////////////////
// Module : wrapper.sv
// Project : FDM UVM Verification
// Task : Creates the FDM module wrapper
// Author : Zenith & Laksh
////////////////////////////////////////////////

module QPSK_wrap(FDM_interface.qpsk_mp FDM_inf);

QPSK QPSK_dut(.clk(FDM_inf.clk),
    .rst(FDM_inf.rst),
    .stopout(FDM_inf.stopout),
    .pushin(FDM_inf.pushin),
    .datain(FDM_inf.datain),
    .firstin(FDM_inf.firstin),
    .stopin(FDM_inf.stopin),
    .pushout(FDM_inf.pushout),
    .dataout(FDM_inf.dataout),
    .firstout(FDM_inf.firstout));

endmodule : QPSK_wrap
```

Fig. 8. FDM Test

Interface Module FDM: An interface encapsulates all the signals inside a common file shared across DUT and Driver and Monitor. The code's potential for reuse might be improved by logging all relevant signals. There is a possibility that the same interface is used in all other UVM verification settings. No physical connections are made between the input and output signals. Environment Module FDM: Agent and score-board setup and instantiation happen in a DUT setting. The environment scoreboard and agent component are created upon installation. Both the scoreboard and the agent are constructed using id:create types. The advantages of this method make it widely employed at UVM, particularly for overriding.

When the construction is done, you may begin the run phase. Scoreboard Module FDM: Regardless of the task, UVM Scoreboards can handle it. Typically, the monitor's output is utilized for scoreboards. There are two types of models included in scoreboards: predictor and checker methods.

Monitor Module FDM: The data flowing out of the DUT is monitored by UVM Monitor, and then converted into a bitstream. The monitor then sets up a line of communication with the scoreboard through the TLM method.

FDM Sequence and Sequence Item Module: The sequence is responsible for producing all the user-defined and designed stimuli that are given to the DUT. Engineers sometimes resort to arbitrary limits because they cannot provide significant stimulus. The initial sequence is stretched even more by the uvm. Inline restrictions are used to modify the last two bytes of the data that is being entered. The stimulus takes in several different numerical values, all of which it then relays to the DUT by way of its driver.

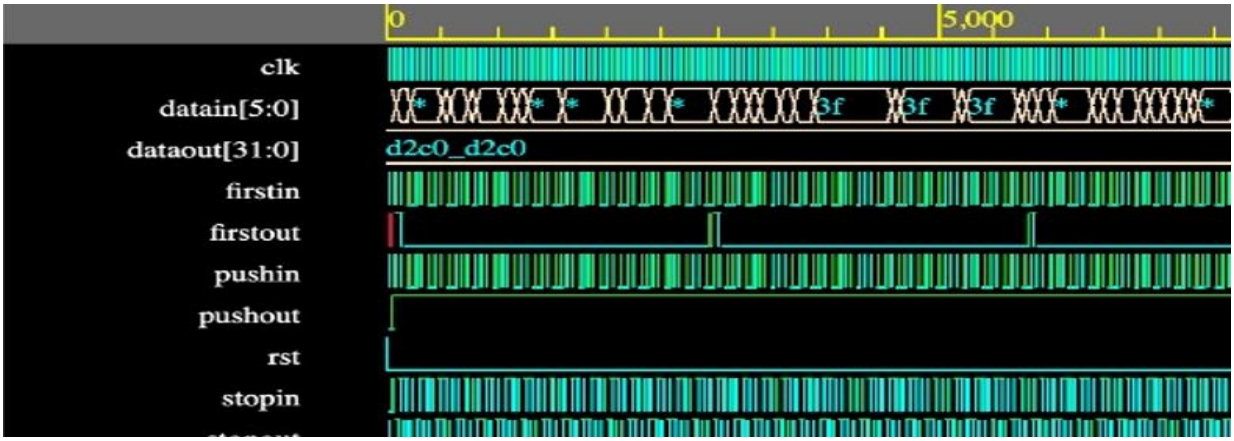

Fig. 9. Waveforms

ISBN: 978-988-14049-4-7
ISSN: 2078-0958 (Print); ISSN: 2078-0966 (Online)

IV. Conclusion

Writing the test bench for the Design Verification has become an extremely simple task thanks to the assistance provided by the Universal Verification Methodology. During this research, the UVM-based verification of the OFDM transmitter was carried out. As part of this project, fundamental UVM classes that are essential to have to finish the verification environment were developed. Within the scope of this project, the OFDM transmitter was tested and validated using the black-box verification strategy.

The project's current capability is only the verification of the Orthogonal FDM Transmitter but due to the abstraction level verification technique, the scope of this project can be extended to verifying the receiver of the Orthogonal FDM system. Moreover, the options of assertions can also be added to the design because the verification environment is made of dynamic entities, and the design environment is made of static entities and assertions are static.

Reference

[1] Xuan, G., Zhang, Z., & Liu, C. (2019). Design of QPSK Sequences for M-Ary Spread Spectrum OFDM Systems. 2019 12th International Congress on Image and Signal Processing, BioMedical Engineering and Informatics (CISP-BMEI). doi:10.1109/cisp-bmei48845.2019.8965673

[2] Nadar, J. I., Koti, J., & Jayaswal, D. (2014). OFDM pilot-based channel estimation. 2014 International Conference on Advances in Engineering & Technology Research (ICAETR - 2014). doi:10.1109/icaetr.2014.7012812

[3] Hamilton, B. R., Ma, X., Kleider, J. E., & Baxley, R. J. (2011). OFDM Pilot Design for Channel Estimation with Null

[4] IEEE Transactions on Wireless Communications, 10(10), 3145–3150. doi:10.1109/twc.2011.090611.101922

[5] Naveen Kumar, Rohith S, H Venkatesh Kumar, "FPGA Implementation of OFDM Transceiver using Verilog - Hardware Description Language," September 2014 International Journal of Computer Applications (0975-8887), volume 102 – No-06

[6] Ray Salemi, The UVM Primer: A Step-by-Step Introduction to the Universal Verification Methodology, 1st Edition, 2013, Guide to Learning the Testbench Language Features, Marlboro, MA, Ray Salemi, The UVM Primer: A Step-by-Step Introduction to the Universal Verification Methodology, 1stE0dition, 2013

[7] Kathleen A Meade, Sharon Rosenberg, A Practical Guide to Adopting Universal Verification Methodology (UVM), Second Addition, San Jose, CA, 2013, ISBN : 978-1-30053592-5

ISBN: 978-988-14049-4-7
ISSN: 2078-0958 (Print); ISSN: 2078-0966 (Online)