Proceedings of the World Congress on Engineering 2007 Vol I
WCE 2007, July 2 - 4, 2007, London, U.K.

Analog Spiking Neuron with Charge-Coupled Synapses

Yajie Chen*, Steve Hall*, Liam McDaid†, Octavian Buiu*, and Peter Kelly†

Abstract—**This paper presents a compact analog neuron cell with an array of charge-coupled synapses connected via a common output terminal. Synaptic responses are fed into a current mirror, the summing point of the neuron. A couple of CMOS inverters are employed to implement the temporal and spatial integration of weighted input spikes generated by the synaptic array. The decay of the membrane potential is mimicked by the charge leakage through a reverse-biased diode, whose model is verified by comparing the simulations and measured data. Spice simulation results show that the proposed neuron cell is capable of capturing the summing and thresholding dynamics of biological neurons.**

Keywords: ***neuromorphic circuits, silicon synapse, spiking neuron***

1 Introduction

In the effort to attain human-level intelligence in both hardware and software, a considerable amount of neural network research has been performed where learning algorithms, trainable networks, dedicated hardware and applications have all been developed throughout the past few decades. Recently experimental evidence has revealed that the traditional mean firing rate method could not describe brain activity since the reaction times are too short to allow temporal averaging for the calculation of the mean firing rate. This has given rise to the interest of alternative coding techniques which has led to the recent trend of Spiking Neural Networks (SNNs), an essential component in information processing by the brain [1]. Therefore much exciting research aimed at implementing human-level intelligence within networks of neurons has been proposed recently [2]-[4]. However these implementations require complex circuitry and consequently the power dissipation of the neuron circuit could be a major problem especially for large network level. Achieving high neuron density and low power operation are major constraints in the development of silicon neural systems.

In this paper, we present a biologically plausible neuron cell based on our recently developed charge-coupled synapse [5]. This silicon synapse produces a weighted spike characteristic using a simple device and when embedded in a point neuron cell, a time dependent output is produced; the output being referred to as the post-synaptic potential (PSP). The signals from charge-coupled synapses are integrated as the summed current by a current mirror configuration where an array of synapses can be connected via a common output node. The functionality of thresholding is realised by a CMOS inverter, which accumulates the weighted charges and captures the time dependency of the postsynaptic membrane decay.

*Department of Electrical Engineering & Electronics, University of Liverpool, Liverpool L69 3GJ, UK (Email: y.chen2@liverpool.ac.uk; s.hall@liv.ac.uk).

†School of Computing & Intelligent Systems, University of Ulster, Londonderry, BT48 7JL, UK (Email: lj.mcdaid@ulster.ac.uk).

2 The Charge-Coupled Synapse

We now review our charge-coupled synapse which is capable of mimicking the spiking dynamics of a biological synapse. Fig. 1 shows the n-channel, two-phase charge-coupled synapse, essentially consisting of two MOS capacitors in series. For the present study, we consider that a voltage, representing the weight, is placed on the first capacitor, but the intention in due course, is to include a floating gate upon which charge can be stored in a similar manner to that of non-volatile memory. The second MOS capacitor serves as the input node of the synapse which is triggered by the pre-synaptic signal. This device mimics the exhibitory synapse. An inhibitory synapse could be implemented as a p-channel charge-coupled device. The output is formed by an n-type implant, on the right hand side of Fig. 1. The n-implant to the left can be used as a minority carrier injector, to speed up the non-

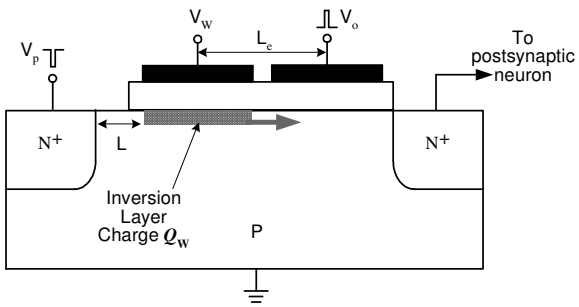

Figure 1: Schematic view of the n-type charge-coupled synapse.

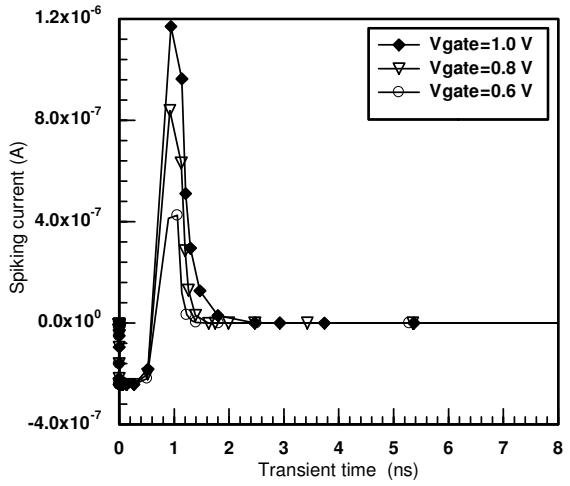

Figure 2: Spiking characteristics of the charge-coupled synapse.

equilibrium relaxation response of the device to achieve biological scale time regimes [6].

The synaptic weight is stored as the charge packet Q_{W} in the inversion layer of the first MOS capacitor. Note that the amount of charge increases linearly with the applied voltage on the first MOS capacitor which operates in the strong inversion state. Therefore the weight modification depends on the updating of the magnitude of the voltage V_{W}; weight storage will be considered in a subsequent publication. At the instant that the pre-synaptic neuron sends out a spiking signal, the second MOS capacitor is driven into the deep depletion state, and the weight charge is released to the output terminal due to the lateral potential variation. Consequently the synapse computes the weighted signal as an output current as shown in Fig. 2. The majority of charge is transferred within a few nanoseconds, and the amplitude of the spiking current is proportional to V_{W}. We use this relationship to implement synaptic plasticity.

3 The Spiking Neuron

In ideal spiking neurons if the sum of the inputs, from different dendrites, surpasses a particular threshold then a spike is produced which propagates along the axon to other synapses. The integrate-and-fire (I&F) neuron model consists of a capacitor and a threshold device [1]. Fundamentally the cell membrane acts as a capacitor where the potential of the cell membrane can be modeled as the response of a capacitor to an injection of current. In response to a stimulant current the capacitor is charged, and when the potential reaches level, a spike is produced and the potential subsequently returns to the resting potential. The concept presented here however, represents a new paradigm to realize a spiking neuron, which has the potential to build more biologically plausible networks.

The circuit diagram of the proposed silicon neuron cell is shown in Fig. 3. M_1-M_2 constitutes a current mirror which is used to integrate the weighted current spikes from a number of n-type charge-coupled synapses. M_3-M_4 forms a CMOS inverter that thresholds the summed signals and generates an output hi-lo transition indicating that the neuron has fired. A 'leaky' diode D_1 enables charge leakage that effectively mimics the PSP decay of biological neurons. M_7 is controlled by the feedback of the neuron output of the second CMOS inverter M_5-M_6, and serves to reset the neuron cell after firing. The second CMOS inverter gives a lo-hi transition and is the actual output which is fed to subsequent synapses.

The charge-coupled synapses are directly connected to the drain of M_1 via a common output terminal. Note that the leakage of charge through the p-n junction formed by the output terminal and the substrate in the silicon synapse is controlled by the thermal generation lifetime and this process is orders of magnitude greater than the aforementioned charge transfer time. Therefore we can consider that no charge is lost during the summing operation. A refractory period is present after the integration of the spiking currents because the recovery of the silicon synapses from the deep depletion conditions takes the order of milliseconds when we employ lifetime quenching. Note that a pulse V_p applied to the left hand n+ region of Fig. 1, causes injection of minority carrier electrons to facilitate and control this relaxation process.

3.1 Current Mirror Operation

All n synaptic output signals are integrated onto the drain of M_1. The transfer of weighted charge packets in n-connected silicon synapses results in a current I_{in}. Two p-channel devices which can be triggered by I_{in} are required in the current mirror configuration. Therefore the accumulated charge is transferred to the drain of M_1, the reference current I_{in} increases and is mirrored as I_{sum} in M_2. The current I_{sum} charges the gate voltage V_{sum} of the first CMOS inverter and D_1 is now under reverse bias.

Assume that two p-channel MOSFETs, M_1 and M_2, have the same oxide thickness and threshold voltage. The current for M_1 (assuming a long channel device) in saturation, whose source and substrate is connected to V_{dd}, is given by:

$$I_{in} = k_1 \frac{(V_{GS} - V_T)^2}{2} \tag{1}$$

where $k_1 = \mu C_{ox} \frac{W_1}{L_1}$ is the gain factor of M_1, and $V_{GS} = V_{in} - V_{dd}$.

The summed current from the synaptic array sets the V_{in} to:

$$V_{in} = V_T + V_{dd} - \sqrt{\frac{2I_{in}}{k_1}} \tag{2}$$

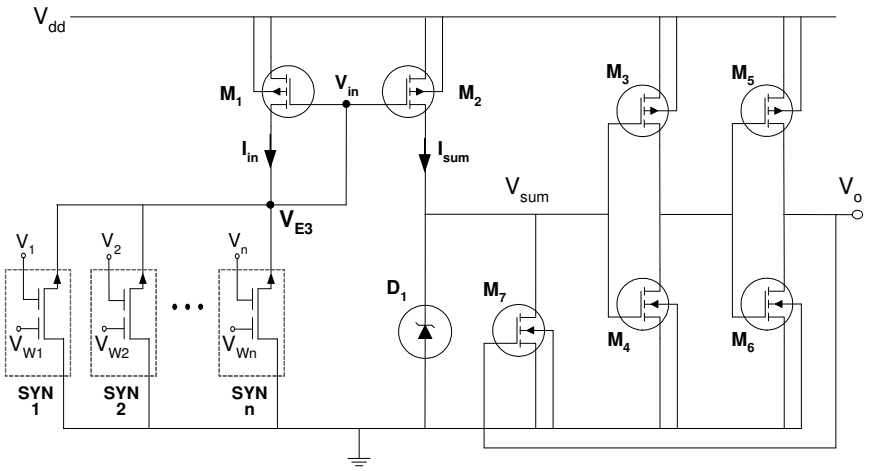

Figure 3: The analog neuron circuit with an array of n-type charge-coupled synapse; The integration and thresholding functions are implemented by the current mirror configuration and CMOS inverter respectively.

By using appropriate W_1/L_1 ratio, larger fan-in of the current mirror can be achieved, allowing the integration of a large number of synapses. For the device with equal W_1 and L_1, 20 nm oxide, and the power supply of 3 V, the approximated number of synapses in one-dimensional array can be 320. M_2 is then controlled by V_{in}, and the output current I_{sum} is obtained:

$$I_{sum} = k_2 \frac{(V_{in} - V_{dd} - V_T)^2}{2} \tag{3}$$

where $k_2 = \mu C_{ox} \frac{W_2}{L_2}$ is the gain factor of M_2.

Substitute (2) into (3), the current I_{sum} is expressed as a function of I_{in}:

$$I_{sum} = \alpha I_{in} \tag{4}$$

where $\alpha = \frac{W_2 L_1}{W_1 L_2}$ is the aspect ratio. This allows current signals to have a fan-out greater than one and each output can be scaled using appropriate W/L ratios. If M_1 and M_2 are matched in all respects, $I_{in} = I_{sum}$. After the spike emission period, V_{in} is driven back to V_{dd} causing the resetting of the common output terminal of the synaptic array.

3.2 Thresholding Operation

The CMOS configuration is employed in the circuit to perform the thresholding function which plays an important role in neuron computation. The summed current I_{sum} will charge the gates of M_3-M_4, causing the membrane voltage V_{sum} to increase. Consider the case where only one synapse is activated, and assuming a charing duration of τ_r. Therefore the membrane voltage can be expressed as:

$$V_{sum} = \frac{1}{C_{ON}} \int_0^{\tau_r} I_{in} dt \tag{5}$$

where $C_{ON} = C_D + C_p$ is the capacitance at the membrane node; C_D is the diode capacitance; C_p is the capacitance associated with the CMOS input gates.

The discharging of the gates of M_3-M_4 is due to the leakage through the reverse-biased diode D_1, as shown in Fig. 3. A 'leaky' diode with a reverse-current characteristic dominated by Zener tunneling is preferred and results in biological scale relaxation rates. A numerical solution gives us the approximation that $\tau_r << t(V_{sum})$ [6].

The switching threshold V_{Th} for CMOS inverter is defined at the point where the input and output voltages are equal. Assume the voltage supply is high enough so that the transistors operate in saturation. The expression for V_{Th} is given by:

$$V_{Th} = \frac{(V_{T4} - \frac{V_{DSAT4}}{2}) + r(V_{dd} + V_{T3} + \frac{V_{DSAT3}}{2})}{1 + r} \tag{6}$$

where V_{T3} and V_{T4} are the threshold voltage of pMOSFET and nMOSFET; V_{DSAT3} and V_{DSAT4} are the saturation drain voltages for M_3 and M_4 respectively; $r = \frac{k_3 V_{DSAT3}}{k_4 V_{DSAT4}}$ assuming equal oxide thickness; k_3 and k_4 are the gain factors.

When I_{in} increases sufficiently to make V_{sum} exceed the switching threshold of the CMOS inverter, M_3 is on and in saturation and M_4 operates in the linear region. The output voltage is then located at low level, which means the neuron has fired. Subsequently the output voltage V_o of the neuron will increase rapidly and turn on the transistor M_7. This discharging action resets the inputs of M_3-M_4, and the output V_o is constrained by the feedback to be a very short voltage spike.

4 Results and Discussion

The silicon neuron circuit is simulated in Spice. The models are defined to match the devices fabricated in 0.5 μm

process. The oxide thickness of the accompanying transistors is set to 20 nm which is used for charge-coupled synapse to provide enough fringing field. The threshold voltages of the p- and n-channel transistors are -0.74 V and 0.74 V respectively. For all the transistors, the same width and length are used (W=L=1.2 μm). Note that the size of the transistors can be varied to demonstrate the exact behavior of the realistic biological neurons. We represent the output of the charge-coupled synapses using current pluses of amplitude 1.2 μA for each activated synapse. The power supply V_{dd} is set to 3 V.

A low breakdown 'leaky' zener diode, whose reverse leakage is dominated by Zener tunneling, is employed to form a leakage path. This allows the discharge of the PSP which mimics the decaying of the membrane potential in biological neurons. Fig. 4 shows the I-V curves of the zener diode under non-zener condition. Good correlation between the modeled and measured characteristic is evident.

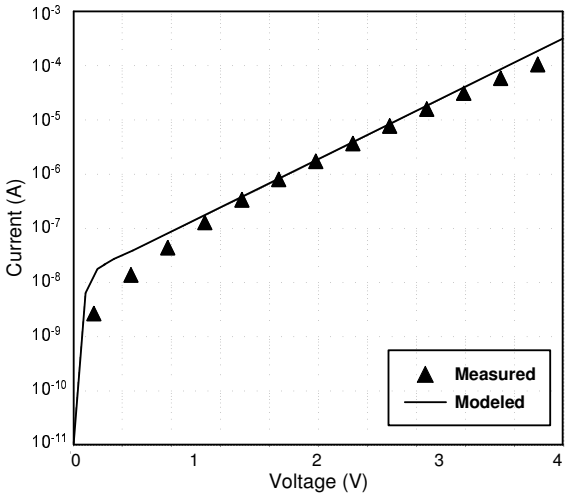

Figure 4: Measured and modeled I-V curves of the reverse-biased zener diode with breakdown voltage of 4.7 V.

In our experiment, 100 synapses were activated concurrently and the accumulated peak in current is 120 μA. The membrane node voltage V_{sum} at the gates of M_3-M_4 is shown in Fig. 5. The voltage, following the rise of the synaptic signal, has a fast rise time reaching a peak value 2.7 V which causes the first CMOS inverter to change state as shown in Fig. 6(b), demonstrating the firing of the biological neuron. Due to the leakage of D_1, the PSP shown has a much slower fall time of the order of milliseconds, exhibiting the characteristic shape observed in biological neurons.

Fig. 6(a) shows the accumulation of successive PSP signals when the synapses emit spikes with various time lags. In this simulation, there are 30 active synapses divided into 6 groups where each synapse is activated at the same

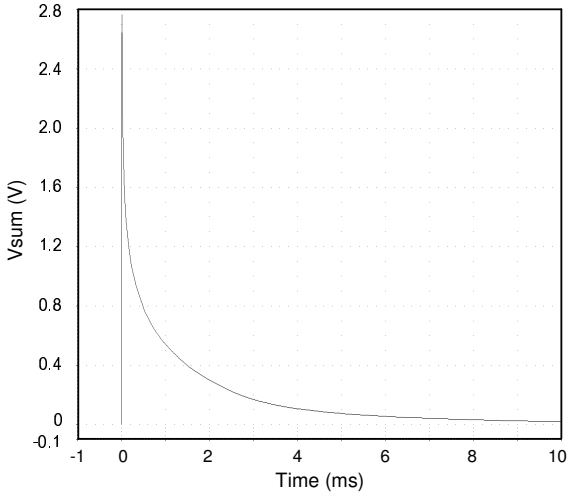

Figure 5: The membrane potential V_{sum} when the spikes are generated at the same time.

time with an interval between each group. The associated accumulation of charge produces the V_{sum} shown in Fig. 6(a). Therefore, the threshold is reached and the CMOS inverter is triggered to send out a spike, as shown in Fig. 6(b). Because the membrane node discharging is of the order milliseconds, the accumulation behavior is limited by the interval between each group. If we assume 2 ms interval, the majority of charges are used to compensate the leakage rather than commit to neuron's firing. In addition, any spike arriving after the resetting of the membrane node will contribute to the subsequent firing events. It is worth noting that the resetting signal to the gate of M_7 should have a certain delay to ensure the neuron output V_o has a fan-out capable of driving multiple synapses on subsequent layers.

5 Conclusion

An analog neuron cell is presented in this paper. It consists of a current mirror, two CMOS inverters and a leaky diode for the charge leakage which emulates PSP. The spiking current emitted by the array of charge-coupled synapses is easily integrated onto the membrane node which is the gates of the first CMOS inverter. The neuron circuit is capable of aggregating signals which contribute to the firing of the neuron. A reverse-biased leaky diode is used here to form a leakage path for the decay of the membrane node allowing the spike decay to be implemented. Since the charge-coupled synapse requires minimal area and operates at low power, it can be scaled to achieve a low power spiking neural networks. Simulations were presented to verifies that the proposed neuron cell implementation is feasible and has the potential for implementing biological neural networks in hardware.

ISBN:978-988-98671-5-7

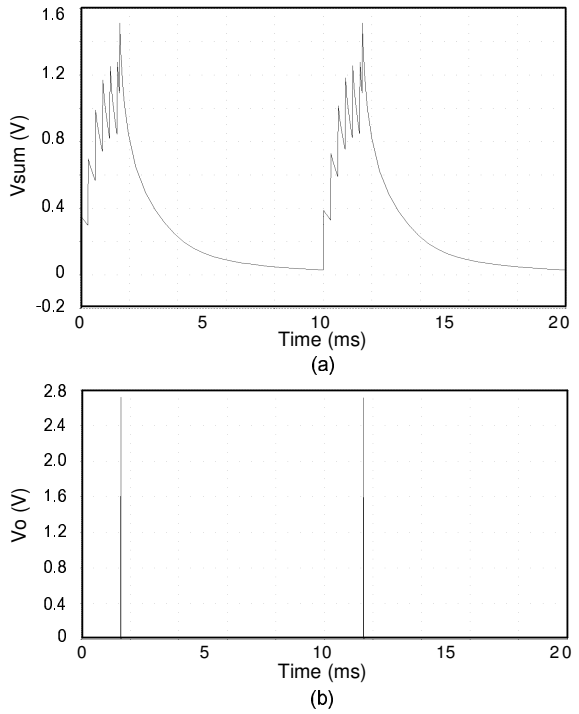

Figure 6: (a) The membrane potential V_{sum} when a series of spikes are generated with various time lags; (b) The output voltage of the second CMOS inverter M_5-M_6. The neuron fires when the membrane potential exceeds the threshold of CMOS inverter.

References

[1] Gerstner, W., Kistler, W.M., *Spiking Neuron Models: Single Neurons, Populations, Plasticity*, Cambridge University Press, 2002.

[2] Liu, S.C., Douglas, R., "Temporal Coding in a silicon network of integrate-and-fire neurons," *IEEE Transactions on Neural Networks*, V15, N5, pp. 1305-1314, 2004.

[3] Bofill-i-Petit, A., Murray, A.F., "Synchrony detection and amplification by silicon neurons with STDP synapses," *IEEE Transactions on Neural Networks*, V15, N5, pp. 1296-1304, 2004.

[4] Indiveri, G., Chicca, E., Douglas, R., "A VLSI array of low-power spiking neurons and bistable synapses with spike-timing dependent plasticity," *IEEE Transactions on Neural Networks*, V17, N1, pp. 211-221, 2006.

[5] Chen, Y., Hall, S., McDaid, L., Buiu, O., Kelly, P., "On the design of a low power compact spiking neuron cell based on charge-coupled synapses," *IEEE International Joint Conference on Neural Networks*, Canada, pp. 1511-1517, 2006.

[6] McDaid, L., Hall, S., Chen, Y., Buiu, O., Kelly, P., "A biologically plausible spiking neuron cell in hardware," submitted to *IEEE Transactions on Neural Networks*, 2007.