On Line Surface Roughness Measurement Using Image Processing and Machine Vision

M.Rajaram Narayanan, S.Gowri, M.Murali Krishna

***Abstract* - Machine vision has evolved to become a mainstream automation tool, enabling computers to replace human vision in high speed and precision manufacturing techniques. Images usually acquired through modern cameras may be contaminated by a variety of noise sources and decreasing intensity and in most cases the type of noise and state of lighting are also not known a priori. In this paper, the design of image operator for illumination enhancement and noise filtering using evolutionary approach is presented. The advantage of the proposed structure is that it is evolved from primitives. The evolvable hardware (EHW) configuration uses reconfigurable Xilinx Virtex2 FPGA xc4000 architecture. The developed image operator is tested for its performance by applying it on images of surfaces of machined components grabbed using vision systems with linearly decreasing intensity. The evolutionary enhanced image is then processed and a relationship between the feature of the surface image and the actual surface roughness is obtained using regression analysis. Comparing with the stylus method, the constructed computer vision system is useful method for measuring the surface roughness with faster, lower environment noise and lower price in computer integrated manufacturing process (CIM).**

Keywords: **Evolvable hardware, Neural network. Surface Roughness,**

I. INTRODUCTION

Evolvable systems (EHW) are hardware units that are built on software reconfigurable logic devices such as FPGA and PLD and whose architecture can be reconfigured using genetic learning. To design conventional hardware, it is necessary to prepare all the specification of the hardware functions in advance. In contrast to this, EHW continues to reconfigure itself without such specifications to achieve a better performance. The basic idea of EHW is to regard architecture bits of a reconfigurable device as a chromosome for GA, which searches for an optimal hardware structure. In the field of digital image processing particularly, a broad and disparate range of applications using evolutionary computation may be found in the literature, including the use of genetic algorithms in the segmentation of medical resonance imaging scans [3], a genetic program that performs edge detection on one-dimensional signals [4], the evolution of genetic programs to detect edges in petrographic images [5], and the evolution of spatial masks to detect edges within gray scale images.

This paper, presents evolvable hardware architecture, dedicated for implementing high performance image noise filtering on a custom Xilinx Virtex FPGA xcv1000, together with a flexible local interconnect hierarchy. After processing the initially grabbed images using the EHW system, the improved quality images of surfaces are used for evaluation of surface finish.

II. EVOLVABLE HARDWARE SYSTEM

The EHW architecture can be classified into functional and gate level [2] and is shown in figure1 and 2. In gate-level EHW, the architecture bits of PLDs are treated as GA chromosome. The architecture bits can be downloaded on PLDs. Such downloading can be engaged in either during or after the learning process.

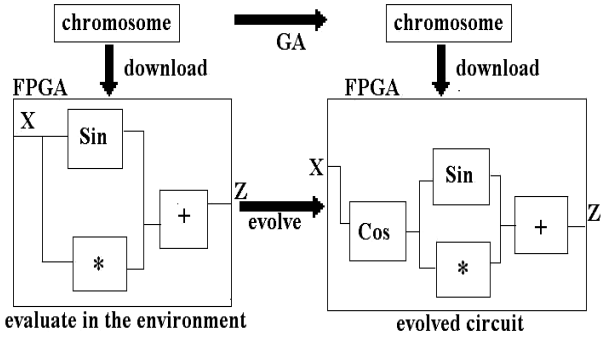

Fig. 1 Functional level evolution

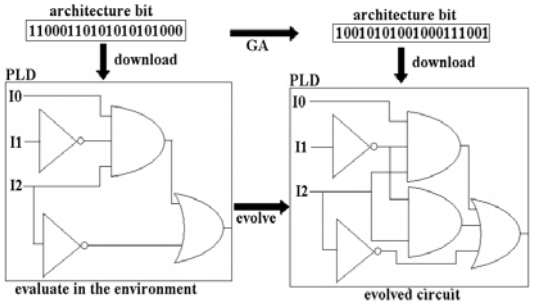

Fig. 2. Gate level evolution

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III. MEASUREMENT OF THE SURFACE IMAGE OF WORKPIECE

A schematic diagram of the machine vision system for inspecting surface roughness in milling operations is shown in fig. 3. It consists of the light source and a CCD camera of 512 x 640 resolution to capture the image of the surface, the captured image is given to the EHW system for subsequent analysis and image processing.

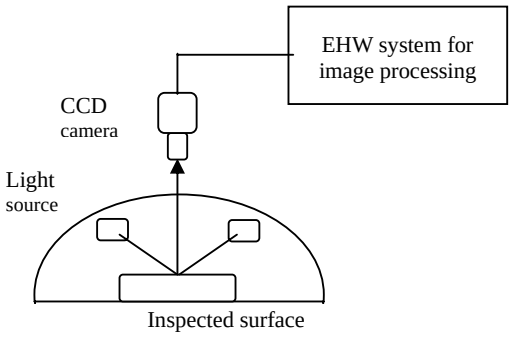

Fig.3. Machine vision system

estimate surface roughness under different cutting conditions ,a number of cutting tests were carried out using a Milling machine with carbide tool and working on mild steel bars. Experimental data with regard to different cutting parameters (feed, speed and depth of cut) were performed. Machined surface roughness was estimated by a profile meter (Surfcorder SE1200) within a sampling length of 8mm and measurement speed of 0.5mm/s.

The surface roughness parameter used in this study is the average surface roughness (R_a). It is defined as the arithmetic average of the absolute value of the heights of roughness irregularities from the mean value measured and is given by

$$R_a = \sum_{i=1}^{n} \frac{|y_i|}{n} \quad (1)$$

where y_i is the height of roughness irregularities from the mean value and 'n' is the number of sampling data. In this work, the arithmetic average of the gray level is used to estimate the surface roughness of the work-piece. The arithmetic average of the gray level can be expressed as

$Ga = (\sum(|g_1 - g_m| + |g_2 - g_m| + ... + |g_n - g_m|)/n$ where g_1, ---, g_n are the gray level values of a surface image along one line and g_m is the mean of the gray values and is determined as

$$g_m = (\sum(g_1 + g_2 + ... + g_n))/n \quad (2)$$

IV. RECONFIGURABLE ARCHITECTURE

The virtual reconfiguration chip (VRC) of the EHW unit is shown in figure 4. In the present work, each PE except the first stage is assumed to receive inputs from any of the previous two stages. A total of 25 PE's used in the VRC. The genetic unit is programmed to give the best chromosome and using this, the initial configuration of the VRC is chosen. Each PE can handle 16 different functions as listed in Table – I

Table – I. Function codes

Code	Function	Code	Function
F0: 0000	X >> 1	F8 : 1000	(X+Y+1) >> 1
F1: 0001	X >> 2	F9 :1001	X & 0x0F
F2: 0010	~ X	F10: 1010	X & 0xF0
F3: 0011	X & Y	F11: 1011	X | 0x0F
F4: 0100	X | Y	F12: 1100	X | 0x F0
F5: 0101	X ^ Y	F13: 1101	(X&0x0F) | (Y&0xF0)
F6: 0110	X + Y	F14: 1110	(X&0x0F) ^ (Y&0xF0)
F7: 0111	(X+Y) >> 1	F15: 1111	(X&0x0F) & (Y&0xF0)

The logical configuration of the circuit is defined by a set of 25 inter triplets, one for each of the 25 PEs in the reconfigurable architecture. The first two integers of each triplet represent the source of inputs to the PE (cfg1 & cfg2) and the third integer of the triplet (cfg3) indexes the function (refer Table 1) to be applied by the PE.

V. EVOLUTION OF CHIP

The proposed EHW system is shown in figure 5. The configuration word contains details about the interconnection between the PE's of the VRC and the functional operations performed within each PE. For each PE, the multiplexer inputs are chosen from the outputs of the previous two columns. Both cfg1 and cfg2 are constrained such that they should not exceed the number of the multiplexer inputs. The cfg3 input is the binary representation of the number of functions in store.

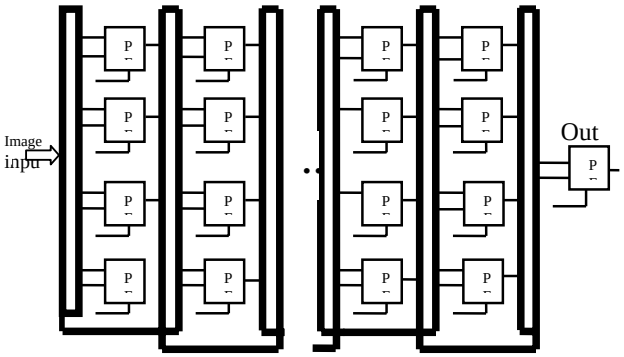

Fig. 4. Reconfigurable architecture

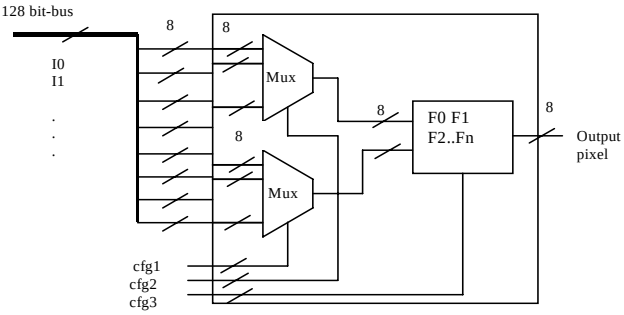

Fig. 5. Architecture of a single PE [output = F {mux(cfg1), mux(cfg2), cfg3}]

VI. DETAILS OF HIGH SPEED IMAGE PROCESSING CARD

The proposed video processing card is interfaced in the PCI bus & is a cost – effective platform for developing video & multimedia based applications. The card has an in board high speed video ADC & DAC. The board supports real time video processing of components video signals. The on board SRAM & Flash memories is used for storing data i.e. the configuration bits if the VRC. The Genetic processor code is stored in the on board power PC. The developed card can be used as a standalone video processing board. The FPGA processor used in the board is XCZVP30. The card has five fully independent banks of IMX16SRAM & 3 fully independent banks of 512K x 16 flash PROM. The sampling rate is 30 MSPS. The prototype of the high speed card is shown in figure 6.

Fig 6. High speed Image Processing Card

VII. EXPERIMENTAL RESULTS

The surface images of the specimens grabbed using the CCD camera are given to the EHW Chip and the configuration word is selected to eliminate the effects of improper illumination and noise. Preprocessing is performed to enhance the quality of images. Given an input images. 'I' with a resolution m x n , the chip extracts the edges and replaces the original low quality image with an output image 'O'. For experiments the number of initial population is set to 16 each chromosome is evolved with crossover 0.9 and mutation 0.01. Figure 7 shows the images corrupted by noise and figure 8 shown the preprocessed images using the EHW system. The two images in figure 7 are the raw images obtained using vision system. The quality of the images is enhanced by 62.5% with the evolvable hardware chip unit.

Fig. 7. Images with noise

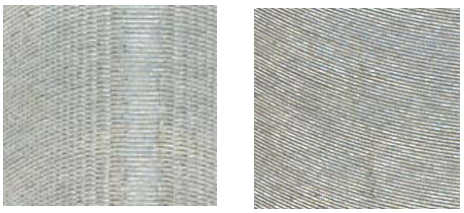

Fig.8. Images without noise

The surface roughness values obtained using the stylus approach along with the parameters feed, depth of cut (doc) and spindle speed are listed and the surface finish values obtained by using the evolvable hardware system on the milled surface is compared with other approaches and given in Table – II.

Table – II

S.N	Feed (mm/rev)	Doc (mm)	Speed (m/min)	R_a (Stylus) (µm)	R_a Reg. Analysis (µm)	R_a EHW (µm)
1	150	0.5	123	3.05	3.23	3.12
2	150	0.8	123	3.19	2.61	3.18
3	150	0.5	153	5.35	6.05	5.58
4	200	0.5	123	5.62	6.13	5.34
5	200	0.8	123	3.75	3.38	3.48
6	200	0.5	153	2.94	1.95	2.89

VIII. CONCLUSION

This paper has presented a genetic algorithm based EHW chip to inspect the surface roughness of components generated using milling process by preprocessing the images to remove the noise. The correlation obtained using regression approach after improving the quality of the surfaces using EHW system was better than that without enhancing the images. The experimental results clearly indicate that the proposed technique can be used to evaluate the roughness of the machined surfaces. Future direction of study is to be focused on using an artificial neural network (ANN) to predict the surface roughness using image features as input.

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