An Efficient Programmable Logic Device Implementation of the Second-order Extended Physical Addressing

Mountassar Maamoun, Abdelhamid Meraghni and Abdelhalim Benbelkacem

Abstract—**This paper describes an efficient Programmable Logic Device (PLD) implementation of the Second-order Extended Physical Addressing, connecting the microprocessor-based systems and the external peripherals. This addressing technique, based on the use of software/hardware systems and reduced physical addresses, enlarges the interfacing capacity of the microprocessor-based systems. The input of our system hardware part will be connected to the system bus. The output, which is a new bus, will be connected to an external device. To accomplish the bus communication, the hardware part realizes a conversion of system bus data into new bus addresses. Furthermore, the software part ensures the transfer, with distinct addresses, of the simple data and the data that is intended to be converted. The use of this system with three system addresses and N bit data bus gives a new bus with N bit data bus and 2^{2N} physical addressing capacity.**

Index Terms—**Interfacing, Bus communications, PLD, Software/hardware System, Second-order Extended Physical Addressing.**

I. Introduction

The I/O microprocessor-based systems communications are generally handled in the form of bytes, words, or double words for the most recent processors [1]. The physical communication between microprocessor-based systems and an external peripheral is ensured by enabling the address decoder as soon as the address of this latter peripheral is available on the system bus. This process explains why the installation of expansion cards sometimes causes conflict problems: it is possible that two cards can be assigned the same field of addressing or have overlapping fields.

The Second-order Extended Physical Addressing, similar to the Extended Physical Addressing, is an interfacing system which is aimed to reduce the use of physical addresses in microprocessor-based systems. Furthermore, it will improve the effective data exchange speed. The proposed system combines a software/hardware solution to obtain the above objectives. This solution consists in creating a new bus, made up of a data bus, an address bus and a control bus.

The suggested architecture is composed of both hardware and software parts. The first is made up of a new bus and an interface between the system bus and the new bus. The software part ensures the communication between the microprocessor-based system and our interface.

The preliminary version of the Extended Physical Addressing was published in the 14th IEEE-CCECE [2]. The bus transaction of the first and second order is published respectively in the Information Technology Journal [3] and the 7th IEEE International Symposium on Signal Processing and Information Technology [4]. The PLD implementation of the second order Extended Physical Addressing are presented in this paper.

The main technique of this interfacing system has been applied for the implementations of video signal generation [5].

II. Second-order Extended Physical Addressing

The Second-order Extended Physical Addressing is based on a mixed software/hardware architecture, which increases the hardware addressing capacity of the computers and the microprocessor-based systems.

In this system, we have used some addresses of the microprocessor-based system addressing area to cover a significant external memory capacity. The Extended Physical Addressing system represents the starting point of the Fast Physical Addressing system, the Accelerated Physical Addressing system and the Advanced Physical Addressing system.

Manuscript received February 28, 2008. This work was supported in part by the LATSI Laboratory, Department of Electronic, Blida University, Blida, Algeria and the LSIC Laboratory, (ENS) Kouba, Algiers, Algeria.

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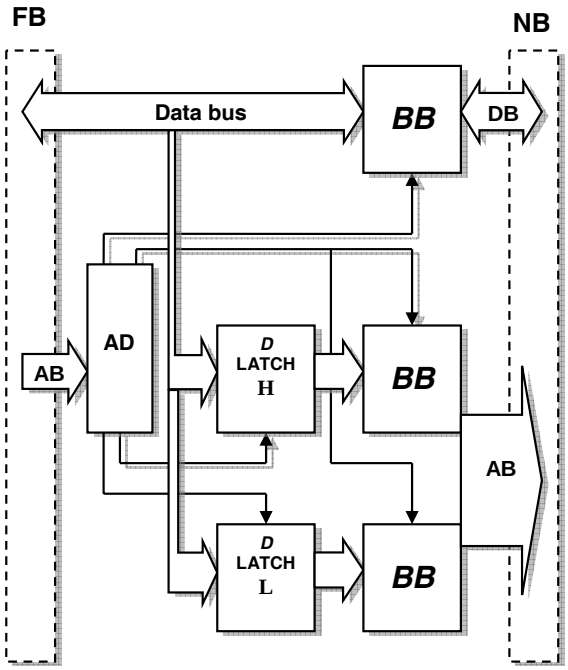
A. Hardware part

The hardware part of this system is made up of a new bus and an interface. This latter is intended for use as an interconnect between the system bus (or I/O expansion bus) and the device that will be addressed by this technique.



BB: Bus Buffer, **AB:** Address Bus, **DB:** Data Bus, **AD:** Address Decoder, **NB:** New Bus, **FB:** First Bus (System Bus or expansion Bus)

Figure 1. The Second-order Extended Physical Addressing bloc diagram.

The input of the interface of this system will be connected to the microprocessor-based system bus. The output will be connected to an external device, which contains the new data and addresses bus. Figure 1 illustrates the basic bloc diagram of the hardware part of the Second-order Extended Physical Addressing.

In our interfacing, the data bus ensures the transfer of the simple data and the transfer of the data that is intended to be converted into addresses (for the new bus). The software part of our system establishes the transmission of the two types of data in two steps and on distinct addresses, where the address decoder of the Second-order Extended Physical Addressing hardware enables the separation between the two data types.

B. Software part and I/O transactions

This technique can be done in two phases. The software ensures the presence of data intended to be present on the new bus as addresses (Figure 2**);** the decoder ensures the activation, with **adr1** and **adr2** respectively, of the **D "LATCH" L** and the **D "LATCH" H** to record these data and disables the three bus buffers until the second phase. **L** denotes the lowest part and **H** the highest part.

The addresses and data lines of the new bus will be at the high impedance state. In the second phase, the software ensures the presence of the data. Whereas, the three bus buffers are activated by the address decoder with **adr3**.

The data values on the new bus are identical to the system bus data of the second step (data3) and the address values are identical to the data of the system bus first step ([data2][data1]). Figure 3 presents the basic Extended Physical Addressing I/O transactions. We use two physical addresses, the first one the data/address conversion task and the other for the data transfer.

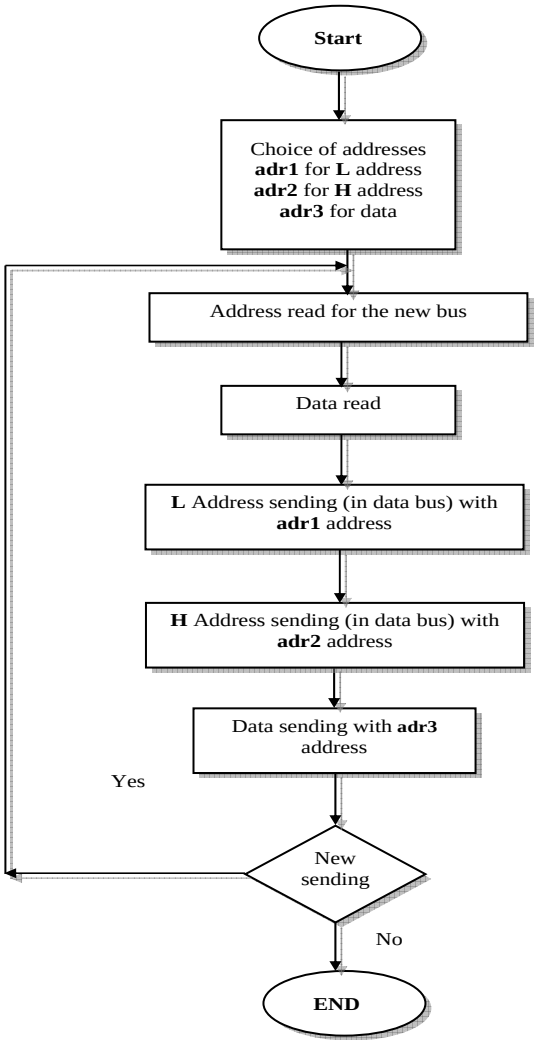


Figure 2. The Second-order Extended Physical Addressing software flow chart.

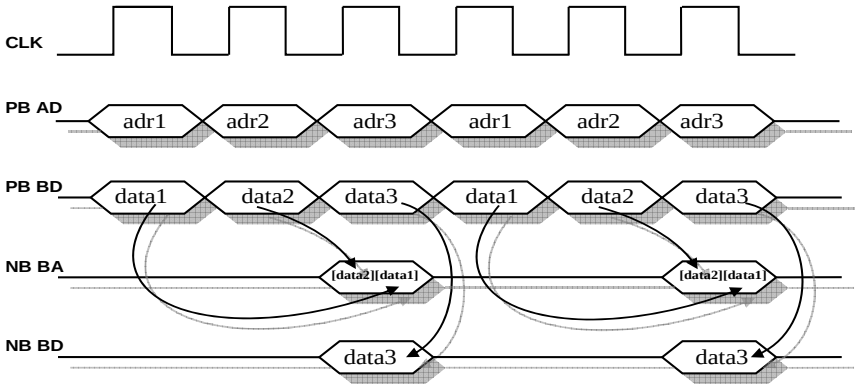


Figure 3. The Second-order Extended Physical Addressing main I/O transactions

The addressing capacity of the suggested system is directly related to the data bus size of the system bus or the used expansion bus. The control and the address lines of the first bus are used for the addresses decoding in the hardware part of our system. The control lines of the new bus will be designed according to two methods. Firstly, the control lines of the system bus will be adapted to produce the new control lines. Secondly, the new control lines will be designed with combinatory logic and according to our specified application.

III. PLD IMPLEMENTATION

In order to test the Second-order Extended Physical Addressing system, CPLD (Complex Programmable Logic Device) and FPGA (Field Programmable Gate Array) implementation are performed.
A Very High-Speed Integrated Circuit Hardware Description Language (VHDL) and the Engineering Capture System (ECS) is exploited to create the schematic. A Xilinx Integrated Software Environment (ISE) has been used for the programmable logic implementation on a Xilinx XC2V1000 Virtex-II and XC9572-10PC84 devices.

A model of schematic implementation is presented in figure 4. BUFE8 is an internal 3-State Buffer with Active High Enable and LD8 is a multiple Transparent Data Latch. The dec301_2_3 symbolize the address decoder. The VHDL architecture description of the address decoder are shown in figure 5.

The figure 6 illustrates a Second-order Extended Physical Addressing "Test Bench Waveform".

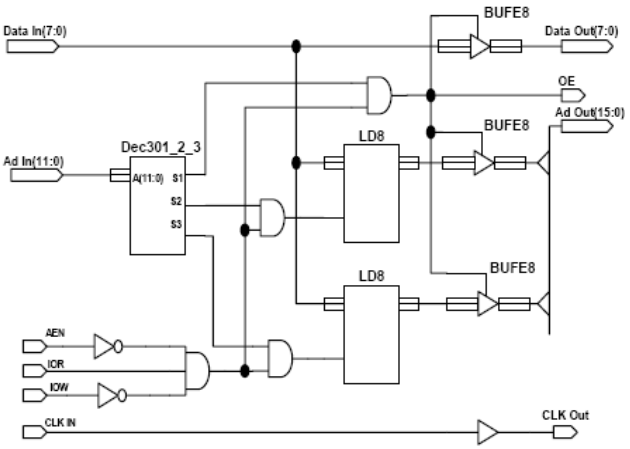


Figure 4. ECS Second-order Extended Physical Addressing schematic

```
entity dec301_2_3 is
  port (A : in std_logic_vector (15 downto 0);
        S1 : out   std_logic;
        S2 : out   std_logic;
        S3 : out   std_logic);
end dec301_2_3;

architecture DESCRIPTION of dec301_2_3 is
begin
            S1 <= '1' when A= x"0301" else '0';
            S2 <= '1' when A= x"0302"  else '0';
            S3 <= '1' when A= x"0303"  else '0';

end DESCRIPTION;
```

Figure 5. The VHDL architecture description of the address decoder

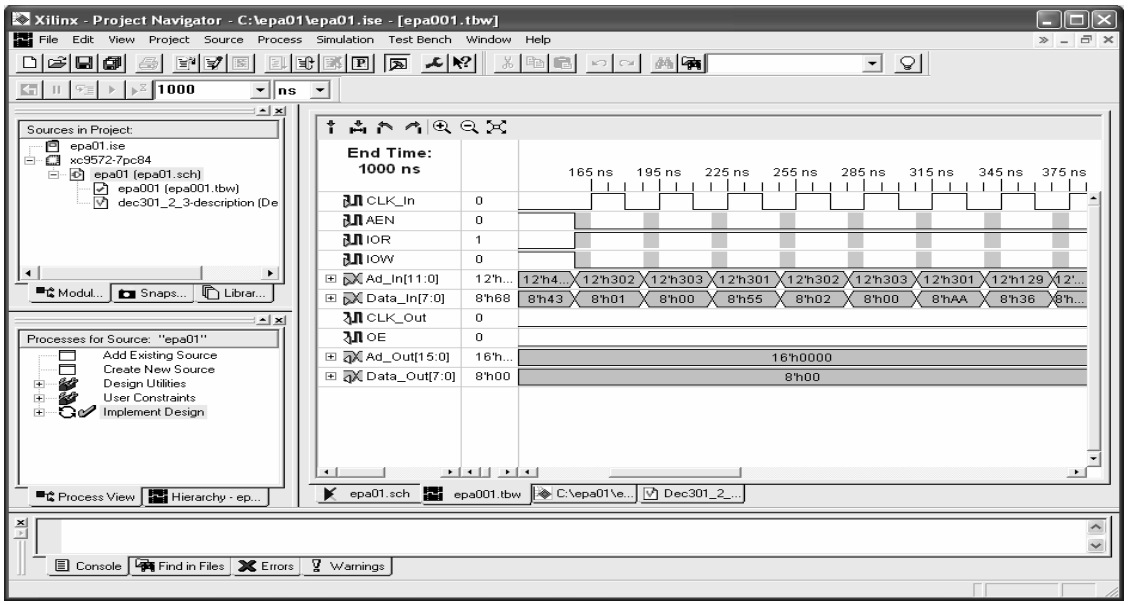


Figure 6. Second-order Extended Physical Addressing "Test Bench Waveform"

IV. RESULTS

The proposed architecture enlarges the physical addressing capacity of the microprocessor-based systems. Furthermore, this solution resolves the conflicts problems by the capability of using reduced system physical addresses with an adaptable address decoder.

The use of three addresses on an operating system bus with **N** bit data bus and operating at frequency **F** gives a new bus with **F/3** working frequency, **N** bit data bus and $\mathbf{2^{2N}}$ physical addressing capacity. The figure 7 illustrates a "ModelSim" simulation.

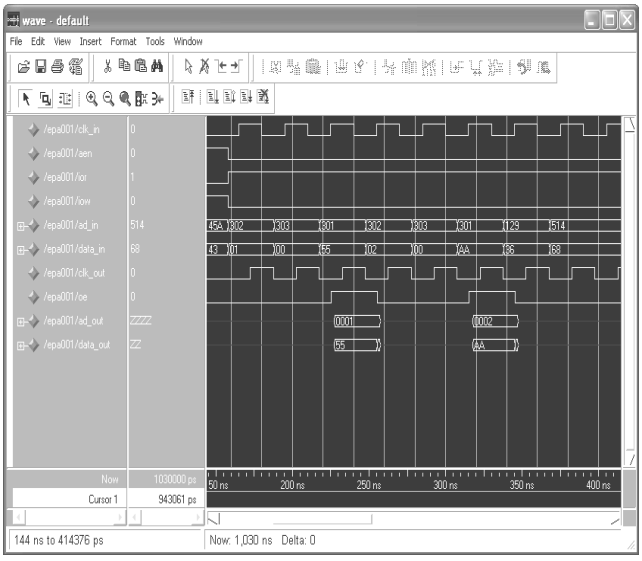


Figure 7. Second-order Extended Physical Addressing "ModelSim" simulation

V. CONCLUSION

In this paper, we have presented a PLD implementation of the Extended and the Fast Physical Addressing with programmable logic using Xilinx FPGA and CPLD devices. This proposed solution is based on the use of a mixed software/hardware system. This new system presents a solution for improving the physical addressing capacity of the microprocessor-based systems, which is independent of the addresses bus of the system bus. This new system presents a solution for improving the data communication capacity of the microprocessor-based systems, which is independent of the addresses bus of the system bus. The main technique of this interfacing system has been applied for the implementations of prototype cards which work on IBMTM computers and compatible [5].

REFERENCES

[1] Hesham El-Rewini and Mostafa Abd-El-Barr, "*Advanced Computer Architecture and Parallel Processing*", John Wiley & Sons Inc, USA. 2005.

[2] M. Maamoun. and G.Zerari, "Interfacing in Microprocessor-based Systems with an Extended Physical Addressing". *in Proc. 14th IEEE-CCECE*, Toronto, Ontario, Canada, 13-16 May 2001.

[3] M. Maamoun, A. Meraghni, A. Benbelkacem and D. Berkani, "Bus Transactions in Microprocessor-based Systems using the Extended Physical Addressing", *Information Technology Journal*, vol. 6, no7, pp 1104-1107, Sep. 2007.

[4] M. Maamoun, A. Benbelkacem and D. Berkani, "Bus Transactions in Microprocessor-based Systems using the Second-order Extended Physical Addressing", in *Proc. IEEE-ISSPIT*, Cairo, Egypt, pp 517-520, Dec 2007.

[5] Xilinx Product Specification, "*Xilinx XC9500 In-System Programmable CPLD Family*", Xilinx, Inc, USA. 2006..